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EDN

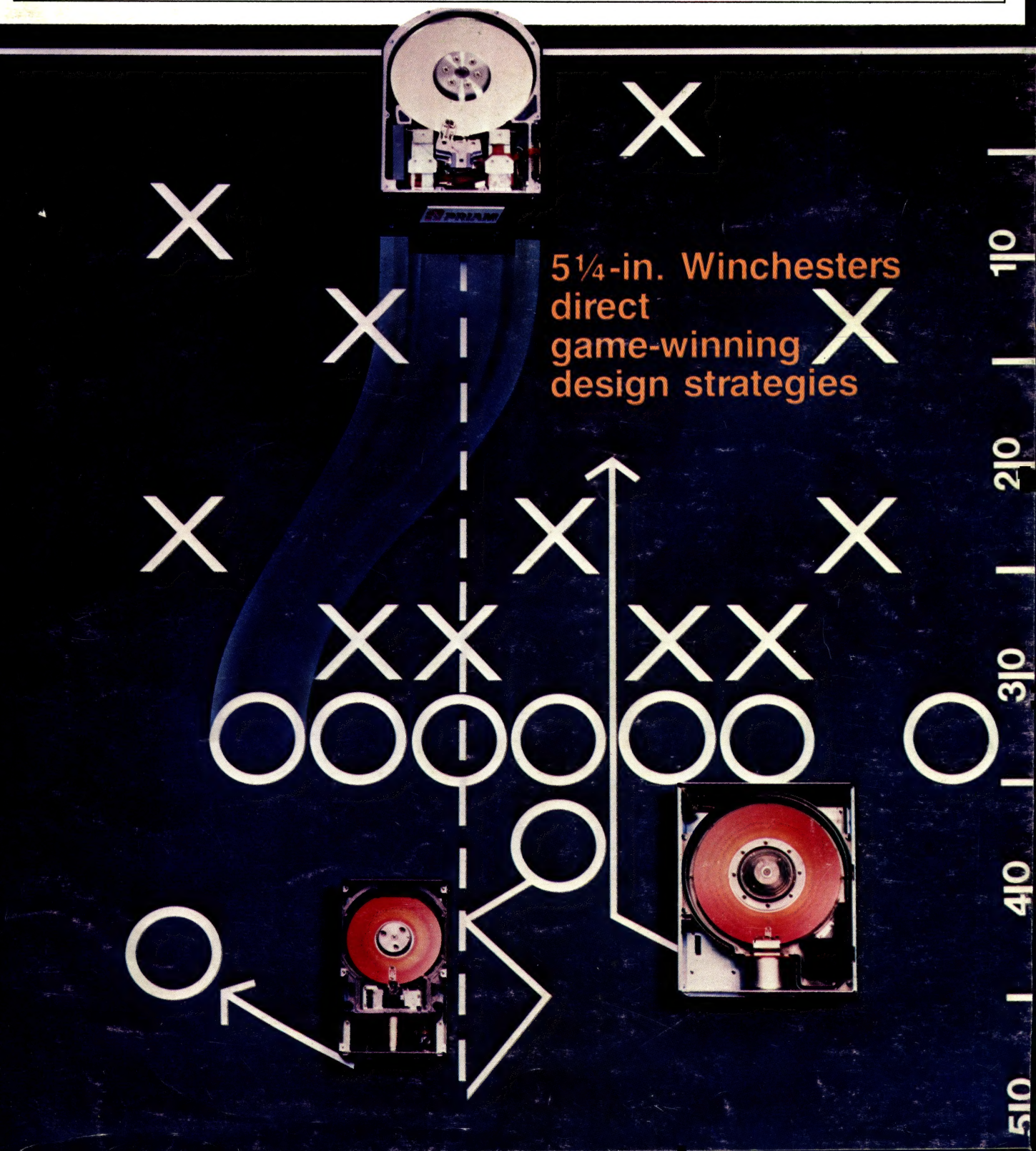
EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Software developments to highlight NCC 84

Use thermal effects to solve circuit problems

EDN networking project: LAN breadboard works

Track/hold amplifiers



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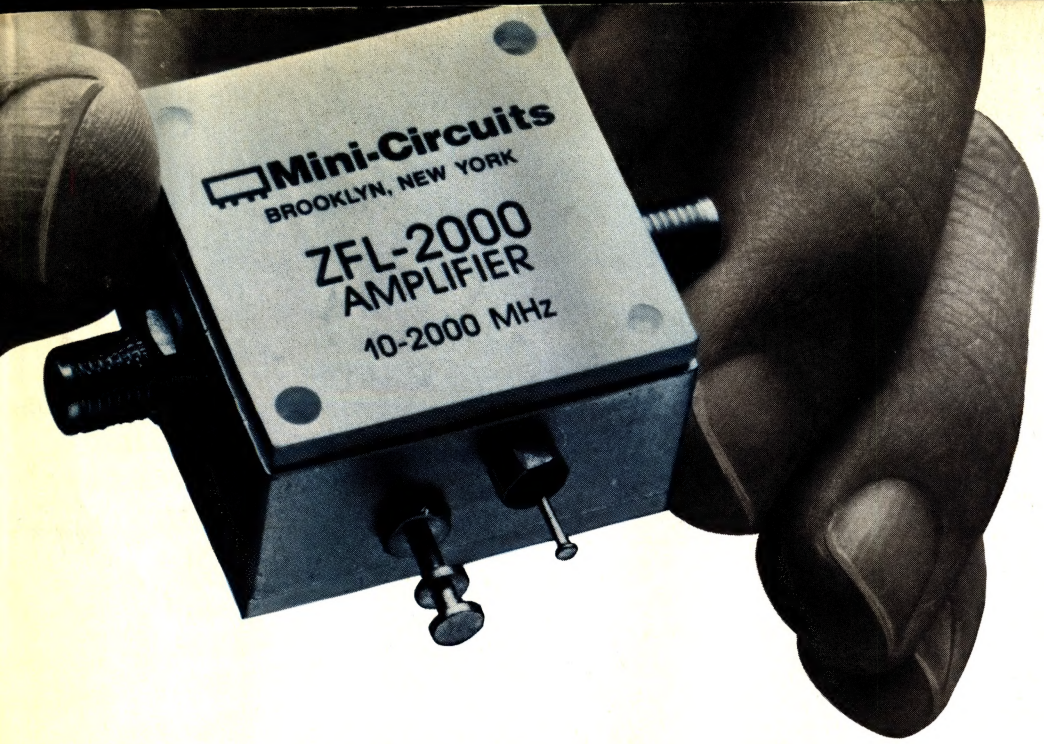


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INTERCEPT POINT (3rd order)	25 dBm
VSWR, 50 OHMS	2:1
DC POWER volt, current	+15 V, 100 mA
HEAT SINK	Internal
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—AT—10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1
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JUNE 28, 1984 • VOLUME 29, NUMBER 13 • EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

DESIGN FEATURES

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Winchester-disk-drive manufacturers continue to make technological innovations, pushing capacities, performance and packaging densities to significant new levels.

Additional LSI and hybrid parts ease completion of LAN 153
Bringing up the completed LAN-node breadboard turns out to be easy. Three volume-produced devices perform the difficult token-passing and line-interfacing tasks.

NCC sessions to highlight software developments 167
The latest demands of software engineering, along with many current hardware concerns, are the focus of more than 90 meetings at the Las Vegas show.

NCC '84 products 173
Reviews of noteworthy products slated for exhibition highlight some of the excitement in store for attendees in Las Vegas.

MOSFETs vie with Schottky diodes in low-voltage-supply designs 197
Lower R_{DS} renders the power MOSFET competitive with Schottky diodes for low-voltage, high-current power supplies. However, to take full advantage, carefully consider circuit implementation.

Hands-on chip analyses determine project success 212
In a blazing triumph of editors over technology, EDN's first semicustom ICs actually work. Performance and cost analyses prove that gate arrays easily satisfy our design objectives.

GaAs logic characteristics result in integration problems 225
The high speeds of gallium-arsenide logic devices create a new set of design constraints and challenges that occur from circuit conception and board layout through testing.

Take advantage of thermal effects to solve circuit-design problems 239
You probably consider thermal effects in circuits your enemy, but they can prove useful in many design situations.

Understand system partitioning to optimize custom-IC use 255
Custom and semicustom ICs provide myriad system benefits. Realization of these advantages requires effective partitioning of large systems into economically integrated segments.

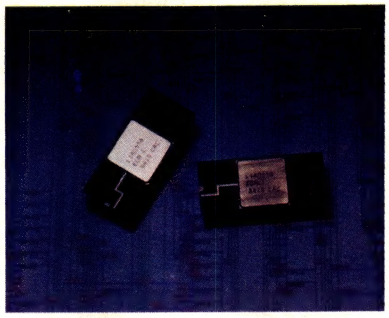
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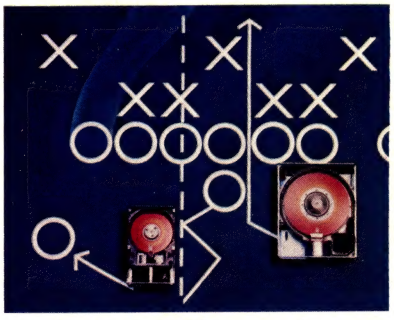


New graphics-controller ICs *coming to market provide increased resolution and faster processing in graphics-display systems. The improved devices exemplify the growing trend toward bit mapping (pg 61).*



EDN's first semicustom ICs actually work. *These gate arrays not only meet our initial design specifications, but their performance and economy clearly demonstrate the benefits of semicustom-IC use (pg 212).*

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On the cover: *OEMs must plan game-winning design strategies to be competitive in the market. High-capacity 5¼-in. Winchesters are going to help them score. See pg 132. (Photo courtesy Priam Inc; cover concept by Imagination)*

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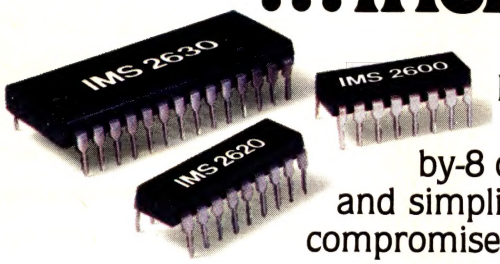
Standard-function ICs yield to custom circuits . . . Fine, ultrafine filters to reach $525M by 1988 . . . Packaged-software market to see tenfold increase.

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16K x 4 — The performance chip. With 100, 120, and 150ns access times, this organization makes a lot of sense in high-performance systems, such as high-resolution graphics, where high data rates are required. Packaged in plastic DIPs, the IMS2620 also gives you the right combination of cost, organization, and speed for microprocessor systems, terminals, and even arcade and home games. If you're upgrading from 16K x 1 chips, it provides a factor of four reduction in chip count. And its "$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$" refresh assist function minimizes required support circuitry for cost and space savings.

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16K x 4	100	160	IMS2620-10
	120	190	IMS2620-12
	150	240	IMS2620-15
64K x 1	100	160	IMS2600-10
	120	190	IMS2600-12
	150	230	IMS2600-15

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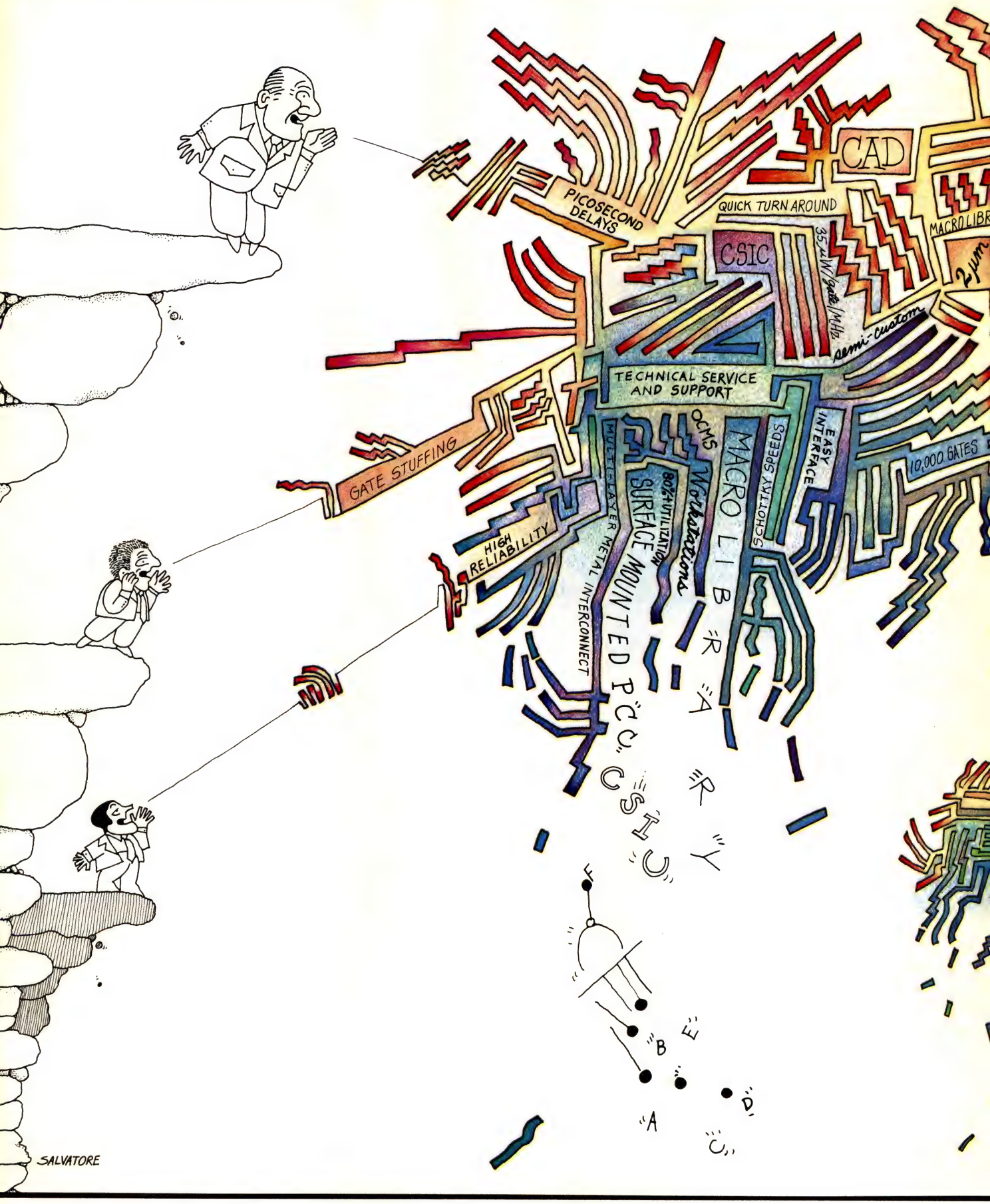
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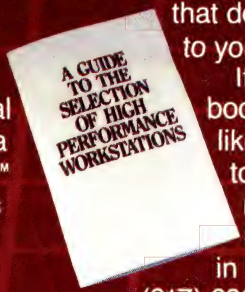
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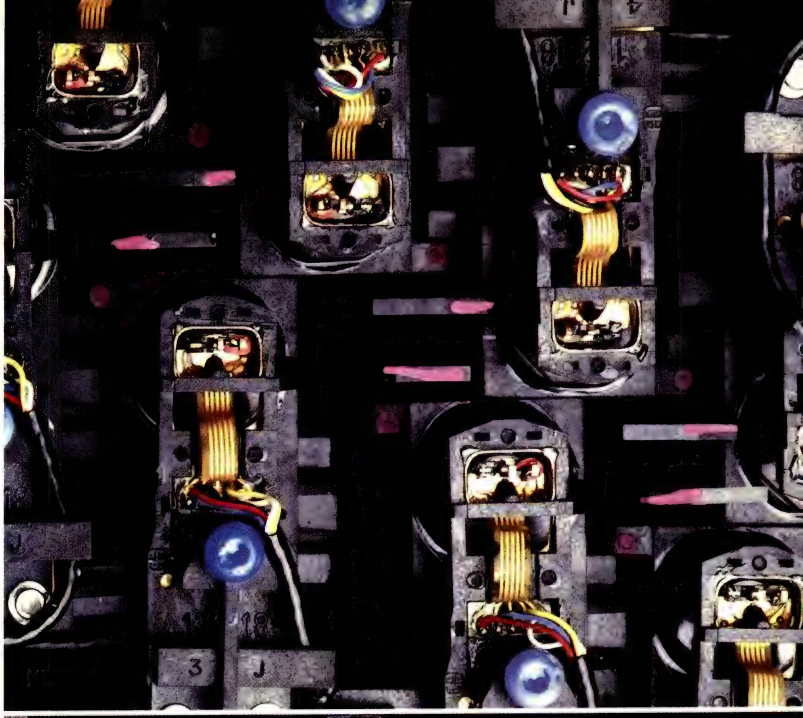
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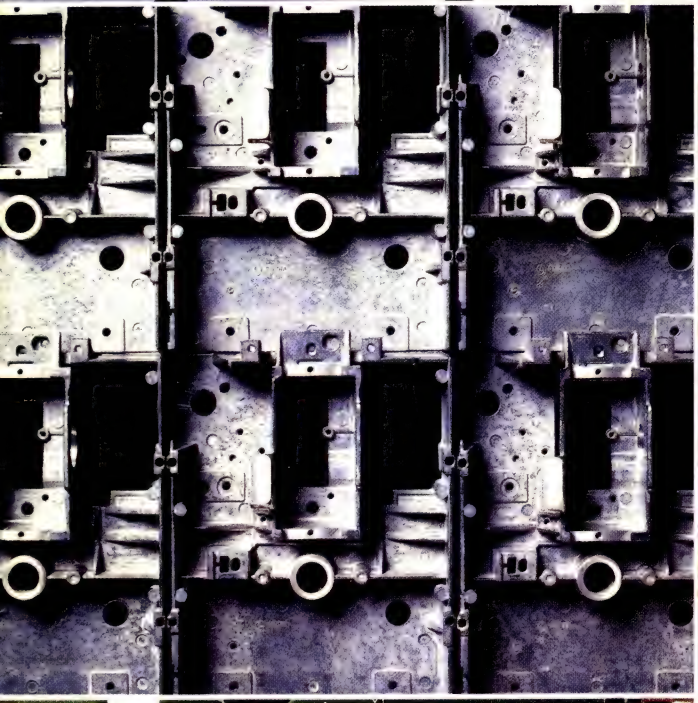
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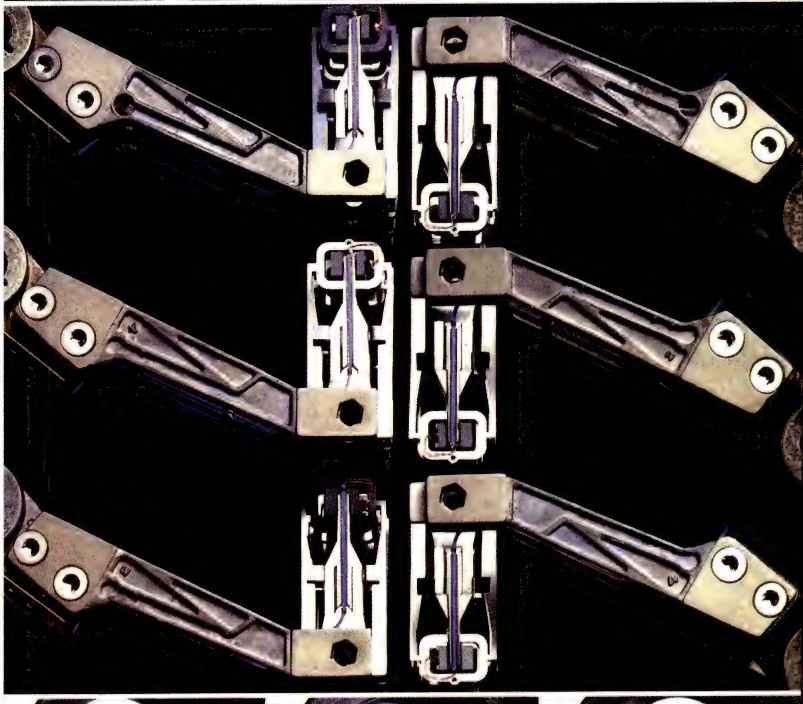
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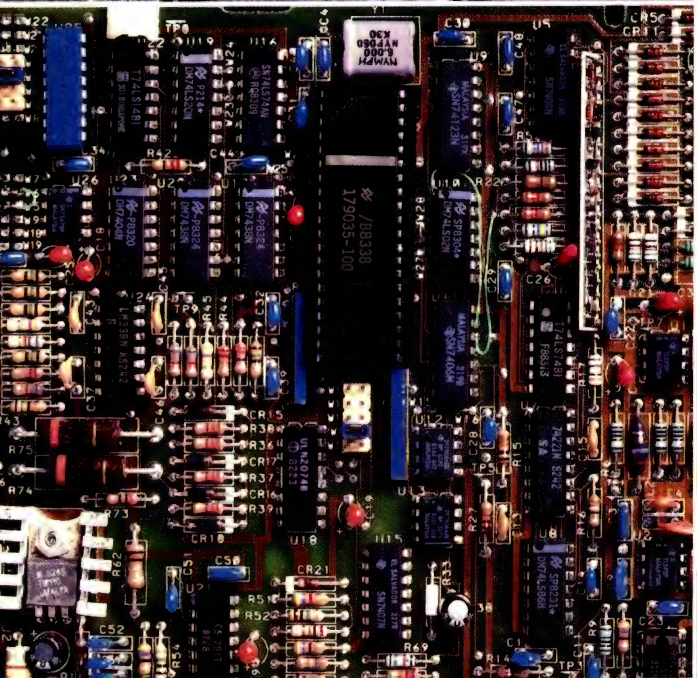
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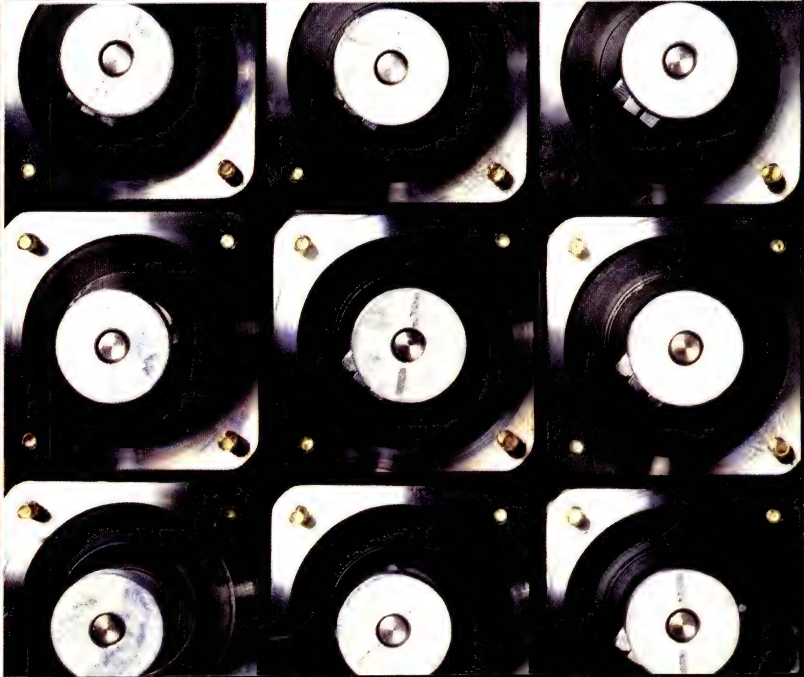












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CIRCLE NO 8

NEWS BREAKS

Edited by Joan Morrow

MULTIBUS CARDS PROVIDE SEGMENTED-PAGED VIRTUAL MEMORY

A set of Multibus cards from Virsys Technology Corp (Mt View, CA, (415) 965-8460) combines to create a microcomputer with a segmented-page virtual-memory system, such as that used in mainframe computers. The CPU card combines an NS16032 processor and NS16082 memory-management unit to support UNIX and applications such as interactive timesharing, CAD and database management. Model CPU1632 card also comes with a hardware floating-point processor and interrupt-control unit designed to minimize the software needed to handle priority interrupts. The CPU card costs $2750. Dual-port memory cards (the DMM1024 master memory and DMS1024 slave memory) each give the system 512k bytes of 150-nsec RAM. The master board costs $2750 and also provides the ECC and refresh logic; the slave board costs $1750.—Ed Teja

FORTH DEVELOPMENT SYSTEM WORKS FROM ROM/RAM INSTEAD OF DISK

National Semiconductor's (Santa Clara, CA) MA2301 FORTH system comes in the firm's Macrocomponent package. This stackable package—approximately the size of a tape cassette—allows you to assemble a complete diskless development system without any backplane. A complete system consists of the FORTH module (FORTH kernel in ROM), a CPU module and RAM modules; serial and parallel I/O modules for terminal and printer; and a power-supply module. The FORTH module runs ANSI-79 standard MVP FORTH, modified to obtain its screens from RAM instead of disk. You can develop code for Z80, 8080/85 or NSC800 μPs.—Charles H Small

100-MHz PORTABLE SCOPE CALCULATES DIFFERENTIAL MEASUREMENTS

With a built-in processor and a price (approximately $2500) that will probably be slightly less than its closest competing model from Tektronix, the Hitachi Denshi (Woodbury, NY) V-1100 100-MHz portable oscilloscope has on-screen displays from a built-in frequency counter and DVM. This feature allows the scope to print on its CRT differences in voltage and time between reference cursors. The on-screen display is handy: You can record the reading with a scope camera.—Charles H Small

PORTABLE COMPUTERS, PERIPHERALS, PRINTERS SHARE COMDEX LIMELIGHT

Several portable computers and some very quiet printers were among the most popular new products introduced or demonstrated at COMDEX/Spring, which was held last month in Atlanta, GA. Other interesting introductions included microfloppy-disk drives and an ST-506 hard-disk controller that provides cache memory for increased speed.

Three of the products were from Hewlett-Packard (Palo Alto, CA). The company's new LaserJet printer, based on technology used in the Canon LBP-CX personal copier, prints 8 pgs/min (more than 30 cps) and registers a noise level of less than 55 dB. The $3495 printer generates letter-quality characters or 300-dots/in. graphics. Microsoft (Bellevue, WA) announced its intention to supply versions of Word, its word-processing software, that will utilize the LaserJet's capabilities to print italics and other fonts along with regular text. A printer somewhat similar to the LaserJet, the Lasergrafix 800 Model I, was introduced by Quality Micro Systems (Mobile, AL) at a price of "less than $10,000." Also based on Canon's electrophotographic technology, the Lasergrafix emulates Diablo and Qume printers and Tektronix 4010/4014 display devices.

Along with the LaserJet, HP demonstrated its recently introduced ThinkJet printer ($495) and its portable computer ($2995), which features a 16-line × 80-column LCD screen and built-in 1-2-3 software from Lotus Corp (Cambridge, MA). Another computer vaguely resembling HP's portable unit, the 80C86-based Pivot from Morrow Inc (San Leandro, CA)

was also introduced at the show. It includes a built-in modem and a 5¼-in. floppy-disk drive in a 9-lb package. The PC-compatible machine will be available in August for less than $2500.

Indicative of the popularity of light-weight portables was the introduction by Panasonic (Secaucus, NJ) of six new microfloppy-disk drives. Of the six, three are 3-in. drives (the size previously chosen by Panasonic), while three use 3½-in. media. One of the 3-in. drives requires only a 5V supply and draws approximately 3W, suiting it to portable applications. The drives cost $125 to $200 (1000).

For nonportable, high-speed hard-disk applications, the $795 STDC controller from Cromemco (Mt View, CA) contains 64k bytes of on-board cache memory that speeds program execution from three to 10 times. The cache on the S-100 board, which was designed for use with the company's 68000-based systems and ST-506 disk drives, buffers four tracks of disk data and employs a least-recently-used algorithm to minimize disk accesses.—Gary Legg

MAJOR μP FIRM GOES OUTSIDE FOR DEVELOPMENT SUPPORT

NEC Electronics (Mt View, CA) isn't selling proprietary development systems for its μPs. Instead, the firm will depend on Tektronix (Beaverton, OR) for development stations and in-circuit emulators for the μPD7800 Series 8-bit (16-bit internal) single-chip μPs. Tektronix will supply a 6140 system, which includes an 8561 development station, an 8540 integration unit and a 4105 color-graphics terminal. NEC, like other makers of 8-bit microcontrollers, is rushing to fill the gap caused by 8051 shortages.—Charles H Small

MODEM MEETS 212A AND X.25 REQUIREMENTS

The WD212-X modem from Wolfdata Inc (Chelmsford, MA, (617) 250-1500) gives a personal computer a variety of synchronous and asynchronous communications capabilities: Bell 103, Bell 212A and CCITT X.25 LAPB. The synchronous X.25 packet-communication scheme lets the modem meet international standards and also adapts to let your computer talk to mainframe computers via such protocols as SNA and SDLC. Five on-board processors provide conventional features like autodial (both pulse and tone) and autoanswer, and they handle direct connection to telephone lines (including equalization). The modem comes as a single IBM PC-compatible board or as a stand-alone RS-232C peripheral.—Ed Teja

NEWSLETTER SUITS ENGINEERS USING PERSONAL COMPUTERS

Dedicated to serving engineers who use their personal computers for engineering work, *Personal Engineering & Instrumentation News,* (Box 983, Back Bay Annex, Boston, MA 02117) will feature updates on computer-aided-design tools, personal-computer-based data-acquisition systems and other topics. Focusing on personal-instrumentation systems, the newsletter will attempt to keep subscribers informed on news and technologies that could change the way engineers use personal computers.—Charles H Small

FLUKE INTRODUCES DIRECT VOLTAGE-MAINTENANCE PROGRAM

Built around the portable 732A dc-reference standard, Fluke's (Everett, WA) voltage-maintenance program will maintain traceability to the legal volt as set by the National Bureau of Standards. You can obtain the service in two basic ways, ranging in price from $250 to $500: Either Fluke will power up and certify your new 732A prior to shipment, or it will rent you one for certifying your own in-house voltage standards. The program is possible because the 732A is a solid-state unit and travels well—unlike chemical reference cells that loose their calibration.—Charles H Small



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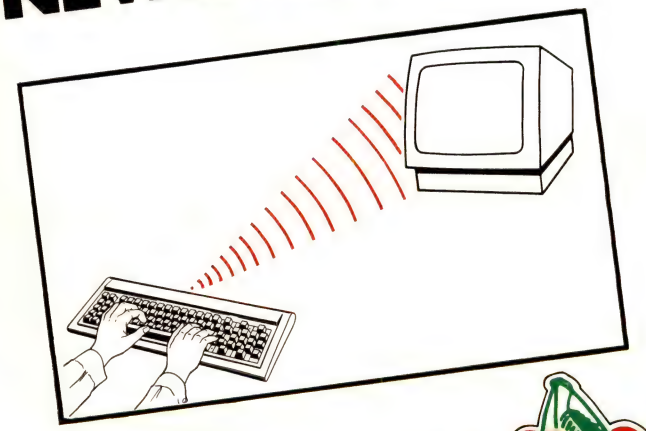
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CIRCLE NO 9

NEWS BREAKS: INTERNATIONAL

by Shelley Mumford

LOGIC-CIRCUIT SHORTAGE CREATES INCREASED PRODUCTION

Nippon Electric Co (NEC) and Matsushita Electronics Corp are increasing their production of logic circuits in response to a growing shortage of the parts. NEC plans to double production of its high-speed-CMOS standard-logic devices to about 2 million pieces per month by this fall. The firm also intends to expand its product line from 50 to 80 types of devices. The number of DIP models produced will grow from 17 million to 20 million pieces monthly; miniflat devices, from 1 million to 3 million parts.

Toward the end of the year, Matsushita will increase production from 7 million to 10 million pieces per month. Currently, the company offers 140 types of low-power Schottky TTL devices, several advanced LS TTL devices with 4-nsec speeds and 1-mW/gate power dissipation, and 117 CMOS-logic devices.

FIRMS BATTLE FOR LEAD IN 256k-DYNAMIC-RAM PRODUCTION

In an effort to overtake Nippon Electric Co (NEC) in 256k-dynamic-RAM production, Toshiba Corp plans to increase its product output from 100,000 to 1 million pieces per month by the end of this year. If Toshiba realizes its goal, the firm will be the first to achieve such an output for VLSI memories. NEC has similar plans, but its target date for 1-million-part production is scheduled for next spring. In response to its production plans, the company has recently completed a new VLSI plant and is currently constructing an assembly and inspection facility. Both are scheduled to be operational by July.

COMPANY SEEKS LARGER μP MARKET SHARE WITH THE 68000

Seeking to capitalize on the current shortage of 68000 μPs, Hitachi Ltd plans to more than double its monthly output from 20,000 to 50,000 pieces in the near future. The 16-bit-μP market is currently dominated by Intel Corp's 8086/8088 family, with a 70% share of the market. Hitachi hopes to gain part of Intel's share by making the 68000 more readily available to users.

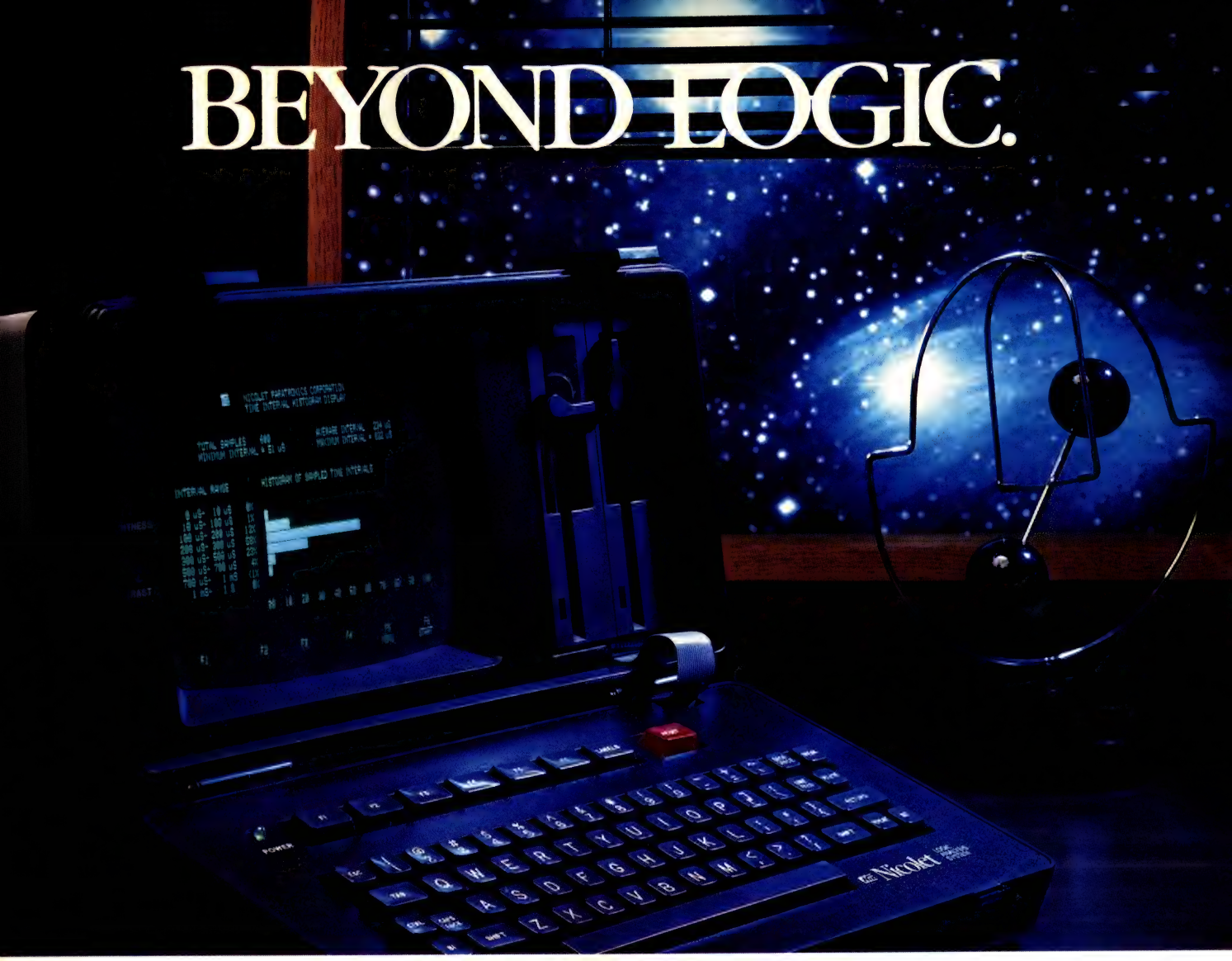
CACHE AUGMENTS BUBBLE MEMORY IN PROTOTYPE COMPUTER

Tokyo Agricultural and Industrial College has developed a prototype computer using bubble-domain memory for the main memory and a cache memory to speed access time. Specifically, the 2M-byte computer uses four 512k-byte bubble devices with a 13-msec average access time and 32k bytes of RAM with a 230-nsec max access time. The computer was produced in an attempt to use large-capacity bubble memories without sacrificing speed. Although bubble memories are already available in 4M-bit configurations (16 times as large as the 256k dynamic RAM), the bubble seriously lags behind in access time. Bubble memories, with access times of more than 10 msec typ, are considerably slower than the 100- to 300-nsec semiconductor memories.

GOVERNMENT ENDS TAX WRITE-OFF ON SEMICONDUCTOR EQUIPMENT

An amortization program that allows semiconductor manufacturers to write off their semiconductor-production equipment in five years instead of the usual seven will be terminated from fiscal 1985, according to the Japanese Finance Ministry. Japanese sources report that the Ministry sees no need to extend such preferential treatment to an industry that's become fully competitive. Moreover, the government feels that the additional ¥30 billion ($133 million) in tax revenues generated by the program's termination could help reduce mounting deficits in the national budget.

Japanese semiconductor producers are expected to protest the action strongly, claiming that the program's abrogation would blunt their competitive edge. It's also anticipated that



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CIRCLE NO 10

industry will demand an extension of the program, as well as a shortening of the write-off period to three years. Such a reduction is justified, the manufacturers contend, because the rapid advances in semiconductors have abbreviated the life span of production equipment.

SURVEY PREDICTS JAPANESE-PRODUCT SUPREMACY TO YEAR 2000

Japanese supremacy in products and productivity will continue well in to the early part of the 21st century, according to a recent survey by the Japan Economic Research Center. The study states that while the US might retain its lead in basic research, Japan will remain ahead in commercializing products. The Center claims Japan's edge is primarily caused by the US's inability to organize cooperative ventures between government and business. This is in sharp contrast with Japan, which has succeeded in its national efforts to develop new-generation computers and robots.

The survey claims that the US will even have difficulty keeping ahead in biotechnology, despite its R&D lead in that area. Unable to translate the biotechnology into actual products, the US will be surpassed by the Japanese within three to five years. The Center concedes, however, that Japan is seriously behind in the aerospace industry.

OPTICAL DISK COATING INCREASES MEMORY CAPACITY BY 30%

Ricoh Co has developed an optical disk coating that increases memory capacity by 30% compared with conventional disks coated with metallic material. Suitable for mass production, the material could also lead to at least a 60% reduction in production costs. The nonmetallic coating features low thermal conductivity, which permits reduction of the size of the information-recording pits. Conventional disks can accommodate pits no smaller than 0.9 μm, because the heat from the laser beam could distort the material. With the organic-pigment material, however, the pit size can be reduced to 0.7 μm. The coating can be applied under a normal atmospheric environment. Ricoh plans commercial introduction of the disks by 1986.

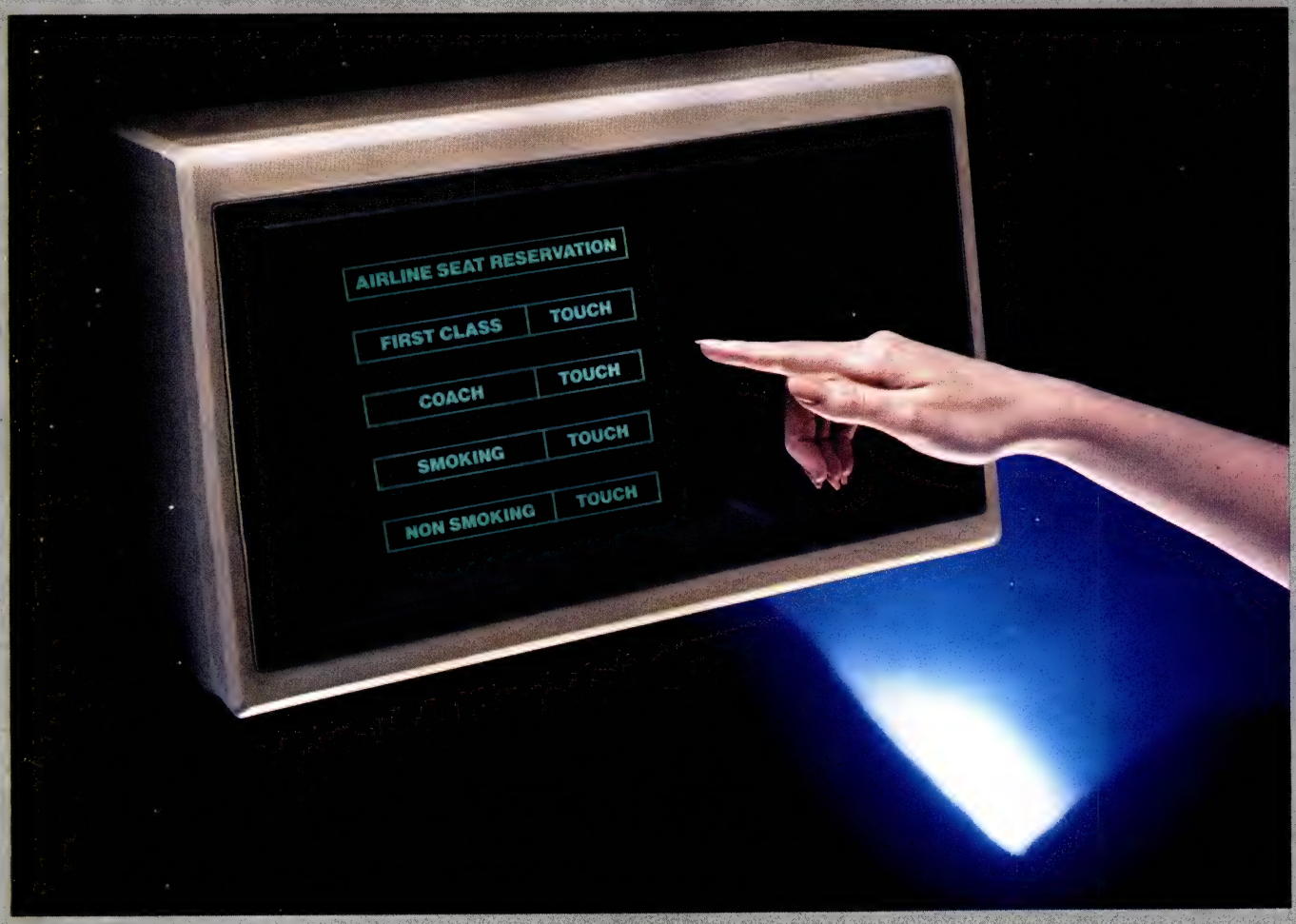
FIRMS EXPLORE BIOENGINEERING POSSIBILITIES

Japanese electronics firms are exploring the bioengineering field and the possible development of biochips and biocomputers. Sharp Corp, for example, plans to build a manufacturing facility for organic thin-film material as substrate material for microchips. Similarly, Matsushita Electric Industrial Co, Hitachi Ltd, Nippon Electric Co, Fujitsu Inc, Toshiba Corp and Sanyo Electric Co are also involved in the preliminary research of a new-generation chip, which might expand memory capacity 1000 times and processing speed 1 billion times over the most advanced silicon chips. The companies are experimenting with an organic film process developed by two General Electric Co scientists.

VIDEOTAPE RECORDER SUITS USE IN HIGH-DEFINITION TV

Nippon Hoso Kyokai (NHK), Japan's public broadcasting station, has developed a home videotape recorder (VTR) designed for high-definition television receivers. High-definition receivers feature more than 1000 scanning lines (compared with 525 lines for conventional TVs), which results in superior picture quality. Because the high-definition receiver's signal volume is five times greater than that on conventional TVs, the ½-in. tapes used in typical home VTRs are too narrow to record the more advanced image formation. Consequently, NHK devised a signal-compression method, which divides a picture frame into quarters and assembles them into a complete picture at the receiving end. Metal tape is used to allow high-density recording. Japanese industry regards NHK's development as a major gain in the global race to determine a high-definition-TV standard. The US has proposed a 1050-line system; the Europeans, a 1250-line system.

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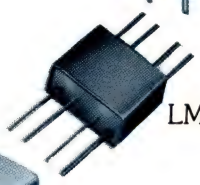


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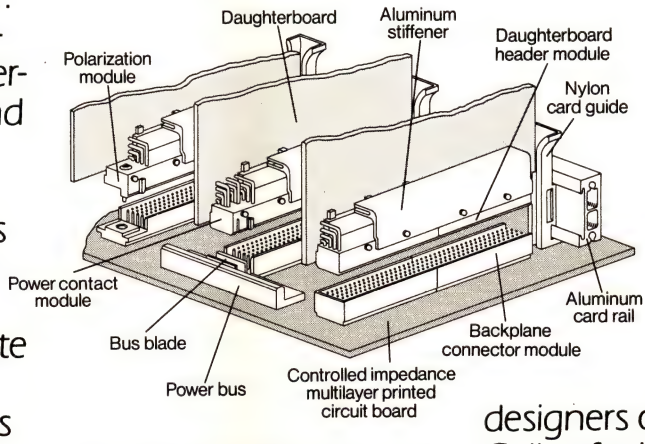
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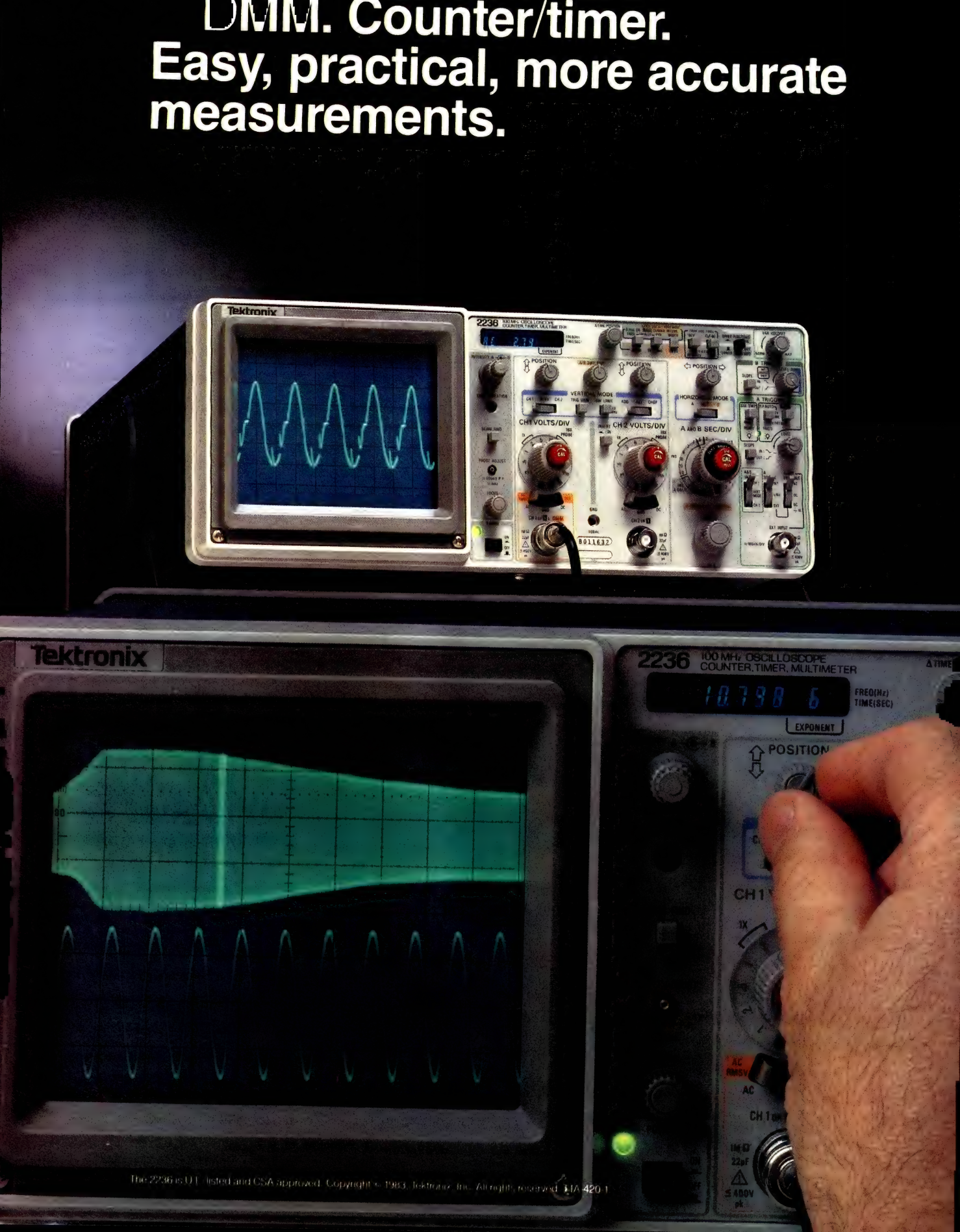
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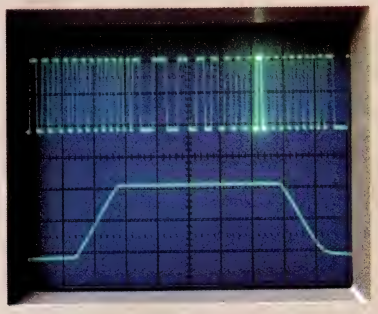
Practicality is the cornerstone of the 2236. The 2236's intensified on-screen markers make gated counter measurements easy, with no mental arithmetic required. And the 2236 offers an independent floating 5000 count auto-ranging multimeter with side inputs for DC voltage measurements to 0.1%. An auto-ranging ohmeter provides resistance measurements ranging from 0.01Ω to GΩ—as well as audible continuity. Operator prompts, auto-ranging and audible, automatic diode/junction detection features serve to simplify set-up and enhance confidence in your measurements.

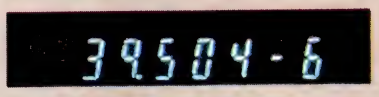
You can obtain scope, counter and DMM input simultaneously through a single probe. The same probe is used to provide input for the 2236 CRT display and the digital measurement system resulting in easy set-up, greater measurement confidence and reduced circuit loading. You can make direct digital measurement of dc volts and ac coupled true RMS volts through the Ch 1 input.

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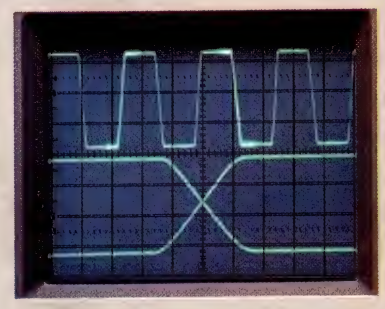
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Gated width measurement. Pulse of interest is selected with the intensified zone. Both width and period measurements are made with up to 10 ps resolution.





Delta time measurement. Time between two intensified zones on the A sweep is measured with up to 50 ps accuracy.

Left top: Ch 1 true RMS & DC volts measurements. Made easily at the probe tip. (The 2236 adjusts automatically to 1X or 10X probes.) The 2236 includes relative reference capability for subtracting offsets.

Left bottom: Gated frequency measurement. Intensified zone brackets the period of interest by means of the delayed sweep, allowing easy frequency measurement on any specified portion of the waveform.

Tektronix

SIGNALS & NOISE

FFT program corrections

Dear Editor:

As you might guess, in spite of my supposedly thorough testing, readers have found two errors in the programs contained in my FFT series of articles (EDN, March 8, pg 209, and April 5, pg 237).

The first error is on pg 213 of the March 8 issue in **Fig 2,** line 8626. The term "C(ID)" should be "C(IZ)." Because this term has no effect except in analyzing bandstop filters where C(IZ) might not be zero, I didn't catch the error.

The second error occurs in the April 5 issue on pg 238, **Fig 1,** lines 7000 through 7110. This is a printout routine that's never accessed by the program. I deleted the menu reference to the routine when I decided that a printout feature wasn't needed, but I neglected to take out the routine itself. Readers can either eliminate the routine or include a menu reference and an "IF...GOTO" line in the menu section of the program.

Incidentally, I've been receiving calls with questions about the programs. So far they are running not only on Apple systems but on an IBM Personal Computer, an HP-86 and an HP-9825.

Sincerely,
R F Cobb
Senior Scientist
Harris Corp
Melbourne, FL

Play it again

Dear Editor:

I read with interest the exchange between David D Collins and William R Scharrenberg (Signals and Noise, March 8, pg 24) regarding the choice of a name for floating-gate MOS memory devices that are not designed to be erased. Both gentlemen have valid points. Mr Scharrenberg points out the desirability of leaving the "E" in EPROM to denote that the technology is that of the EPROM. Mr Collins, however, recoils at the use of an "E" (for "erasable") to stand for a nonerasable device.

I propose the term "NEPROM," for "nonerasable PROM." The connotation of EPROM technology is retained, and the fact that the device is not erasable is clear. (Of course, it can be argued that a fuse-link PROM is not erasable as well. But you can't have everything.)

It has always struck me as curious that ROMs, which are randomly accessible memories, can also be considered as RAMs. Insofar as it's possible, terminology should be chosen that not only accurately describes devices but also discriminates against unintended interpretations. Perhaps we in the industry should take one more look

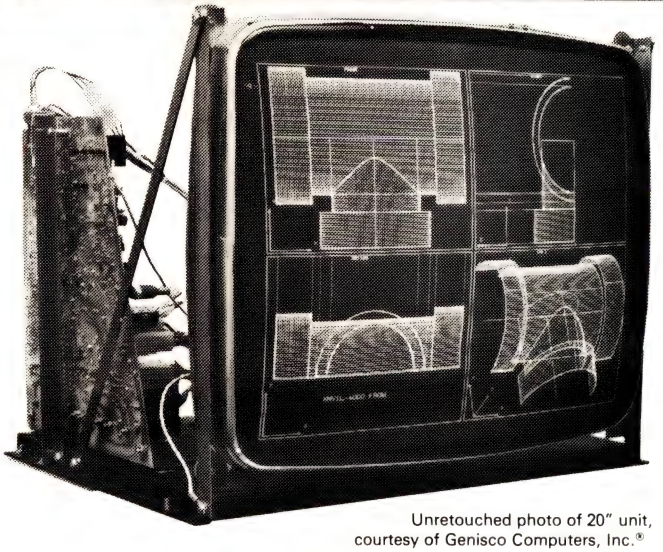
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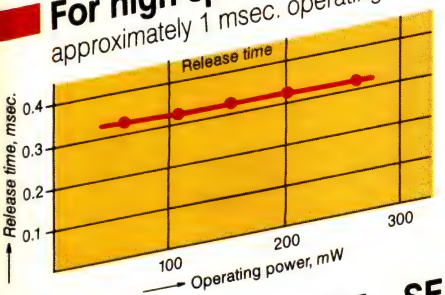
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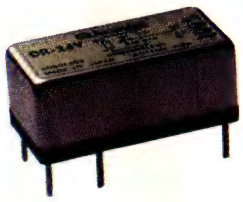
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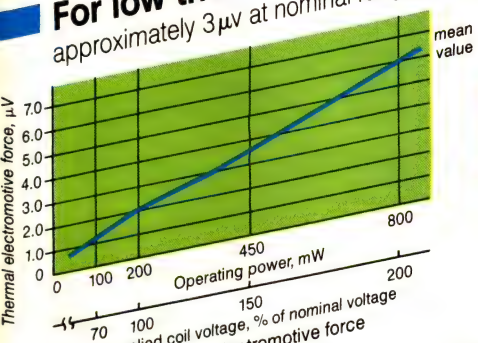


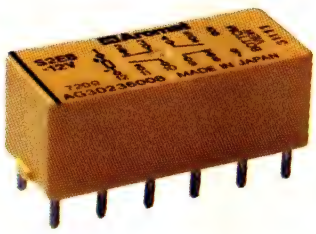


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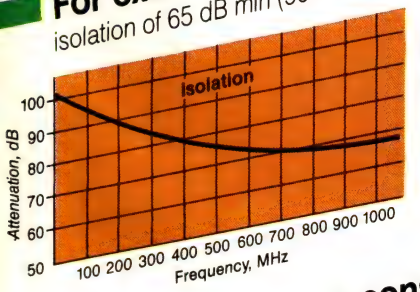
approximately 3μv at nominal range.

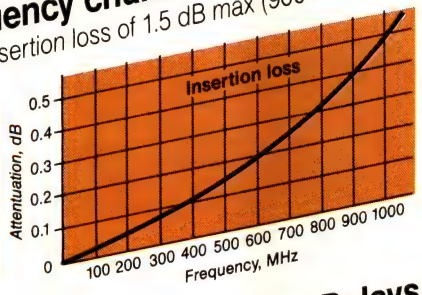


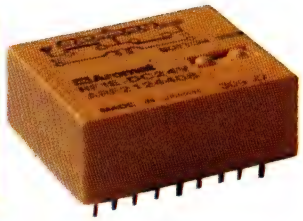


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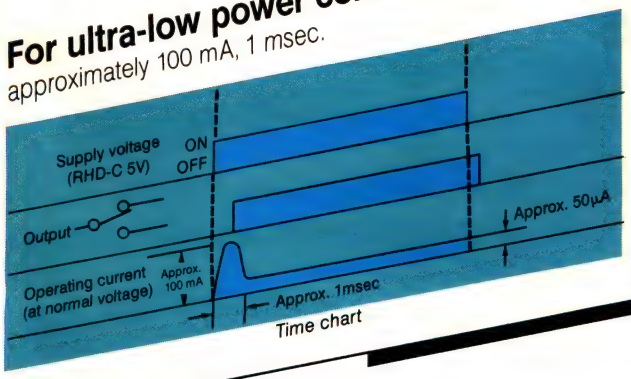






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CIRCLE NO 16

at what we are going to call nonerasable, floating-gate MOS memory devices. It looks like they will be with us for some time.

Sincerely,
Ted Yellman
Engineering Assurance Manager
Data I/O
Redmond, WA

VME Bus Design Idea

Dear Editor:

We would like to point out a few shortcomings in the Design Idea "FPLA forms VME Bus interrupter" (EDN, December 22, 1983, pg 270).

- The block diagram (**a**) implies that more than one load is connected to the AS* line. This is likely to violate the dc loading specifications of the VME Bus specification, revision B, section 7.5.1.
- IACK* is also overloaded with respect to the specification. The peripheral device circuitry will require a further connection to IACK* to distinguish between slave and interrupter operation as indicated by VME Bus specification, revision B, section 2.4.1.
- There is no hysteresis on the AS* input as required by VME Bus specification, revision B, 7.5.1.
- A standard PAL16R4 has a maximum propagation delay of 35 nsec over the commercial operating range. The VME Bus specification, revision B, section 4.5, table 4.3, entry 17 requires that the IACKOUT* line goes high within 30 nsec of AS* going high. A faster PAL16R4 would help but it is necessary to include the delay of the necessary buffer with hysteresis.

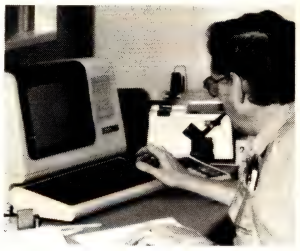
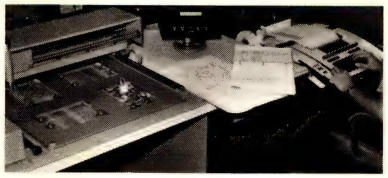
The VME Bus specification is often violated, usually unintentionally. For the convenience of those users, we urge those involved in designing VME Bus products to spend time implementing the specification fully.

Sincerely,
Karl Wood
Walter Scheepens
Philips Research Laboratories
Solid State Electronics Div
Surrey, England

Storage-scope maker

In the Special Report on storage oscilloscopes (EDN, April 5, 1984, pg 154), Norland Corp was listed in the table of digital-storage-scope specs but not in the manufacturers list on pg 166. You can contact the company at:

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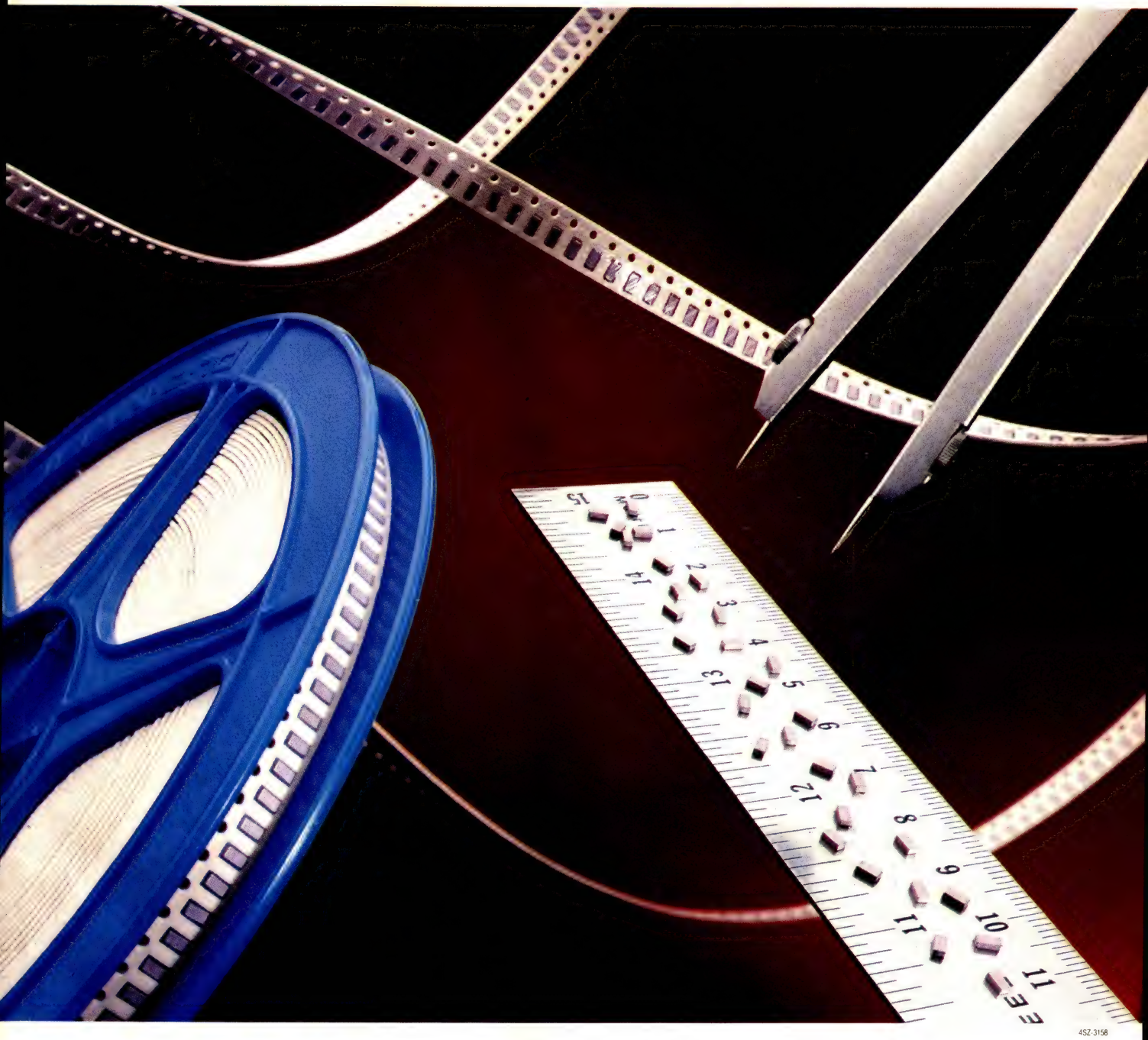
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Texas Instruments and Data General push supermini performance to new heights.

- **TI's Advanced Schottky Family** includes the industry's highest speed TTL logic, which helps double throughput of new DG state-of-the-art-designed superminicomputer (*Page 2*).
- **Performance Budgeting** options—available only with TI's Advanced Schottky Family of ALS/AS devices—optimize your system speed/power product (*Page 3*).
- **Having over 240 functions today with more to come,** TI's rapidly growing ALS/AS Family maximizes your design options in high-performance TTL logic (*Page 4*).▶

TI's high-supermini

When it came time to design a virtual-memory 32-bit superminicomputer unmatched for performance, Data General logically turned to Texas Instruments for semiconductor logic. And TI came through.

By designing-in high-speed AS logic functions from TI's Advanced Schottky Family, Data General was able to introduce its new ECLIPSE MV/10000™ superminicomputer a year ahead of the industry. And achieve a blazing machine cycle time of 140 ns.

Speed increases from 45 ns to 32 ns

The TI 'AS881, a 4-bit arithmetic logic unit/function generator, got the MV/10000 off to a flying start. Far faster than standard Schottky, it reduced the delay time of a 32-bit ADD operation from 45 ns to 32 ns. Plus, its 24-pin, 300-mil-wide package required 50% less board space.

TI's high-speed 'AS882, a 32-bit look-ahead carry generator, also proved crucial to the supermini's state-of-the-art design. It integrates a 32-bit look ahead on a single chip.

Strong support speeds supermini to market

From an initial presentation . . . to meeting specs . . . to producing devices . . . to testing . . . to on-time delivery, TI gave Data General its full support and cooperation.

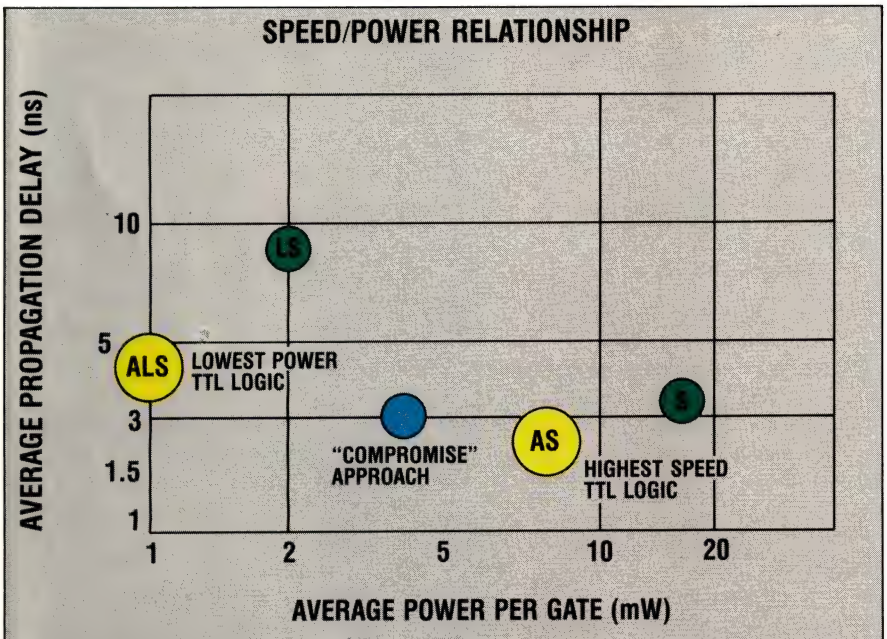
All of which helped Data General get its new supermini to market a year early.

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◀ **For maximum speed,** DG's new ECLIPSE MV/10000 32-bit superminicomputer incorporates 51 TI high-speed AS logic devices—46 'AS881s and five 'AS882s. A versatile, high-performance computer system, the MV/10000 can be used on a wide variety of design projects. Cover example: Development of plans for a skyscraper involving simulation of various physical forces on the structure.

speed AS logic speeds DG's off the drawing board...at 140 ns!



Performance Budgeting—specifying Advanced Schottky Family ALS and AS devices on a socket-by-socket basis for optimum combination of speed and power—allows designers to achieve outstanding performance levels in a wide range of state-of-the-art system designs.

Performance Budgeting: The key to optimizing system speed/power product.

Why compromise your design with too little TTL speed? Or too much power? Instead, get the highest speed and lowest power with TI's Advanced Schottky Family of ALS/AS devices. Put TI's Performance Budgeting to work for you.

Performance Budgeting means you can place AS devices in the critical speed paths to take advantage of their fastest speeds, while spotting ALS devices where you can make the most of their lowest power.

By specifying socket by socket, you can achieve the optimum combination of system speed, power, and economy.

AS functions: World's highest speed TTL

When speed is your top TTL priority, TI's AS logic is your best choice. With a typical 1.7-ns gate delay and only 8-mW power dissipation per gate, AS logic is faster than a compromise approach to TTL (see above and at right). And TI offers you a wide choice of AS logic devices.

In addition to the high-speed 'AS881 and 'AS882 devices used by Data General, there are also the following new, very fast, 8-bit, byte-oriented ICs:

'AS870/'AS871 register files contain internally multiplexed, dual, 16-word by 4-bit data sources for direct ALU input. Plus, multiplexed I/O ports minimize processor data-path access times to memory and system bus structures.

The 'AS877 octal transceiver provides both parallel and serial ports for system interconnection. Its integral serial data port simplifies fault detection and reduces system debugging.

'AS867/'AS869 octal bidirectional counters are fully paralleled, high-performance, presettable 8-bit counters that minimize next-address generation compromises. Both asynchronous and synchronous clear versions are offered.

Many more AS logic devices available from your TI distributor are listed on the next page.

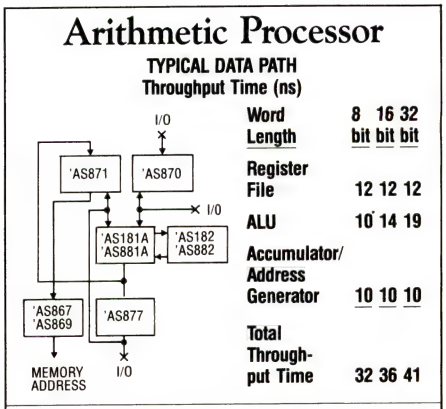
ALS functions: Lowest power TTL

Is low power your key TTL requirement? Then TI's ALS devices are your best solution. They give you absolutely the lowest power—1.2-mW gate power dissipation—plus very respectable speed at 4-ns gate delay, typically. ALS logic typically requires 68% less power than a compromise-logic approach, with only 25% less speed.

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See back page for more information.

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74ALS21
74ALS22A
74ALS27
74ALS28A
74ALS30
74ALS32
74ALS33A
74ALS37A
74ALS38A
74ALS40A
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37401BCB	54ALS08
37402BCB	54ALS11
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Please send me more information on TI's Advanced Schottky Family of ALS/AS devices.

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  16K DRAM, 4K SRAM, HKE 80 8-bit Microprocessor compatible to Z80

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CIRCLE NO 20

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In just 60 DASA a

TI's conductive-rubber keyboard provided DASA with a cost-effective, custom keyboard with a quality look and feel.

The schedule was "near impossible." The specifications tough. And Texas Instruments came through. Working from a DASA concept, TI produced a complete, custom conductive-rubber keyboard for DASA's advanced Directory Dialer™ in just two months.

A custom keyboard at the right price

TI's versatile conductive-rubber keyboard gave DASA precisely what it wanted for its new Directory Dialer. It provided a rich look. Pleasing tactile response. Custom key sizes and layout. All at a very reasonable price.

Just as important, TI is an established, reliable keyboard manufacturer. Having designed and built more than 150 million keyboards since 1971, TI had both the experience and proven manufacturing capability DASA could depend on. From initial design discussions . . . to a fully assembled custom keyboard.

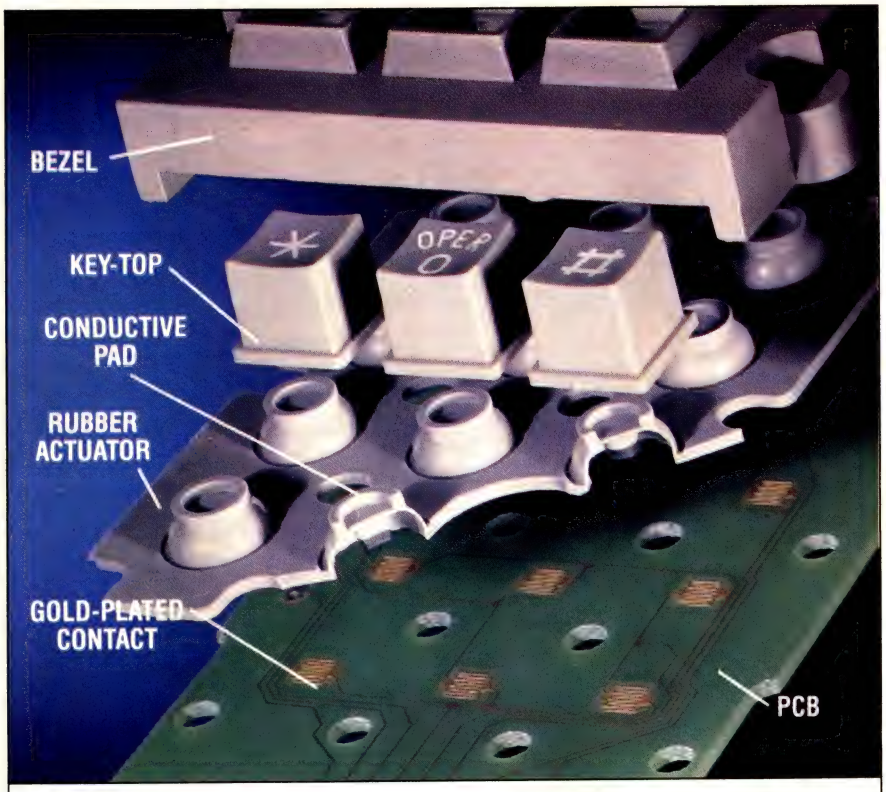
And, because TI is a domestic supplier, DASA had quick and easy access to TI engineers. By working closely with TI, DASA was able in effect to add TI's design engineers to its own design staff. All of which helped speed the DASA Directory Dialer to market.

Today, DASA's design consultant is working with yet another TI keyboard for a new portable repertory dialer.

◀ **At the touch of a key,** the new DASA Directory Dialer can automatically retrieve and dial any number from a directory of 400 names, saving time and effort. TI's custom conductive-rubber keyboard provides the elegant look, rich tactile response, and economy DASA requires.

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days, Texas Instruments made custom keyboard ready for business.



Complete and fully assembled, TI's custom conductive-rubber keyboard includes key-top, bezel, rubber actuator, and substrate.

Give TI a sketch, and we'll give you a keyboard.

It's really just that simple. Once you give TI a concept, we can design and produce a fully assembled, low-cost conductive-rubber keyboard that precisely meets your needs.

Highly flexible, TI's versatile keyboard technology gives you a host of design options. You can choose from a complete range of keystroke/travel. Actuation force from 0.5 to 7.0 oz. Tactile response from firm to soft. Key size and location. And a variety of key-top styles.

Whatever technical assistance you need, you'll also find at TI. Our design engineers are equipped to work closely with you from concept . . . to prototype . . . to finished keyboards.

A reliable domestic keyboard supplier

TI, in fact, offers you a unique combination of advantages unmatched in the industry.

With TI, you get far more than an exceptional custom keyboard. You get the full support of a domestic, vertically integrated keyboard manufacturer.

This works to your advantage in a number of ways.

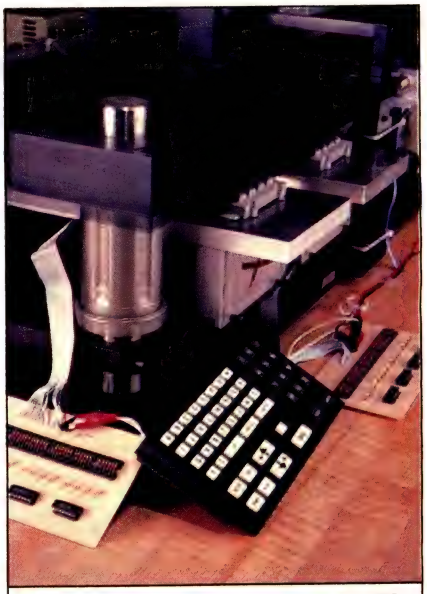
First, you're assured a reliable supply of keyboards from a source near you. This greatly simplifies and speeds keyboard design and delivery. Plus it gives you ready access to TI.

Second, you get a higher quality, more reliable, low-cost keyboard through TI's extensive vertical integration. That's because keyboard components are manufactured, assembled, and tested at TI.

Third, you're dealing with keyboard experts. TI has designed keyboards for virtually any kind of electronic product you can think of. And then some.

So whether your specialty is telecommunications, data processing, instrumentation, or anything else that requires a custom keyboard, you can rely on TI.

For more information on TI keyboards, call (617) 699-5242. Or write Texas Instruments Incorporated, Dept. MSM923ED, P.O. Box 402250, Dallas, TX 75240.



Based on demanding life-cycle tests, TI's durable conductive-rubber keyboard can operate reliably up to 10 million cycles.

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"My father always says 'If you're so smart, give them the part'. That's why we give out over 20 free sample chokes and transformers every day."

Bruce Rensing



"My father's theory is simple: If your products are *really* first rate, they'll talk for themselves a lot better than you can talk for them.

"He started operating on that theory the day he started the business, back in 1955. As soon as somebody contacted him expressing an interest in a part, he'd look to see if he had a standard item with the required specs. If he did, he'd send out a sample the same day. If he didn't, he'd get to work making a sample, and send it out as soon as it was ready — usually about 10 days.

"Well, we're still working the same way. The only differences are that instead of the two or three standard lines my father had in the beginning, we have 15, with over 1,400 values. And we now have a Sample Department that takes care of the non-standard items, and can get the sample out in less than 10 days — sometimes as little as two or three.

"And we're more confident than ever that our products will sell themselves. We've had 29 years of experience added to all the expertise my father had when he started the business. And we've stayed strictly within our specialty, and became probably the leading firm exclusively in the business of making coil-wound products.

"We'd like to send you a free sample. Just dial the Hotline number below and give us your requirements. Or write for our full line catalog. We design and manufacture in the U.S.A., and ship world wide. Thank you."

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CIRCLE NO 21

CALENDAR

CAD/CAM and Robotics, Toronto, Canada. SME, 1 SME Dr, Box 930, Dearborn, MI 48128. (313) 271-0023. June 19 to 21.

International Symposium on Fault-Tolerant Computing, Hyatt Orlando, Orlando, FL. Richard Sedmark, Sperry Univac, Box 500, MS C1SW12, Blue Bell, PA 19404. (215) 542-3638. June 20 to 22.

Computer Showcase Expo, Boston, MA. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 21 to 24.

Computer Showcase Expo, Minneapolis, MN. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 21 to 24.

Design Automation Conference, Albuquerque Convention Center, Albuquerque, NM. Harry Hayman, Box 639, Silver Spring, MD 20901. (301) 589-8142. June 24 to 27.

PC Expo, New York Coliseum, New York, NY. Ralph Ianuzzi Jr, PC Expo, 333 Sylvan Ave, Englewood Cliffs, NJ 07632. (201) 569-8542. June 26 to 28.

Computer Showcase Expo, Milwaukee, WI. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 28 to July 1.

Networks '84, London, England. Online Conferences Ltd, Pinner Green House, Ash Hill Dr, Pinner HA5 2AE, Middlesex, UK. 01-868-4466. July 3 to 5.

NCC '84, Las Vegas Convention Center, Las Vegas, NV. Anne-Marie Bartels, (703) 558-3613. July 9 to 12.

SIGGRAPH, Minneapolis, MN. Cynthia Stark, Association for Computing Machinery. (312) 644-6610. July 23 to 27.

NEWSLINE

SGS product expansion headed by top-performance LS404 quad op amp.

An expanded product line that includes one of the industry's widest package selections, increased production capability and aggressive pricing are enabling SGS to make major inroads in the op amp market. One of the most notable developments in the expanded line is the LS404 quad op amp. The LS404 combines SGS-developed bipolar technology and linear design with a proprietary low noise process. An important feature of this device is the patented input stage which remains in the active region even with signals more negative than the substrate. This makes the LS404 particularly versatile in single supply applications, and useful, too, in industrial control circuits. Standard DIP and SO-package versions are available. The new expanded line also includes a dual op amp (LS204) as well as the complete family "LM" and "MC" types of op amps and comparators. Due to SGS' recent investment in fully automated assembly lines, all op amps and comparators are available at significant price breaks with increased reliability.

PERFORMANCE COMPARISON: LS404 vs. COMPETITIVE TYPES

	LS404	RM4156	SE5532A (High Cost)	TL084	LM324 (Low Cost)
QUALITY FACTOR $\frac{BW}{I_S}$	9	3.1	2.5	2.1	2.1
MAX INPUT NOISE VOLTAGE ($nV/\sqrt{Hz}$) R_g = 10kΩ	15	14	6	25	—
HARMONIC DISTORTION (%)	0.04% max @ 1kHz 0.03% typ @ 20kHz	Not Specified	Not Specified	Not Specified	Not Specified
GROUND COMPATIBILITY OF INPUTS	−0.5V (protected against inversion)	$2V_{BE}$	$V_{BC} + V_{CESAT}$	$2V_{BE}$	−0.3V
CURRENT CONSUMPTION I_S (mA)	1.3	4.5	8	5.6	1.5

Single-chip L296 IC switching regulator delivers 160 watts.

SGS ion implanted technology has resulted in the development of a monolithic linear IC that houses all circuitry necessary to build a complete switchmode power supply. The L296's combination of power, performance and space-saving capabilities is already leading to greater cost efficiency in a wide range of applications. The device has a minimum of external components and features an output power stage which can deliver 160W at up to 100kHz. Operating as a step-down switching regulator, the L296 employs pulse width modulation to provide regulated voltages from 5.1V to 40V. All essential control circuitry is integrated in the chip: soft-start, internal precision reference, output overvoltage sensing and a reset signal for a microprocessor.

Dual power op amp unequalled at 1A output current.

A dual operational amplifier/power booster now available from SGS is capable of delivering up to 1A of output current. This figure is unequalled by competitive monolithic power op amps. In addition, the L272 linear IC operates at voltages as low as 4V and as high as 28V. The high-grain, high-power features of the device make it suitable for a variety of applications. For example, the L272 can be used with motor servos, voice coils and in valve actuation configurations. Other performance advantages include full thermal shutdown protection, low saturation characteristics (1V/0.5A), true differential inputs and single or dual supply. The L272 is available in 16-lead powerdip or 8-lead minidip packaging.

Low power, high speed digital designs replace LSTTL logic.

With over 100 new silicon gate fast CMOS functions currently available, SGS is helping to accelerate the jump from LSTTL logic to fast CMOS. The SGS product line offers pin-for-pin compatibility with standard LSTTL, while providing wider supply voltage usage, higher clock frequencies, better noise immunity, and less power consumption. SGS fast CMOS devices feature typical working clock frequencies of up to 60MHz, a power supply range from 2V to 6V, output drive current to 5mA (4mA to 85°C for standard gate, 400mV thresholds and an operating temperature range from −40°C to + 85°C. Typical quiescent power consumption is only 0.01W. In order to remain at the forefront of this new technology, SGS will substantially expand its family of fast CMOS products during 1984.

For more information on the above products, call SGS at 602/867-6100 or write: SGS, 1000 East Bell Road, Phoenix, Arizona 85022.

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CIRCLE NO 22

Bliley



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CIRCLE NO 24

CALENDAR

Summer Computer Simulation Conference, Copley Plaza Hotel, Boston, MA. The Society for Computer Simulation, Box 2228, La Jolla, CA 92038. July 23 to 27.

International Conference on Luminescence '84, University of Wisconsin, Madison, WI. Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. (202) 223-8130. August 13 to 17.

Basic IC Technology, Sunnyvale, CA. Pat Fruscello, ICE, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. August 21.

International Conference on Parallel Processing, Shanty Creek Lodge, Bellaire, MI. Dr Feng, (614) 422-1408. August 21 to 24.

Basic IC Technology, Minneapolis, MN. Pat Fruscello, ICE, 15022 N 75th St, Scottsdale, AZ 85260. (602) 998-9780. August 28.

National Software Show/West, Anaheim, CA. Raging Bear Productions, 21 Tamal Vista Dr, Suite 175, Cortemadera, CA 94925. September 5 to 7.

International Conference on Optical Fiber Sensors, Stuttgart, Germany. Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. (202) 223-8130. September 6 to 7.

Electronics and Aerospace Systems Conference '84, Shoreham Hotel, Washington, DC. Dr James Babcock, IRT Corp, 6800 Poplar Pl, McLean, VA 22101. (703) 893-2111. September 10 to 12.

MIDCON '84, Dallas, TX. Jerry Fossler, Electronic Conventions Inc, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. September 11 to 13.



WE'VE BEEN DELIVERING 3½" WINCHESTER DISK DRIVES FOR OVER A YEAR.

Rodime has been setting a new standard in Winchester disk drive storage for more than a year. Its 3½" drive with 5 and 10 megabytes of formatted storage has become the industry leader for sub 4" Winchester disk drives. Rodime has now delivered tens of thousands!

The proven compact drive and proven quantity supplier

With thousands of its 3½" Winchester drives in operation today Rodime has further demonstrated its reputation for reliability, a major design consideration for our 3½" drive, and quality. It has a rugged design with high resistance to shock, an important consideration for portability and for vibration prone environments. Using advanced large-scale integration, the entire electronics for the drive are on a single compact board and there are no adjustments or select-on-test components.

New design horizons

The compact size of Rodime's drive suddenly puts large-scale storage into areas never considered before. The 350 series is one-fourth the volume of a 5¼" Winchester drive. And the 250 series, which includes



mounting brackets and a face plate, fits into the same space as a half-height 5¼" Winchester offering even further shock and vibration isolation. Now, system designers have a new level of flexibility. One area that has received attention is use with portable computers. Several major portable computer manufacturers have already incorporated Rodime 3½" Winchester disk drives into their products. There are other equally exciting areas such as desk top computer systems, intelligent terminals, point-of-sale terminals, industrial controllers, telecommunications systems, navigation and guidance systems, and portable instrumentation. In fact, the list of potential uses is only limited by the imagination of the system designer.

A tradition of excellence

In a few short years, Rodime has established itself as a major force within the Winchester disk drive industry. Rodime is one of the few manufacturers that are delivering 5¼" Winchester drives with a broad range of capabilities up to 54 megabytes. And is the only manufacturer delivering high-performance 3½" Winchester drives in production quantities.

For the compact 3½" Winchester disk or other 5¼" Winchester requirements, look to Rodime. Rodime delivers.

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KONTRON ELECTRONICS



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KDS comes complete with all the applications software you need. Editors, linkers and assemblers are provided for assembly language programming and for use with Pascal compilers. Software developed on other Kontron systems can be ported to the KDS via an RS-232 link. Industry-standard operating systems* make KDS even more versatile, opening the door to third party software and many new applications. Find out how much more the KDS Multifunction Development System can do for you. Write for a demonstration.

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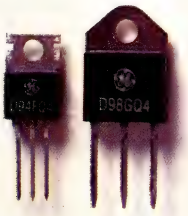
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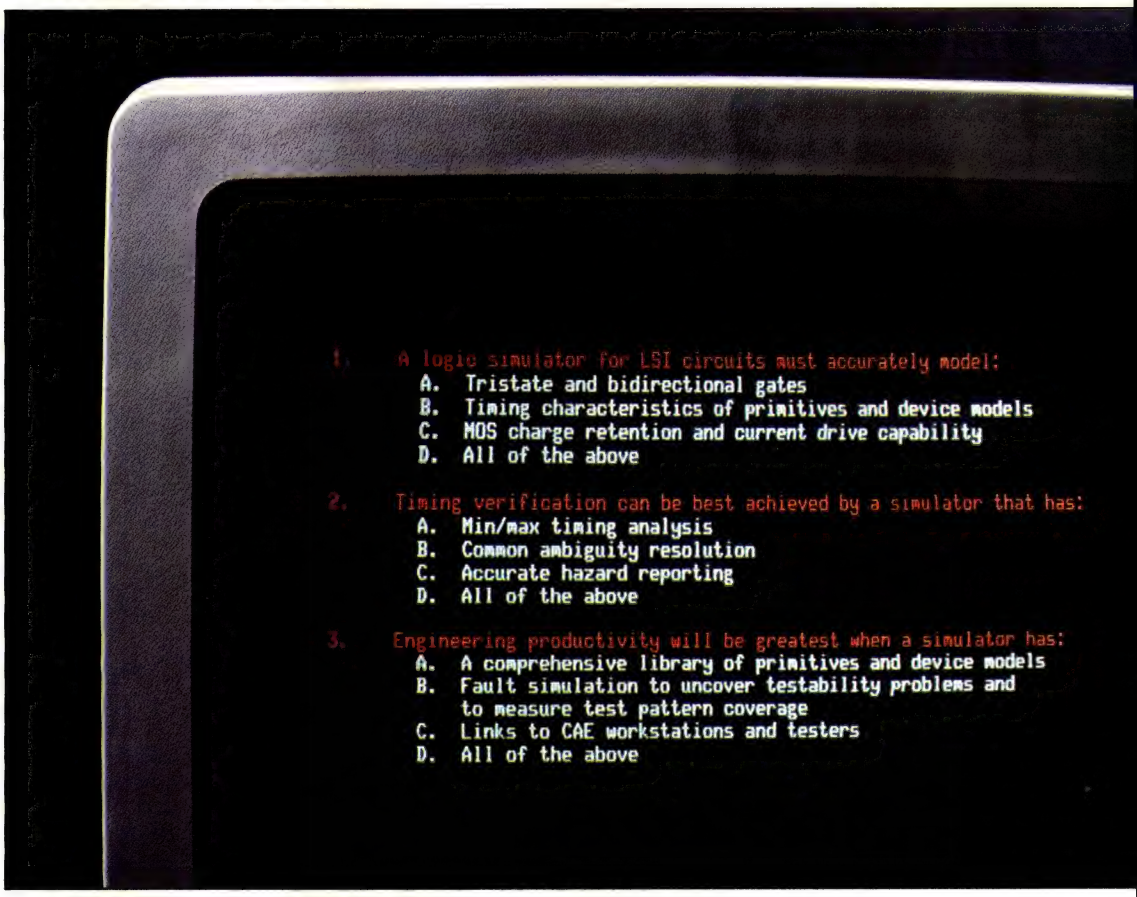
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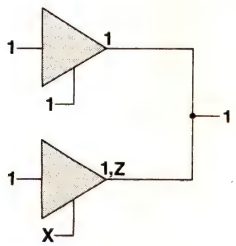
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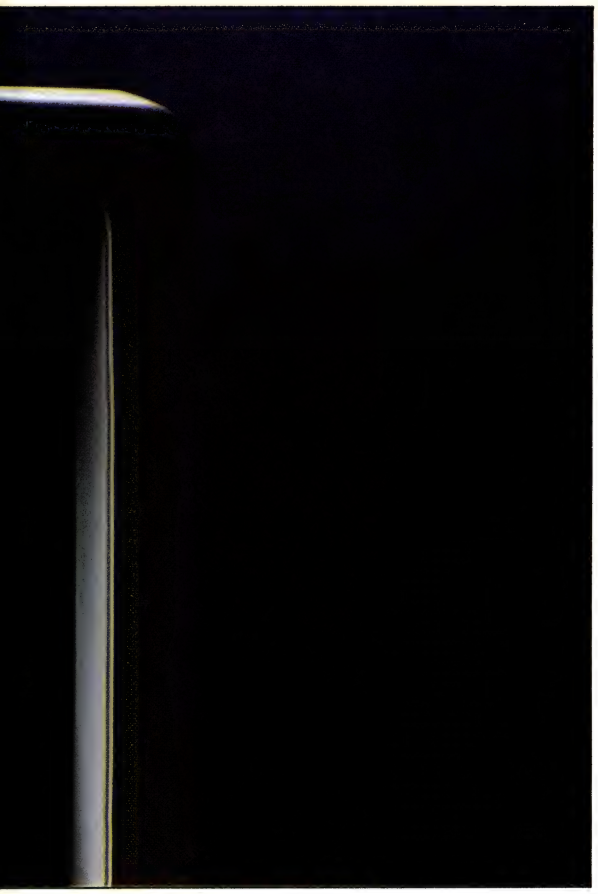
Designers using LASAR software can simulate logic activity more accurately than with any other tool available. Regardless of circuit complexity or IC technology.

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And you won't have to deal with reams of false hazard reports. Or miss any real hazards. By eliminating common ambiguity—the skew in signal timing shared by reconverging signals—LASAR Version 6 pinpoints all actual timing hazards. You'll verify designs more efficiently than ever before.



Use LASAR software PERUSE displays to analyze signal timing.

A model simulator.

Transfer the details of your design directly from your schematic capture or layout system. Or use LASAR Version 6 to model devices from the bottom up, using logic, memory, MOS primitives or gate array macros.

You can also build from the top down using Teradyne Modeling Language. TML is a register transfer language program that lets you compile a structural model from a functional description of a device.

For board-level modeling, LASAR Version 6 offers the largest, most accurate device library available, with more than 3,800 devices, SSI to VLSI.

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Lundy: a company as good as its products.

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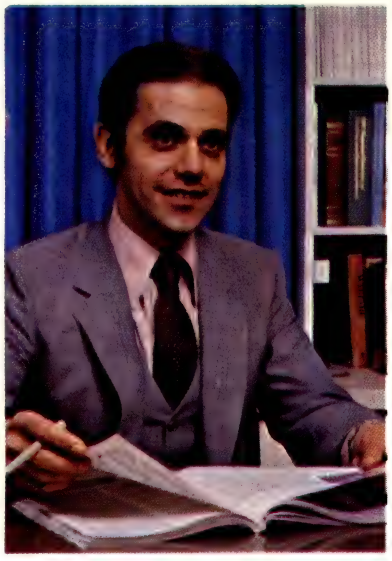
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CIRCLE NO 29

Mt. Everest, symbolic of aiming high, was generated on the Lundy T5680 raster. It offers 16 colors and 136 shades from a palette of 4,096 colors.



EDITORIAL



A negative vote for the IEEE

A new IEEE president-elect for 1984 has been found to fill the position left open by the unfortunate death of Donald King. Unfortunately, IEEE members were not given the opportunity to vote for King's successor. In a closed-door session, IEEE assembly members appointed Charles Eldon as president-elect.

The IEEE has once again left itself open to criticism by opponents of its policies—those who state that the organization doesn't adequately support, or even listen to, the working engineer. In this particular case, we'd be hard-pressed to disagree with these critics.

The Institute has taken the easy way out. Rather than asking its members to select a candidate they feel most represents their needs, the IEEE chose instead to quote from its bylaws, which state that "the assembly shall fill a vacancy occurring in the office of president-elect."

EDN doesn't question Charles Eldon's qualifications as IEEE's president-elect. Indeed, Eldon's past experience as executive VP in 1983, treasurer in 1981 and 1982, and his previous position as director of IEEE's Region 6 (comprised of the western US), makes him uniquely qualified to hold the post.

But is Eldon better qualified to represent the engineer than Hans Cherney or Jerrier Haddad who opposed King in the actual election and who each received sizable portions of the vote? We think not. Why? Because most IEEE members, except for the assembly members, don't know how Eldon stands on issues that might affect engineers.

Unfortunately, it's too late for the engineer to be heard. The IEEE, as a matter of misguided expediency, has made the choice for you—like it or not.

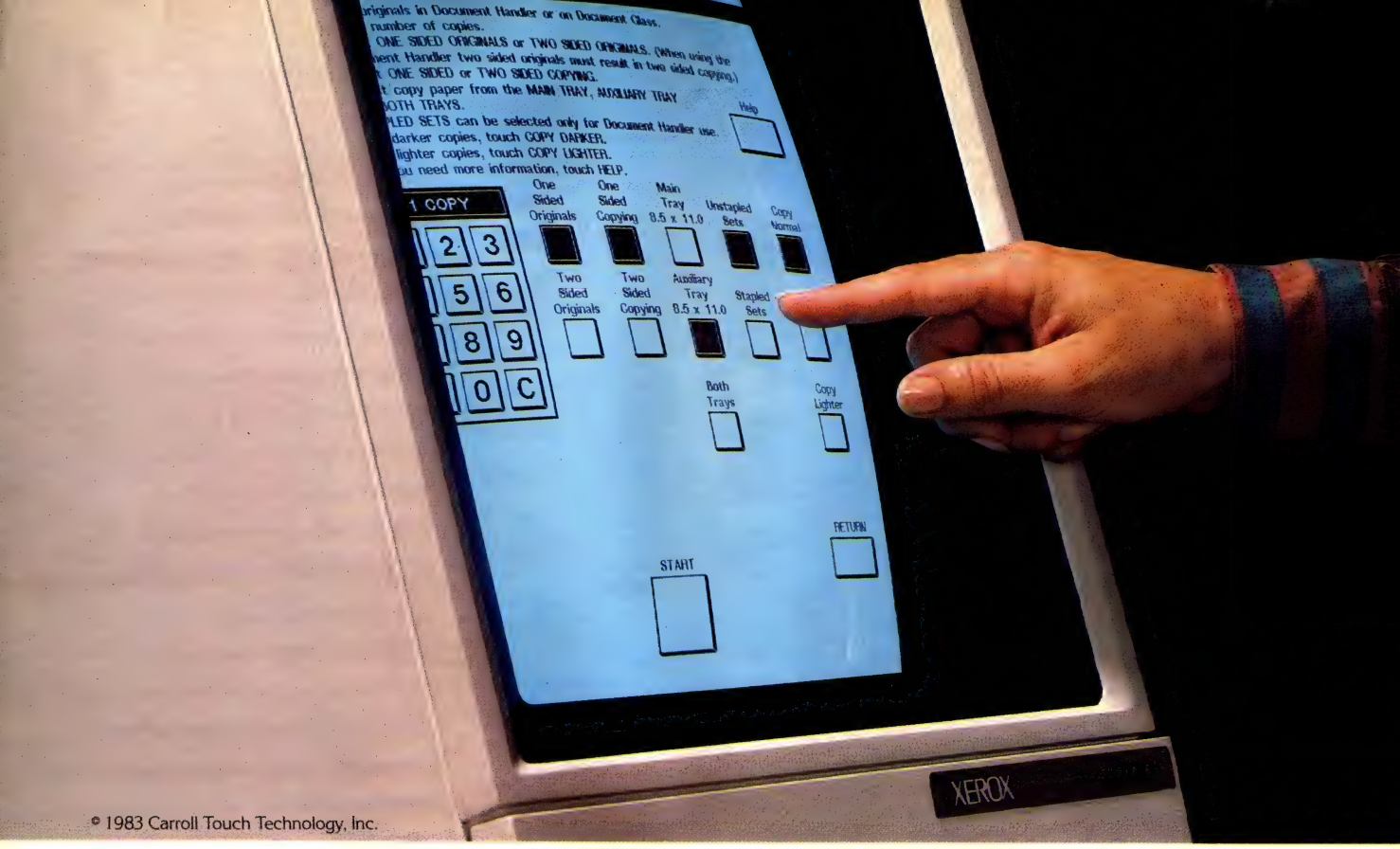
The IEEE strongly contested EDN's recent Professional Issues survey (April 19, pg 461), which found that more than 50% of the respondents were dissatisfied with that organization's representation of the engineer. While the IEEE is entitled to its own opinion, this latest action seems to support our findings. We, at EDN, believe actions speak louder than survey results.

John Tsantes

John Tsantes
Managing Editor



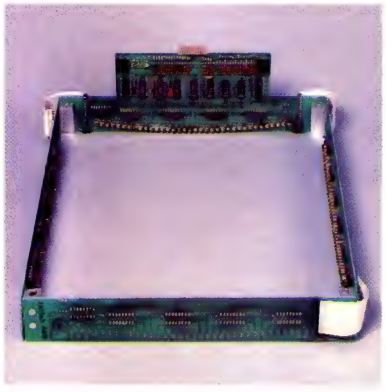
Jesse H Neal
Editorial Achievement Awards
1981(2), 1978(2), 1977, 1976, 1975
American Society of
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Carroll put the touch on Xerox

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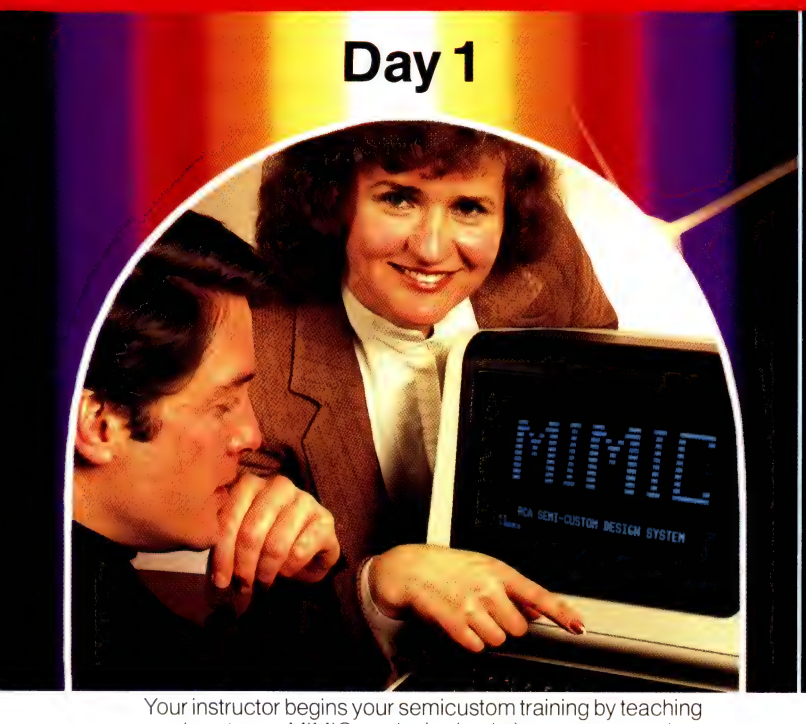
CIRCLE NO 30

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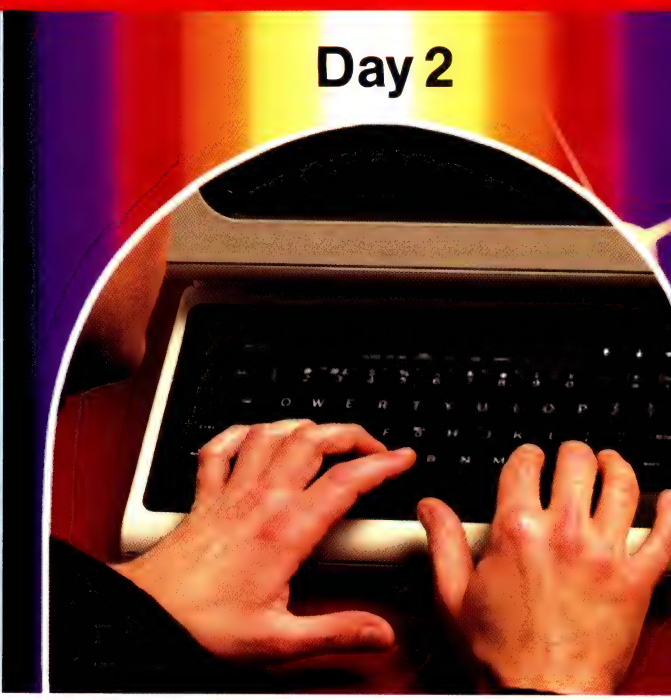


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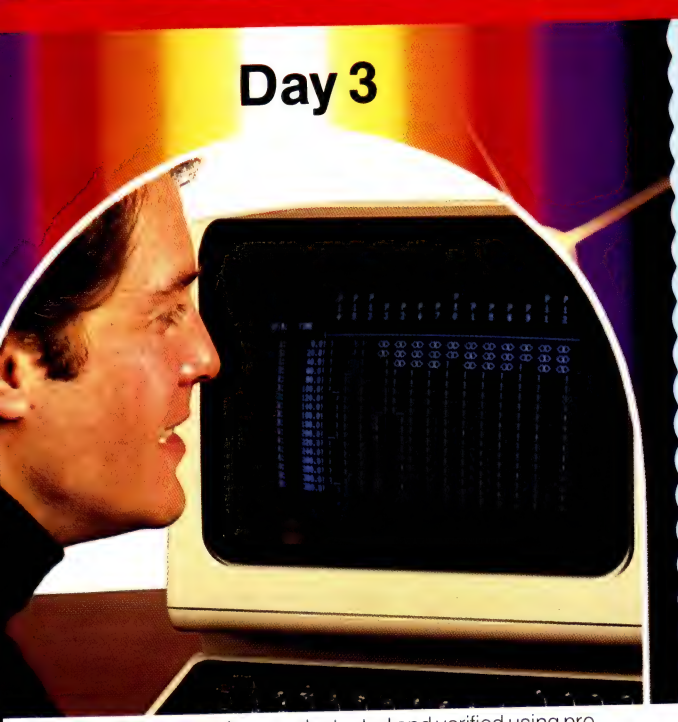
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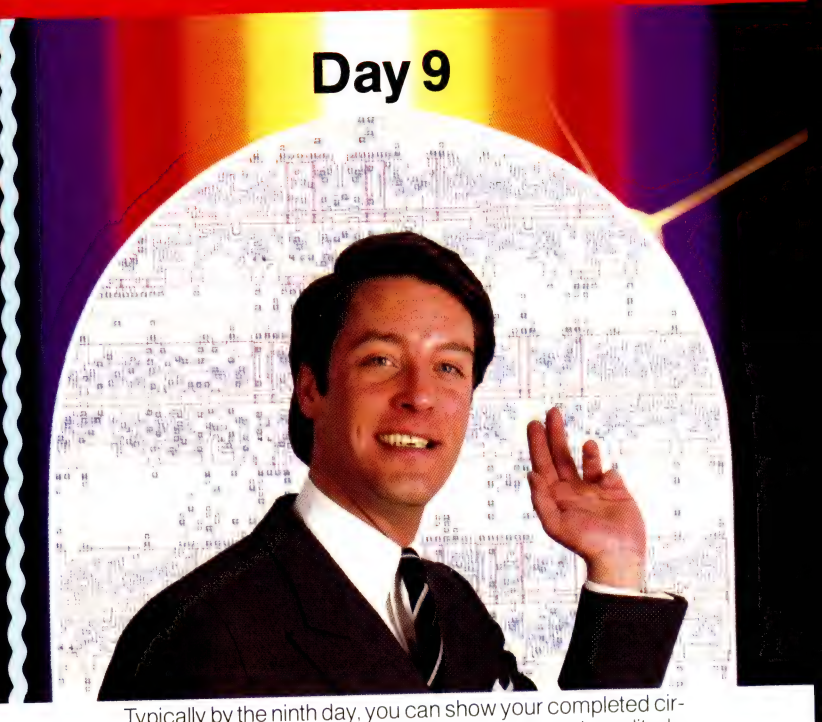
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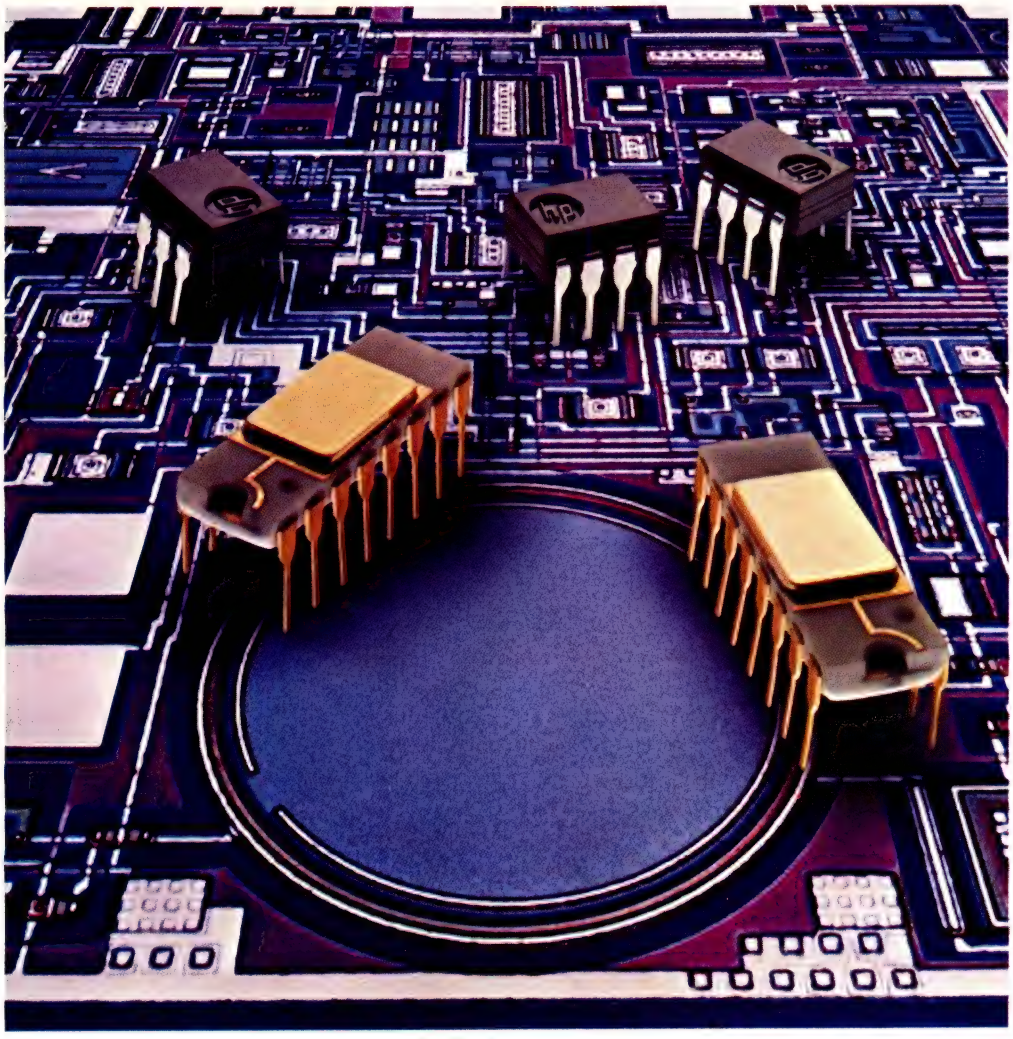
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CIRCLE NO 32

Demand for better resolution and animation spurs graphics-controller-IC improvements

William Twaddell, *Western Editor*

A rising demand for higher quality graphics displays—in a range of applications that includes personal computers, engineering workstations, CAD terminals, advanced video games and videotex—is prodding semiconductor manufacturers to introduce a variety of improved graphics-controller chips. Keyed to the ever-dropping price-per-bit of dynamic memories and exemplifying a growing trend toward bit mapping, these new ICs provide increased resolution and faster graphics-data processing.

Interestingly, the appearance of improved off-the-shelf graphics chips coincides with increased usage of custom chips. With newly available custom-design capabilities shortening chip-production times, graphics-product OEMs find the performance and marketing advantages of home-grown solutions increasingly attractive. Previously found only in expensive graphics workstations, custom graphics chips now appear even in inexpensive home computers.

Consumer products lead the way

In fact, much of the impetus for new graphics chips comes from personal computers such as the recently introduced Mindset and Apple's Macintosh and from video games, the area that started the graphics push. To maintain interest in a pastime that can quickly become boring, producers of the games are demanding graphics chips that provide higher resolution and better animation. In addition, many of these firms see an eventual end to stand-alone video games and are pushing into the low-end home computer business with high-quality video-game capability as a drawing card. Companies that haven't turned to a proprietary custom-chip solution (and many have) look to manufacturers such as Texas Instruments to provide chips with the necessary features.

One chip exhibiting this evolving graphics complexity is TI's advanced video display processor (AVDP). A new member of the 9918/9118 family of low- to medium-resolution display controllers, the AVDP is backward-compatible but adds a number of features not found in previous generations.

For instance, in implementing a NAPLPS (North American Presentation Level Protocol Syntax) videotex system, the AVDP provides improved 256×210-pixel resolution in bit-map mode and displays 16 colors from a palette of 512. Among the chip's other features is the ability to do pixel-by-pixel horizontal or vertical foreground scrolling without affecting memory. This feature allows the foreground to jump by as many as 256 pixels horizontally or as many as 210 pixels vertically.

To further conform with NAPLPS, the AVDP provides an external-video mode. In this mode it supplies a signal to an external video switch pixel by pixel, detailing which source—the AVDP or an ex-



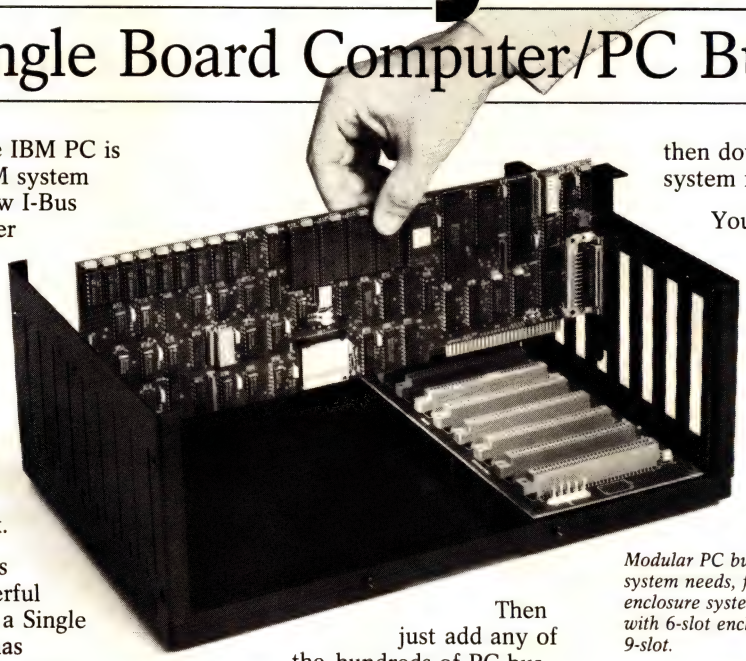
A fully bit-mapped display in NAPLPS *(North American Presentation Level Protocol Syntax) format demonstrates the color capability of Texas Instruments' advanced video display processor. Drawing from a 512-color palette, the chip can modify its 16 display colors on every horizontal retrace for subtle shading effects.*

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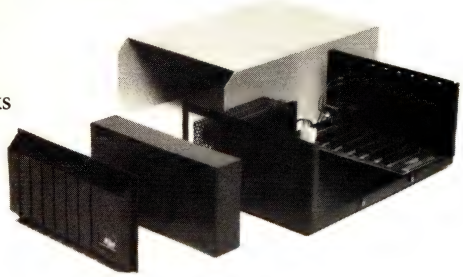
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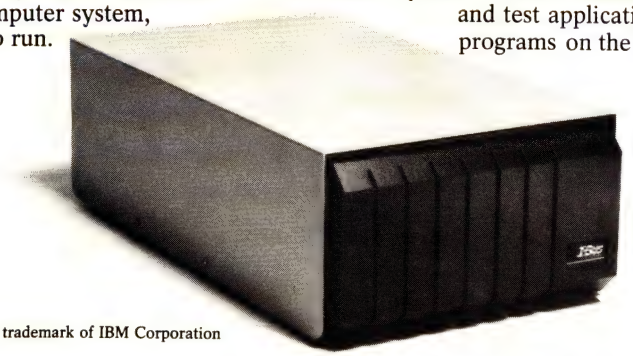
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CIRCLE NO 33

ternal video signal—is to appear on the screen. Another on-board feature is a complex sound generator.

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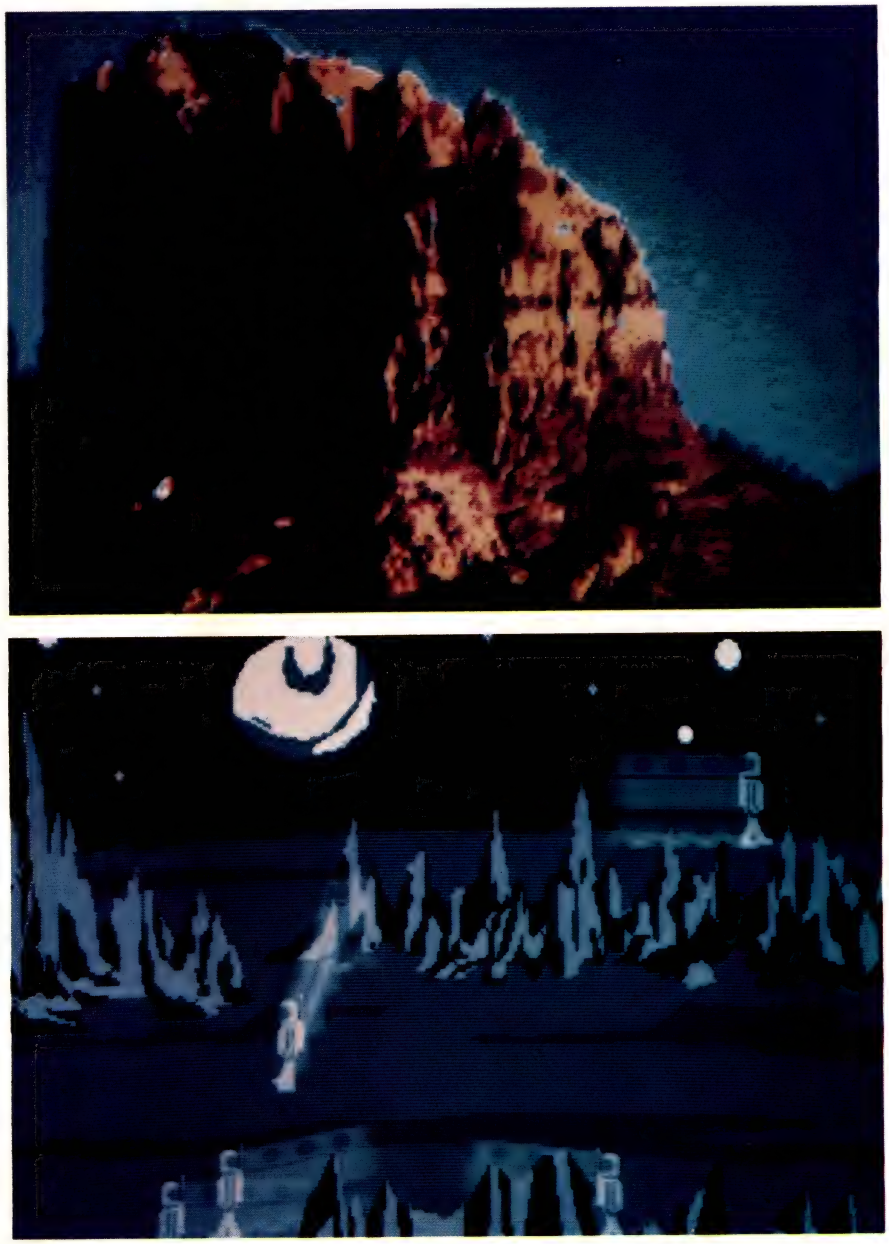
Like its predecessors, the AVDP generates 32 sprite planes that it uses for animation instead of software raster operations (raster ops). Also, like the 9118, the AVDP requires only two bytes to move a sprite anywhere on the screen in one horizontal-retrace time. In addition, it allows 10 sprites per line rather than four, and each line of the sprite can have a different color, thus reducing the number of sprites needed to describe an object completely. Sprites can occupy areas of 8×8, 16×16 or 32×32 pixels.

As another aid to animation, the AVDP allows grouping of sprites into one of eight blocks of related functions—a game's missiles or meteorites, for example—on the screen. A special register, offloading a task from the host μP, tracks each group and records when any member of one group collides with any member of another group. Contents of the eight blocks are dynamically reconfigurable.

The AVDP also contains a block-move instruction for animating a piece of the foreground or inserting a line of text. The instruction handles starting point, destination, number of bytes involved, sequencing, memory-access selection and, when it's through, μP interruption. With a programmable interrupt you can set for every horizontal retrace, the AVDP allows you to change the displayed colors or even redefine one or more sprites, positioning multiple sets of 32 sprites over different areas of the screen.

The AVDP operates in one of seven possible modes: three table-driven graphics modes at 256×192 resolution; one high-resolution, table-driven graphics mode at 512×192 resolution; the 256×210 bit-map mode; and text modes of 40 columns×24 rows or 80 columns×24 rows. The 256 patterns for the text characters reside in RAM and are dynamically redefinable to specify any font. In addition to providing a foreground and a background color, the AVDP's multicolor mode allows highlighting certain operations by overlaying the text character by character with a third color.

A high-density NMOS design, the AVDP can address and refresh 64k of dynamic RAM. It permits μP DMA to the video RAM and also provides all video, control and sync signals for either a TV or a composite or RGB monitor. Sampling of the AVDP is occurring now, and parts should be available sometime this summer. TI hasn't yet announced a price, but the AVDP's TMS9118 predecessor sells for less than $10 in large quantities, a price the AVDP



With attributes useful in games or text applications, *Motorola's MC68486/68487 raster memory system can drive screen resolutions from 64×64 pixels to 640×500 pixels. This mountain scene demonstrates 16-color capability at a bit-mapped resolution of 320×200. The game display shows complex animation effects of true object (sprite) manipulation.*

will doubtless reach in time.

Another graphics chip set comes from Motorola. Although reaching mostly toward personal-computer and workstation markets, the raster-memory system, consisting of the MC68487 raster memory controller (RMC) and the MC68486 raster memory interface (RMI), has features and a price suited for games, videotex and home computers. It takes screen resolution to 640×500 pixels in a PAL standard interlaced mode; normal resolution for a 60-Hz, NTSC standard display with 16-color capability is 320×210 pixels.

Designed to operate with M6809E and M68000 family μPs, the raster-memory set will address and refresh 1M byte of dynamic RAM and is backward-compatible with the MC6847/6883 display set. The RMI, built with bipolar ALS technology, generates all system clock signals and video timing signals. It provides an interface between video memory and the host μP, including handshaking and all timing signals required by the dynamic RAM. In a 6809E system, the RMI handles memory management for memories larger than 64k bytes, making use of page and nibble mode cycles.

The RMC, built in CMOS, features display-address generation, RGB outputs and video-data processing. It has on-chip alphanumeric and mosaic graphic generators and a 32-word color-mapping RAM (CMR) that contains the 32 colors chosen from a palette of 4096.

The RMC operates in bit-plane (bit-map) mode or in one of six list modes. Resolution is selectable from 64 to 640 pixels horizontally and from 64 to 500 lines vertically. In the bit-plane mode, each pixel can assume one of 16 colors, except in a 512× or 640× display where only four colors are available. The six list modes define a combination of features optimized for different applications. Among the choices are character count (32, 40, 64 or 80), number of lines per character row (8, 10, 12 or 16) and number of rows per screen (16 to 25).

In addition to 96 ASCII characters and two types of mosaic characters (in ROM), the RMC allows as many as 32k dynamically redefinable characters (DRCs) for special alphabets plus a special type of DRC called a fixed object. Some attributes of fixed objects—collision, priority (where one sprite passes in front of a second sprite and obscures that second sprite), CMR offset and shading—are especially useful in game applications. Attributes useful in text applications include flashing, video inverting, color, underlining, and generation of double-height and double-width characters.

The RMC can also generate eight different sprites—or true objects, as Motorola calls them—per line. They exist in all modes, and you position them with X-Y registers for use in animation effects. True objects have an 8-bit name that defines 256 different patterns; each true object can also have 24 different colors (with CMR offset) and the attributes collision, priority and zoom (two, four or eight times).

The RMC can accomplish smooth scrolling by defining a visible screen within a much larger virtual screen and then moving the visual screen pixel by pixel either horizontally or vertically. It also allows video overlay from external devices.

To ensure μP access to video memory for information updating, the RMI time multiplexes memory cycles, giving the μP a third of each cycle. Although this multiplexing prevents update/display refresh bottlenecks, it also limits system speed. In addition, with some new video RAMs, the feature is unnecessary (see **box,** "Multiport dynamic RAMs solve video-memory problems").

Motorola expects sampling for the raster-memory set to start in the 4th qtr of 1984. The price will likely be in the $20 range in high volumes by the end of 1985.

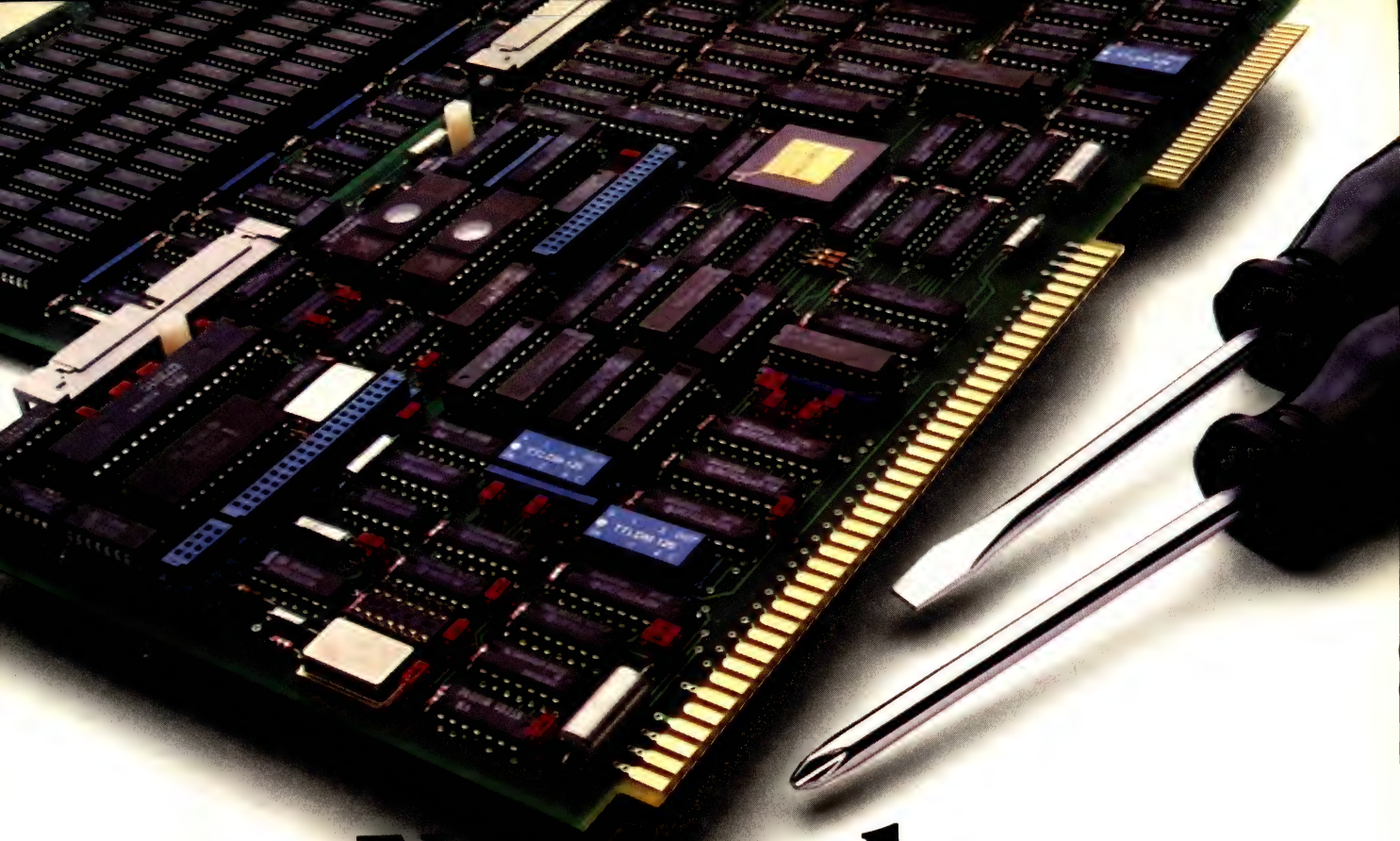
What's interesting about the TI and Motorola chips is their inclusion of a bit-map mode even for low- to medium-resolution applications. This trend to bit mapping is evident throughout the industry and probably spells the end of table-look-up graphics and, eventually, table-look-up text.

The device that started the bit-mapping trend is the NEC μPD7220, the first single-chip bit-mapped graphics controller. This chip has enjoyed the market that it created and that, until recently, it has pretty much had to itself. Several devices have appeared to challenge the 7220, however, and many more are on the way. Among them are the EF9367 from Thomson-CSF and the 7300/7301 chip set from NCR.

Consider first the EF9367. This device will handle a 1024×512 screen in color or black and white, using on-chip character and vector generators for text and graphics. It can also independently scale text characters horizontally and vertically to 16 times. The chip's vector generator can draw lines (continuous, dotted, dashed, or dashed and dotted) at a rate of 670 nsec/pixel. The EF9367 supplies composite sync and blanking signals and the timing necessary for interlaced or noninterlaced data.

NCR's chip set consists of the 7300 graphics-controller chip and the 7301 memory-interface controller. Four 7301s can work together to control as much as 1M byte of video memory. Like the Motorola RMS, the NCR set computes display addresses, refreshes memory, handles DMA and has RGB outputs. Each pixel can display a maximum of 256 colors, and the system allows dot-clock rates as high as 30 MHz.

NEC, meanwhile, isn't sitting still with the 7220. An improved version, the μPD7220A, with 10 functional changes and higher



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More good news from the Chairman of the Board



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speed, is currently in the sampling stage. Although downward compatible with the 7220, the -A version has several new features. For instance, it has two new reset modes that reset only selected parts of the chip, and it has the ability to halt a drawing command during updating of video RAM. In addition, it provides improved area-fill capability, external sync on every frame and a 16-bit μP interface.

The 7220A's major advantage is increased speed; it's now available in 6-, 7- and 8-MHz versions, upgrades from 5 MHz. In addition, by allowing a 128-MHz dot-clock rate, it increases display resolution to 2048×1024 from the previous 1024×792. This increased clock rate also boosts the DMA-channel data rate to 2M bytes/sec and drops the drawing time per pixel from 800 to 600 nsec. Further, using a lower resolution 640×512 display allows cutting that time in half. The 7220A also doubles the display-memory size allowed by the 7220 from 256k to 512k 16-bit words.

Now nearly through the sampling

Multiport dynamic RAMs solve video-memory problems

The trend toward bit-mapped displays is both good news and bad news for dynamic RAM manufacturers. The good news is that bit mapping boosts memory requirements by 10 to 40 times; the bad news is that ordinary dynamic RAMs can't meet the displays' bit-rate requirements. With some soon-to-appear multiport dynamic RAMs, however, the bit-rate problem goes away.

In some low-resolution cases, of course, single-port dynamic RAMs are adequate; certain high-speed devices can service a graphics screen directly. Two examples of such chips are the 80-nsec MK45H64 64k×1 and the 100-nsec MK4856 32k×8 from Mostek (Carrollton, TX). Another example is Intel's 100-nsec 51C64 CMOS 64k×1 dynamic RAM with ripple mode access.

Higher resolution screens, however, require bit rates in excess of 100 MHz, too fast for even static RAMs to handle directly. Consequently, system designers must increase memory bandwidth, using one of several possible approaches. One such approach is to use wider memories, like 16k×4 or 32k×8 devices, and convert back to a serial bit stream with a shift register. This approach is effective, but allowing 50% access for μP updates could require bit widths as high as 64, destroying single-pixel control and requiring many "glue" parts to implement. Double buffering the bit map also works, but it doubles the amount of memory required.

The most elegant solution to crop up comes from Texas Instruments in its TMS4161 multiport video RAM, a 64k×1 NMOS dynamic RAM that features a built-in 256-bit shift register with its own separate controls. Working completely asynchronously, the RAM array and the shift register relieve the bottleneck created from clashing requirements of display updating and screen refreshing.

The 4161's design allows dumping any 256-bit row of the chip's RAM array into the shift register in one cycle time. The RAM and the shift register then disconnect, and the shift register moves data out its own port at rates as high as 25 MHz. While the register is dumping its contents to the screen, the host μP has complete array access for updates.

As an example of the 4161's use, consider a screen with 1024×1024-pixel resolution. Such a screen requires 1M bit of memory, or 16 64k-bit dynamic RAMs, for each plane of color; screen refresh demands a bit rate of about 83 MHz. To satisfy the 83-MHz requirement, each of the 16 dynamic RAMs shifts its data at only 1/16 the dot rate, or 5.2 MHz—an easy task for the 4161. In addition, all the shift registers together hold 4096 bits of data, enough for four lines on the display. Consequently, if the shift registers load on every horizontal retrace (non-cycle-stealing), screen resolution can never outrun the capacity of the shift registers. As you increase resolution, you add dynamic RAMs and thus more shift registers.

Use of this type of memory will probably result in reconsideration of display-memory layout for future graphics systems. Because the shift-register reload time is so insignificant, a unified memory—accommodating both display and system μP—becomes possible. Fully bit-mapped systems will already have placed text and graphics in one memory space, but the parallel operation of RAM array and shift register means the system μP needn't have a separate memory space of its own. In fact, notes Karl Guttag, senior member of the technical staff and graphics definition manager for Texas Instruments, even today's 32-bit μPs aren't fast enough to take advantage of the increased access time the on-board shift registers give for display updating.

TI has been sampling the 4161 since last November and plans to announce the part this July at SIGGRAPH. Also planned for announcement this year will be a competing dual-ported part from NEC. The NEC device will have a 64k×4 architecture and four 256-bit shift registers to handle four bit planes.



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stage and ready for production, the 7220A will initially cost $119.88 (100); the 7220's current price is $87.92 (100).

A possible future competitor for the 7220 family could come from a current alternate source, Intel Corp. In addition to the 7220 (Intel calls its version the 82720), the company makes a highly capable text coprocessor, the 82730. Some combination of these two parts would be a natural extension of Intel's line, although a simple joining of the two parts is unlikely. It's possible that NEC and Intel, having worked together on the definition of the 7220, might engage in a joint effort.

Good graphics at low cost

Despite the capabilities and speed of the 7220A and its potential competitors, manufacturers of the really high-performance, high-resolution graphics terminals have always built their own custom graphics engines and coupled them to bit-slice processors. The resulting machines usually start at about $50,000, however. A new personal-computer company is bringing much of their graphics power to a machine that starts at just $1200.

Sporting high-speed, full-color graphics, the Mindset personal computer from Mindset Corp (Sunnyvale, CA) employs a 16-bit 80186 host μP with a full-custom graphics-coprocessor set. The set, consisting of a graphics-coprocessor chip and a display-processor chip, was designed by Mindset and produced by VLSI Technology Inc (San Jose, CA). Although its designers kept the Mindset computer's resolution low (320×200) to work with low-cost TV displays, the computer nonetheless offers full bit-mapped graphics and text, 16 colors (from a 512-color palette) and hardware raster ops.

The Mindset's graphics-coprocessor chip, which itself has the power and complexity of a 16-bit μP, performs raster-op, or *bitblt* (bit-aligned block transfer), operations that give the computer its seamless graphics and smooth animation. With speed derived from its micro-coded architecture, the coprocessor works as a graphics accelerator to offload the 80186.

Eight different block-transfer modes in the Mindset coprocessor combine source-pixel data (or its inverse) with destination-pixel data. Combinations can occur via the Boolean operations AND, OR, XOR and NOT, or the source-pixel data can simply replace the destination data. In addition, each operation is modifiable by a series of masks. A write mask, for example, defines parts of the destination area to be altered. Similarly, a collision mask defines what constitutes a collision (as of sprites), and a clipping mask defines a screen window in which *bitblt* operations can occur. (Clipping is the process of "trimming" the portion of an image that falls outside a viewable area.) Another coprocessor feature, the transparent mode, allows the creation of sprites with essentially no limitations on size, color or position.

The graphics coprocessor can define a wide range of interrupt conditions, including the occurrence of collision, clipping or the completion of an operation. It can also generate an interrupt on vertical retrace and on every horizontal retrace to allow μP modifications to the frame buffer (video memory). Alternatively, if the computer needs to use only half or less of its 32k bytes of graphics memory, it can set up two frame buffers, alternately displaying each while updating the other.

The graphics coprocessor can also draw arbitrarily selected straight lines using a built-in function. In addition, being completely bit-mapped, it can create text with any font and character size.

As is the case with most two-chip sets, Mindset's second device is a display processor that specifies screen resolution and color and supplies output sync and timing signals. It can drive a 320×200-pixel screen with 16 colors or a 640×200 screen with four colors, both noninterlaced. It also has a 640×400 mode with two colors, but because it's implemented with interlacing, it causes most screens to flicker. Output options for the display processor include TV, composite color monitor and RGB monitor. The device also refreshs graphics memory.

But as capable as it is, Mindset's custom chip set belongs exclusively to Mindset and isn't a threat to standard graphics controllers. Custom solutions have rarely been a threat, in fact, because of the time and money that custom development requires. A recently devel-

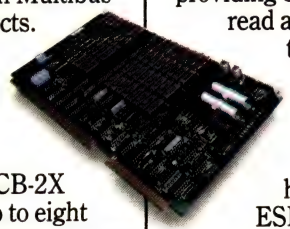


A custom graphics-coprocessor and display-processor chip set *are components in the Mindset personal computer, an 80186-based machine that sells for only $1200 in its basic configuration. The coprocessor performs raster operations that give the Mindset seamless graphics and smooth animation. The Mindset's display, indicative of an industry trend, is completely bit-mapped for both graphics and text.*

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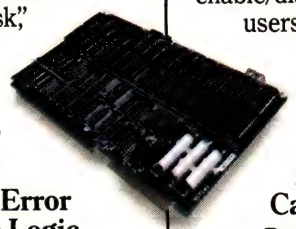
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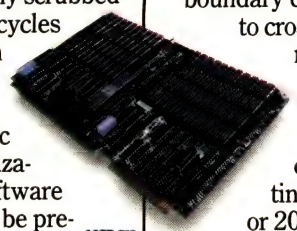
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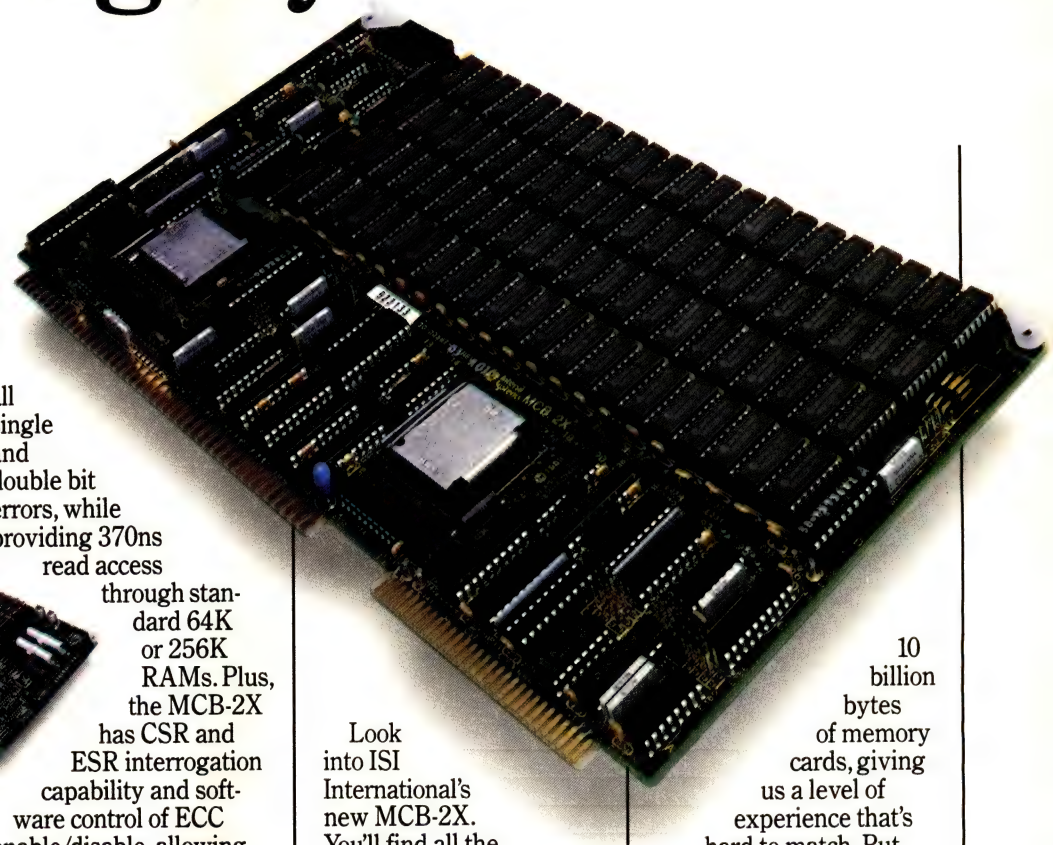
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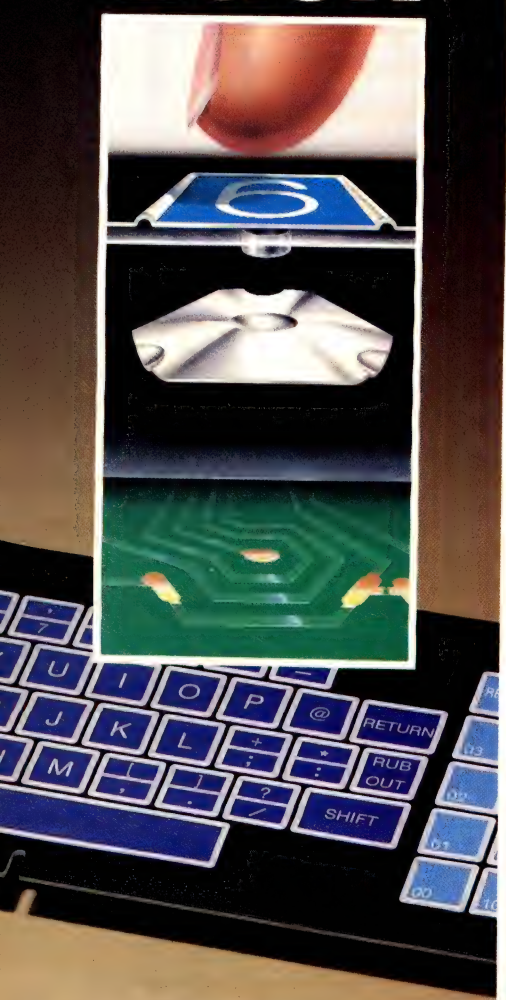
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Silicon Compilers Inc
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Los Gatos, CA 95030
(408) 370-2008
Circle No 676

Texas Instruments Inc
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Houston, TX 77001
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MOS Memory Activity
Box 1443, M/S 6101
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Thomson-CSF Components Corp
Semiconductor Div
Box 1454
Canoga Park, CA 91303
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oped custom graphics-accelerator chip has changed that, however. Now that licenses for manufacturing the chip are available, the device poses a threat to standard products.

The new chip, appropriately named RasterOp and developed by Silicon Compilers Inc for use in workstations manufactured by Sun Microsystems (Mountain View, CA), performs much like Mindset's graphics coprocessor; it handles *bit-blt* operations that are basic to window manipulation, scrolling, drawing vectors or painting characters. Design of the chip took only five months, and production of an actual working chip took a total of only eight months. Silicon Compilers also designed the DEC MicroVAX I and the Seeq Ethernet chips in similar time periods.

Short turnaround times like these can obviously take much of the sting out of producing a custom chip. The RasterOp is a general-purpose chip, not dedicated to any particular architecture, but it could easily have been tailored to a target application, much as was done with the Mindset coprocessor.

In contrast to the Mindset coprocessor's eight operations with modifiers, the RasterOp (part number 16160) implements 256 functions that map source, destination and pattern registers into 16-bit outputs. Using 16-bit data paths, it handles all bit shifts and masks, is display-resolution independent and supports both black-and-white and color displays. Silicon Compilers claims that the RasterOp is 50% faster than implementations of the chip's functions in software.

Silicon Compilers doesn't sell the chip, but it does sell a license to make it for $80,000. While prices like that sound expensive, consider that systems built with standard parts tend to look the same, while a custom chip set like Mindset's can put a company far ahead of its competitors. **EDN**

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1. Twaddell, W, "Next-generation graphics chips to debut; bit-slice designs suit high-performance use," *EDN*, September 29, 1983, pg 63.
2. Williams, G, "The Mindset personal computer," *Byte*, April 1984, pg 270.

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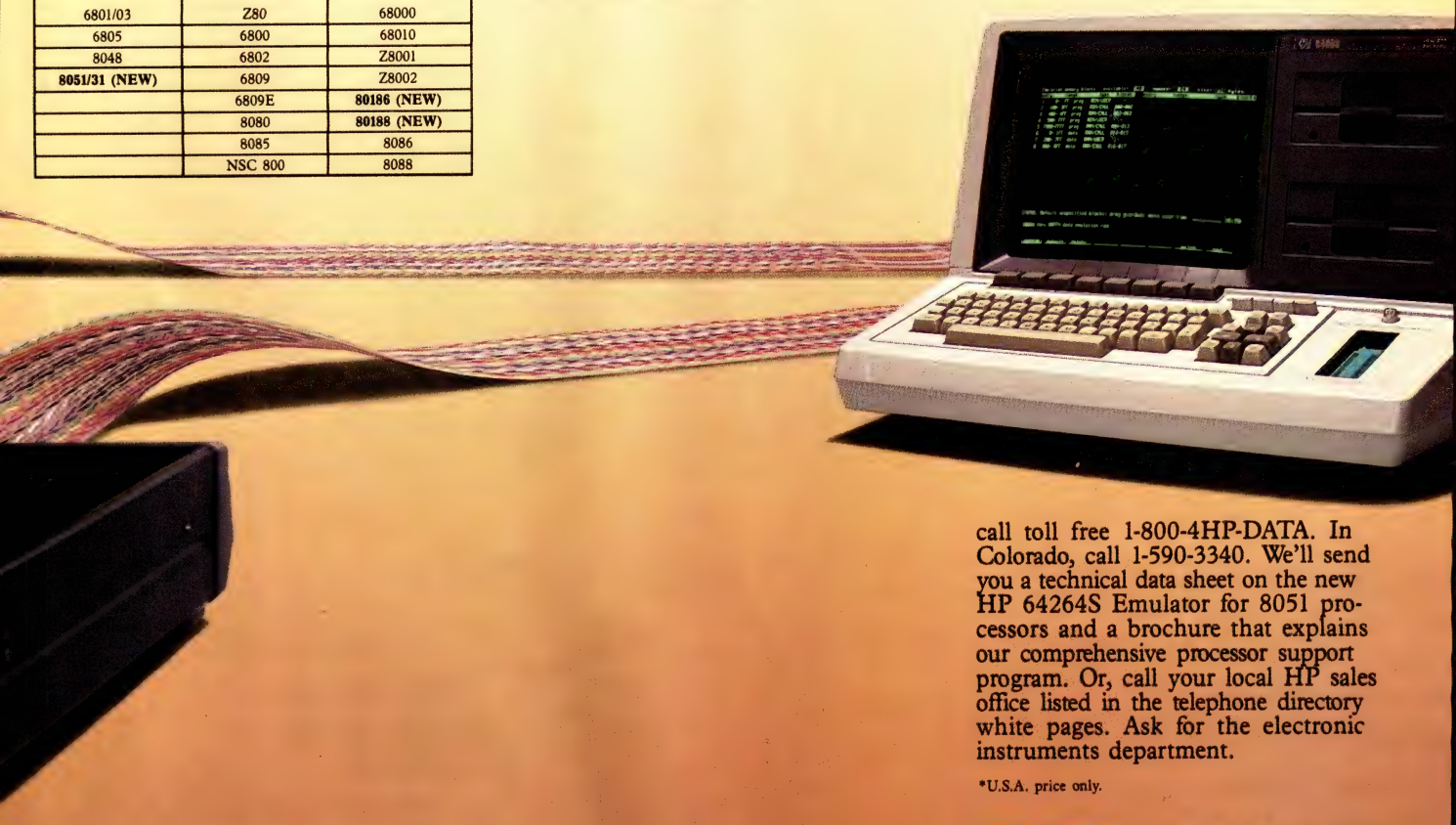
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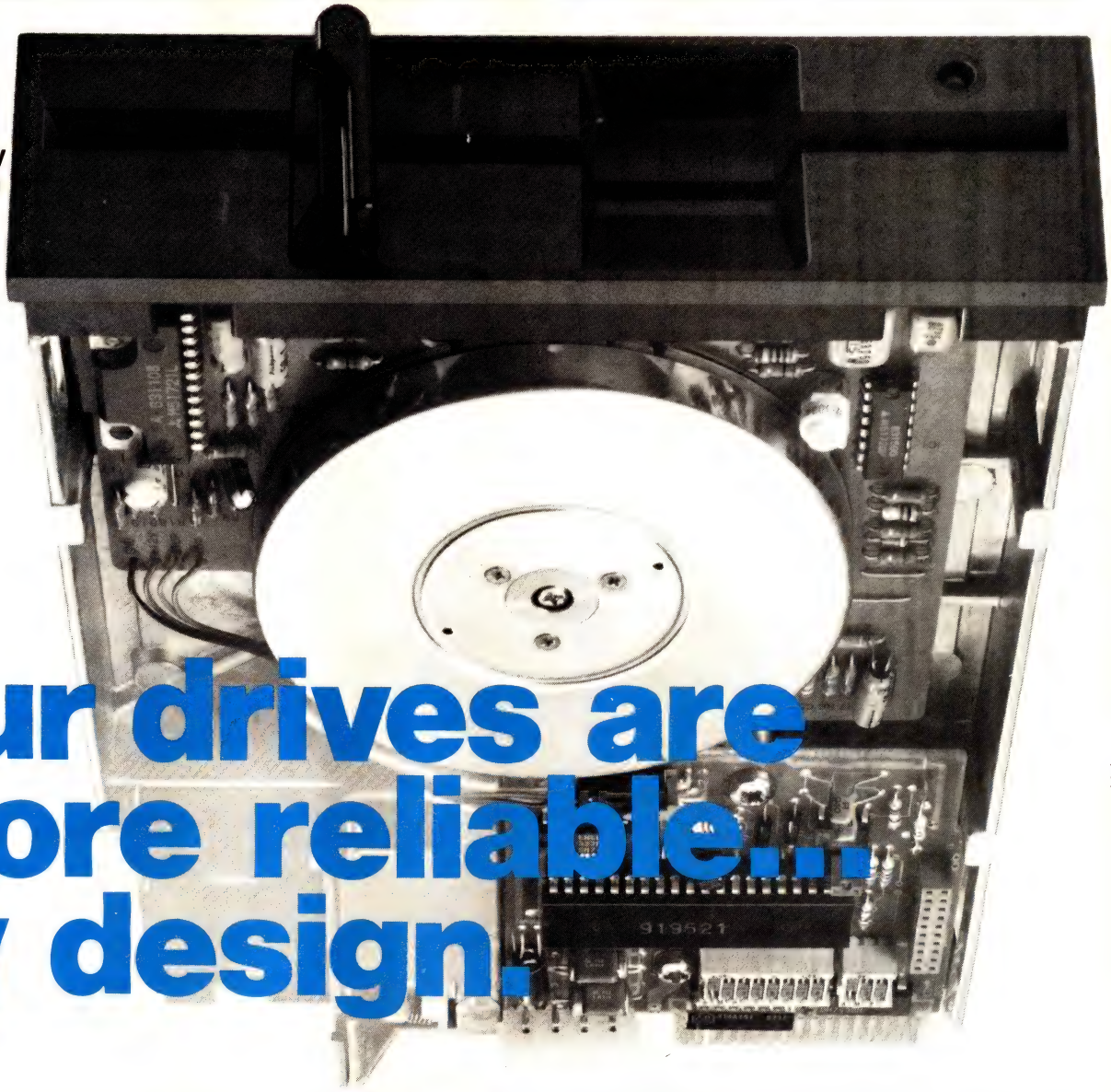
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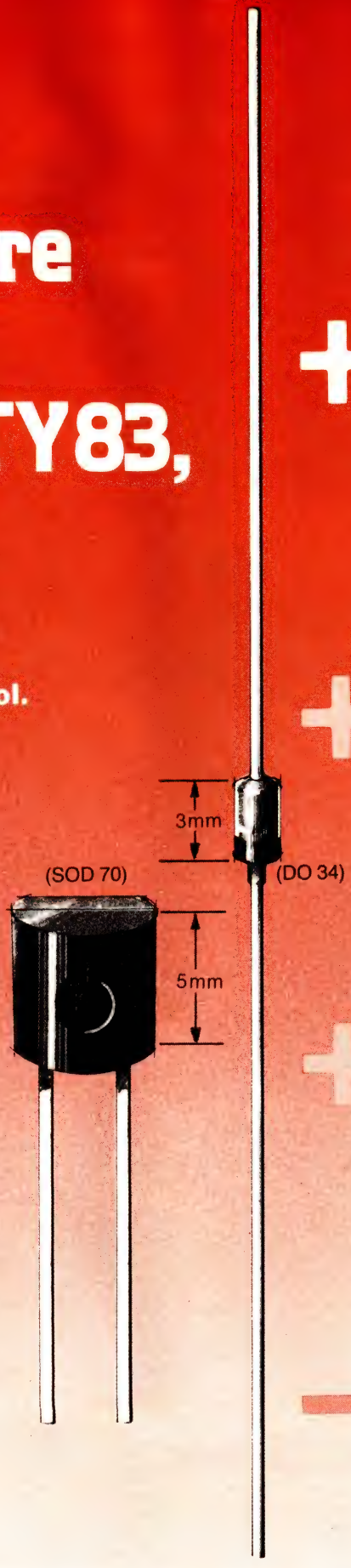
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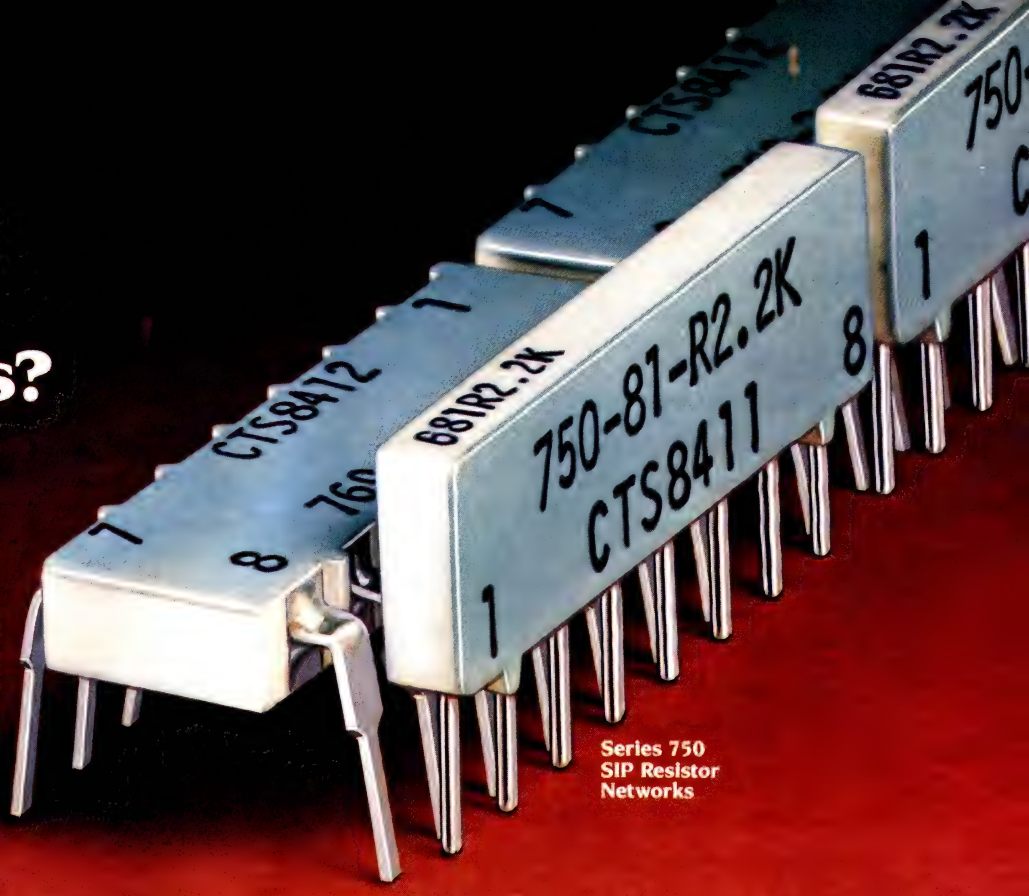
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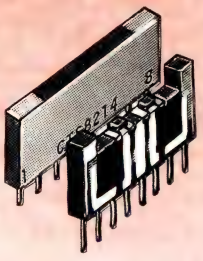
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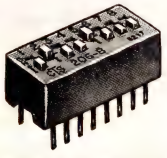


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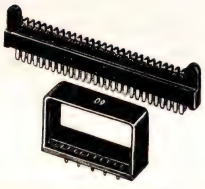
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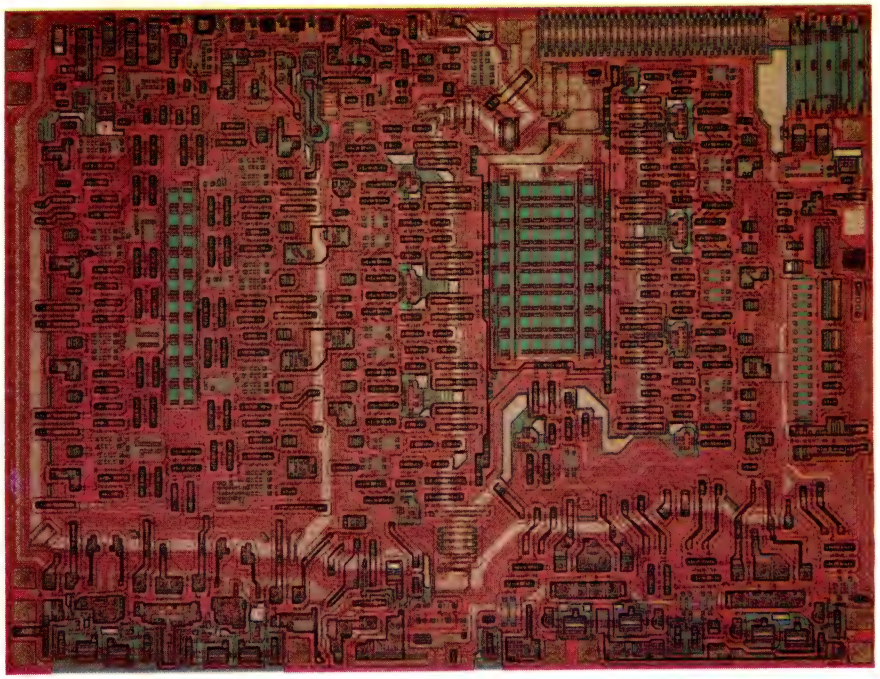
DIP-housed track/hold amplifiers follow A/D-converter advances

Bill Travis, *Associate Editor*

If you're trying to squeeze a little more performance out of your A/D-converter application, you might consider using a track/hold (T/H) amplifier. Though emerging high-speed, high-resolution A/D converters bring dazzling—and affordable—performance to a number of signal-processing applications (see the Special Report on data converters, EDN, June 14, 1984, pg 118), many time-varying-input situations render them next to useless. With the aid of innovative DIP-enclosed T/H amplifiers, however, your A/D converter can live up to its potential.

Before proceeding further, a clarification of the nomenclature is in order. Specifically, it's important to understand the difference between a sample/hold and a T/H amplifier. Upon application of a Sample command, the former captures the instantaneous value of the input signal, and then goes immediately into hold mode. The T/H amplifier acts as a normally-unity-gain amplifier (inverting or noninverting) when in track mode, and it holds the input's value only upon the issue of a Hold command.

True sample/hold amplifiers are rare. They're used in such specialized applications as high-speed radar. Curiously, monolithic-device manufacturers have chosen the in-



A monolithic T/H amplifier *from Precision Monolithics features minimal droop variation over temperature, thanks to its bipolar output amplifier.*

TABLE 1—MONOLITHIC TRACK/HOLD AMPLIFIERS

MODEL	LF198	HA5320	SMP10	SMP11	AD585	HA2420-1	UNITS
INPUT IMPEDANCE	10^{10} TYP	10^{6} MIN	3×10^{10} MIN	3×10^{10} MIN	10^{12} TYP	5×10^{6} MIN	Ω
BIAS CURRENT	25 MAX	200 MAX	50 MAX	50 MAX	3 MAX	200 MAX	nA
GAIN ERROR	0.005 MAX	5×10^{-5} TYP	0.037 MAX	0.037 MAX	NO SPEC A_{VOL}=200,000	NO SPEC A_{VOL}=25,000 MIN	%
DROOP AT 25°C	0.1 MAX C_H=1000 pF	0.08 TYP	0.02 MAX C_H=5000 pF	0.2 MAX C_H=5000 pF	1 MAX	0.05 MAX	V/SEC
DROOP AT T_{MAX}	NO SPEC	1.2 TYP	0.05 MAX C_H=5000 pF	0.36 MAX C_H=5000 pF	DOUBLES EVERY 10°C	0.22 TYP AT 200°C	V/SEC
PEDESTAL	1 MAX	1 TYP	4 MAX	4 MAX	3 MAX	15 MAX	mV
FEEDTHROUGH	−86 MAX C_H=0.01 μF	−76 MAX	−86 MAX	−86 MAX	−92 TYP	−76 TYP	dB
ACQUISITION TIME TO 0.1%	6 MAX C_H=1000 pF	1.2 MAX	3.5 TYP	3.5 TYP	NO SPEC	4 TYP	μSEC
ACQUISITION TIME TO 0.01%	NO SPEC	1 TYP	5 TYP	5 TYP	3 MAX	5 TYP	μSEC



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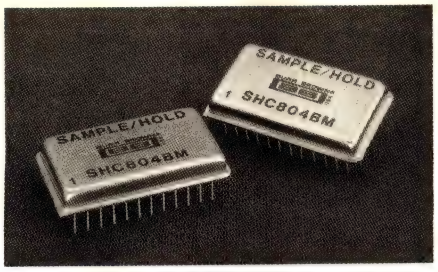
CIRCLE NO 42

correct "sample/hold" designation; all the hybrid products except two use the correct "track/hold" term.

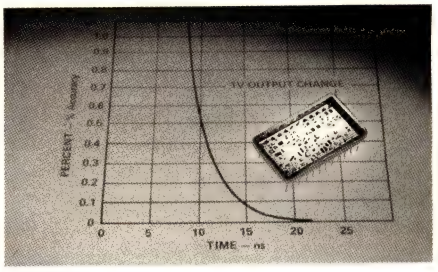
Why use a T/H amp?

The need for T/H amplifiers becomes clear when you consider their role in A/D-converter applications. For instance, suppose you purchase a 12-bit A/D converter that offers a blazing 2-μsec conversion time. This figure, of course, makes you think of 500 kHz and an attendant ability to handle high-frequency signals. In reality, the A/D converter can only tolerate input frequencies of a few tens of hertz before yielding intolerable errors. By using a T/H amplifier at the A/D converter's input, however, you can "freeze" the input during the conversion time, eliminating frequency-limitation errors.

In another application, you might be using a flash A/D converter to digitize signals whose frequencies reach the tens of megahertz. The A/D-converter manufacturer assures you there's no need for a T/H amplifier, because you can latch the input comparators. But while latching the input might work for low- to medium-slew-rate signals, in some cases fast-slewing input signals can cause the input comparators to behave erratically, yielding codes that make no sense at all. Again, the solution is to put a T/H amplifier before the A/D converter to hold the input stable.



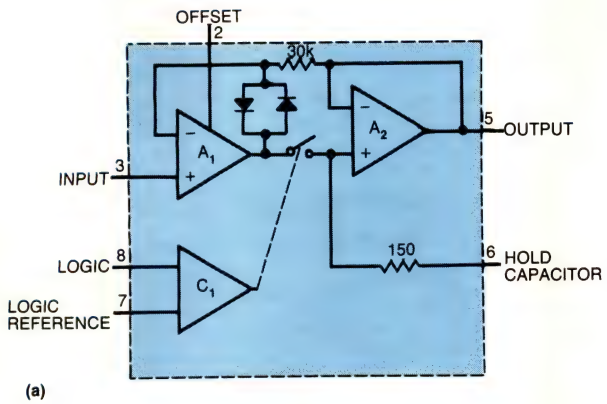
Adding an input-buffer option *to a fast industry-standard 12-bit T/H amplifier, this hybrid from Burr-Brown Corp comes in a metal "bathtub" DIP.*

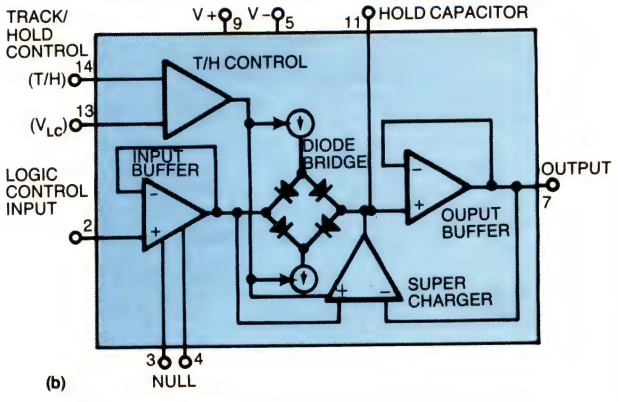


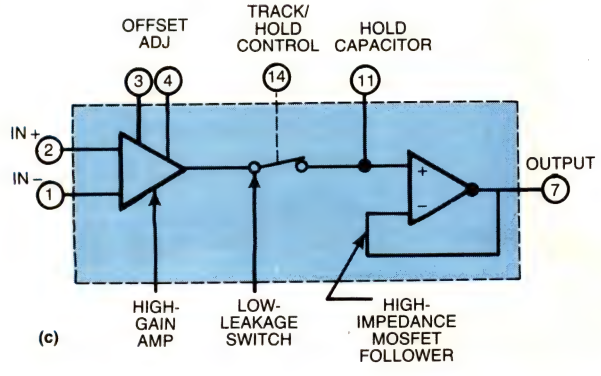
This flash-converter driver *from Analog Devices eliminates input-slewing problems, thereby allowing conversions at the full Nyquist rate.*

Monolithics play catch-up

As in op amps and data-converter products, the level of performance







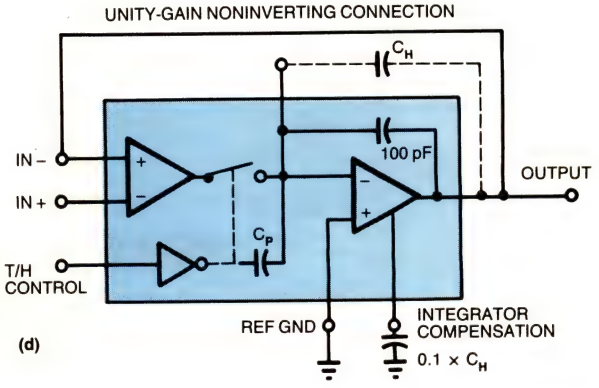
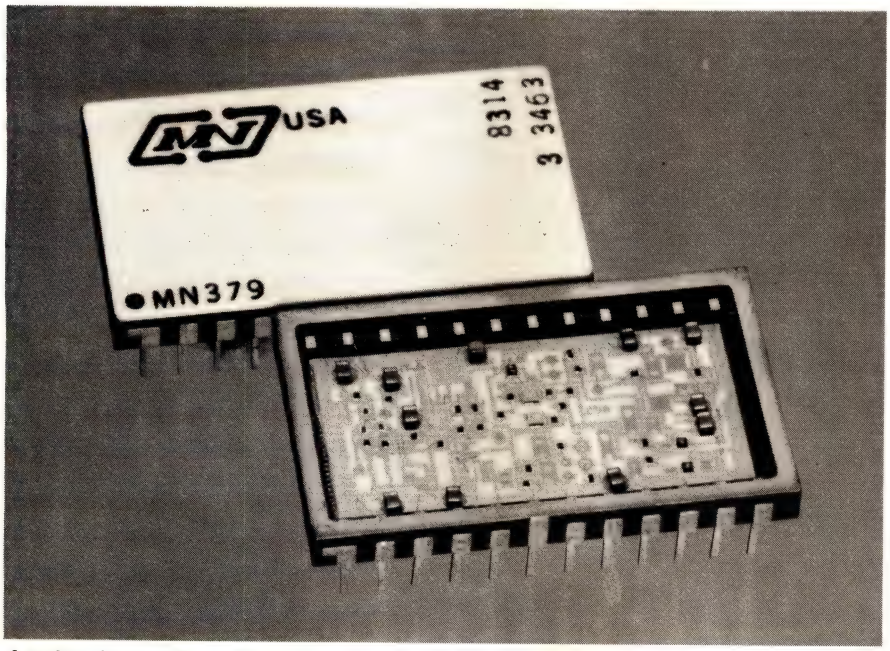


Fig 1—These track/hold-amplifier configurations *fill moderate-speed, moderate-resolution requirements. The classic LF198* **(a)** *is perhaps the most widely used T/H IC in the industry. The SMP10 and -11* **(b)** *improve on the -198's speed. The HA2420-1* **(c)** *specs parameters to 200°C. The pin-compatible HA5320 and AD585* **(d)** *use an integrating approach to minimize pedestal dependency on input level.*

available in T/H amplifiers depends on the technology you select. Indeed, the steady advance in monolithic devices serves to keep hybrid and module manufacturers on their toes. In fact, the newer monolithics discussed here deliver performance only hybrids and discrete modules were capable of until just recently. Unlike these other product areas, however, the number of products available from the industry is small. (The numbers are expected to increase significantly, however, once the performance benefits of these devices become better known.)



Another flash-A/D-converter driver, *this hybrid from Micro Networks features a 20-nsec acquisition time. It's housed in a ceramic DIP.*

Consider, for example, the products listed in **Table 1.** Three are ICs that have existed for a few years, and the other two are newer T/H amplifiers that show clear advances in performance over their predecessors. **Fig 1** gives block diagrams for four classes of products: the multisourced 198/398 family (**a**), Precision Monolithics Inc's SMP10 and -11 (**b**), Harris's 2420 Series (**c**) and the newest configuration (**d**), embodied by Harris's HA5320 and Analog Devices' AD585.

First, consider the industry-standard LF198/398 Series, supplied by National Semiconductor Corp, Advanced Micro Devices, Fairchild Semiconductor, Signetics Corp and Linear Technology Corp. It's a widely accepted, general-purpose T/H amplifier that offers medium performance at prices starting at approximately $2.85 (100). It features splendid gain accuracy and low droop (implying very low leakage at the hold-capacitor junction).

TABLE 2—FAST 12-BIT TRACK/HOLD AMPLIFIERS

MODEL	MN376	MN377	THA05203	SHC803	SHC804	UNITS
INPUT IMPEDANCE	10^3 TYP	10^3 TYP	10^3 TYP	10^8 TYP	10^3 TYP	Ω
GAIN ACCURACY	0.1 MAX	0.1 MAX	0.1 MAX	0.1 MAX	0.1 MAX	%
GAIN NONLINEARITY	0.01 MAX	0.01 MAX	0.01 MAX	0.005 MAX	0.005 MAX	%
INPUT OFFSET	5 MAX	10 MAX	5 MAX	5 MAX (+5 BUFFER)	3 MAX	mV
DROOP AT 25°C	5 MAX	10 MAX	5 MAX	5 MAX	5 MAX	V/SEC
DROOP AT T_{MAX}	15 TYP AT 70°C	NO SPEC	15 TYP AT 70°C	100 MAX AT 85°C	100 MAX	V/SEC
PEDESTAL	20 MAX	25 MAX	20 MAX	5 MAX	5 MAX	mV
FEEDTHROUGH	−74 TYP	−74 TYP	−74 TYP	(0.03% MAX)	(0.03% MAX)	dB
ACQUISITION TIME TO 0.01%	200 MAX	100 MAX	200 MAX	350 MAX	350 MAX	NSEC
POWER DISSIPATION	875 MAX	875 MAX	875 MAX	1025 MAX	875 MAX	mW
SLEW RATE	300 TYP	300 TYP	300 TYP 150 MIN	160 TYP (10 BUFFER)	160 TYP	V/μSEC
APERTURE JITTER	50 TYP	50 MAX	50 TYP 100 MAX	25 MAX	25 MAX	PSEC
TP4860/HTC0300 PIN COMPATIBLE?	YES	YES	YES	NO	YES	



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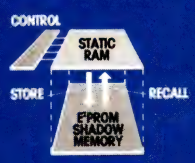
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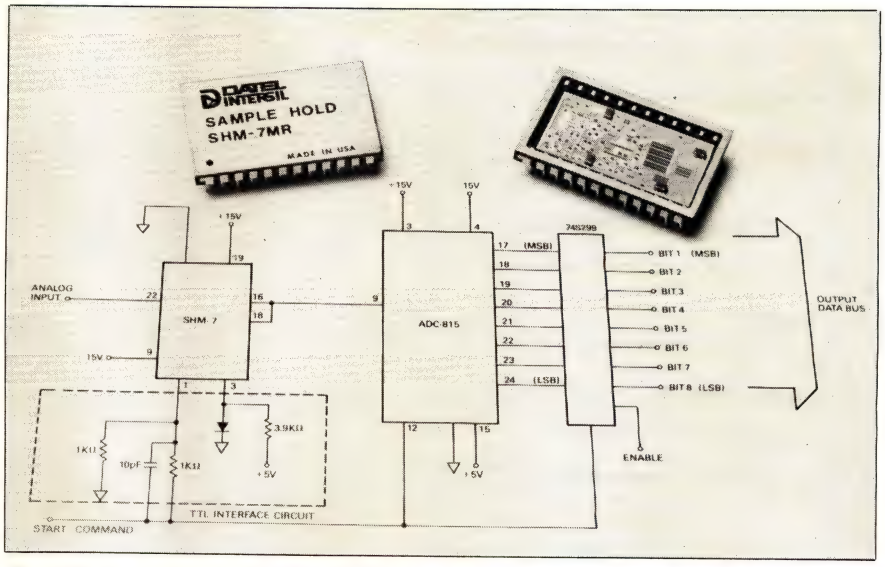
*NOVRAM is Xicor's nonvolatile static RAM device.

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Although the tight gain and gain-drift specs would seem to imply adequacy for 12- or 13-bit applications, beware: You must consider nonlinearities issuing from input-dependent variations in the hold step (also called the "pedestal"; see **box,** "Track/hold specs: a potpourri of terms"). Spec-sheet curves show that with a 1000-pF hold capacitor, the pedestal can change from 13 to 7 mV when the T/H amplifier's input changes from −10 to +10V. This variation, translating directly to a transfer-function nonlinearity, represents 1¼ LSBs at 12 bits.

Why is there this dependency of pedestal size on input voltage? The pedestal, or track-to-hold step,



Containing two output buffers, *this T/H amplifier from Datel-Intersil is ideal for multistage flash-converter configurations.*

Track/hold specs: a potpourri of terms

As splendid as the performance may be for the track/hold (T/H) amplifiers described in the text, you must be able to interpret their data-sheet specs and relate them to your system's needs. Sometimes that's not easy, especially when the vendors of the parts use widely differing terms and, what's worse, disparate definitions of the same terms.

Consider "pedestal," for example. It's the step that appears in the output when you switch from track to hold mode. It comes from the charge dumped from the T/H switching circuitry's stray capacitance to the hold capacitor. Look, however, at the names given this parameter by different T/H-amplifier manufacturers: pedestal, hold-mode charge offset, sample-to-hold step and sample-to-hold offset error.

Another possible pedestal-related area of confusion is the parameter "charge transfer," usually expressed in picocoulombs (pC). This parameter is useful if you want to connect an external hold capacitor. Knowing the amount of charge the switch dumps to the hold capacitor, you can calculate the pedestal by solving for V in the relation Q=CV.

What are the parameters "leakage current into hold capacitor" and "drift current," seen on two manufacturers' data sheets? They're the same: the current that leaks into or out of the hold capacitor with the T/H switch open. Again, this parameter is useful if you're applying an external hold capacitor. To calculate droop, solve for dV/dt in the expression I=CdV/dt.

Now for the can of worms: aperture-time parameters. Consider the following data-sheet definitions:

- Aperture time: The delay required between the Hold command and an input analog transition, so that the transition does not affect the held output.
- Aperture time: The time required for the T/H switch to open (10 to 90% open), independently of delays through the switch driver and the amplifier circuitry.
- Aperture time: The time required for the T/H amplifier to switch from track to hold.
- Aperture delay time: The time from the Hold command's 50% transition point to the time the output stops tracking the analog input.
- Aperture delay: The delay *before* the T/H switch opens (including the switch-driver circuitry).
- Effective aperture delay time: The difference between the propagation time from the analog input to the T/H switch, and the digital delay between the Hold command and the opening of the switch.
- Effective aperture delay time: The interval between the leading edge of the Hold command and that instant when the analog input equals the held value.

Confused? You have a right to be. Take solace, however: The last two definitions (which are really equivalent) seem to be gaining favor in the industry. They effectively define the difference between analog and digital propagation times in a T/H amplifier, and the resulting figure can be negative, zero or positive. According to Analog Devices, this spec is a useful one for assessing T/H performance, because it includes all the components that have an effect on how quickly the device can make the transition from track to hold mode.

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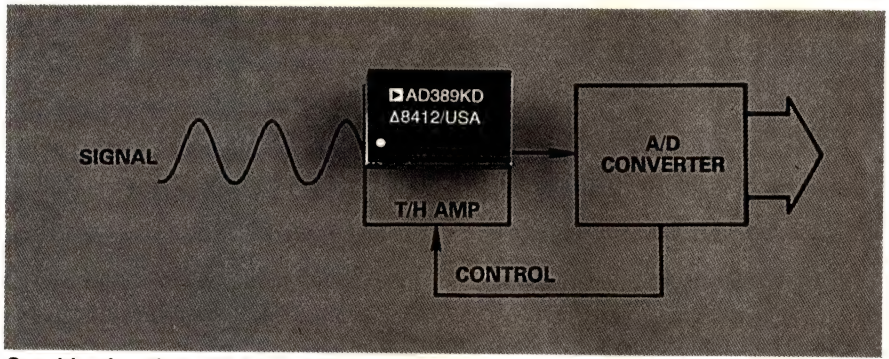
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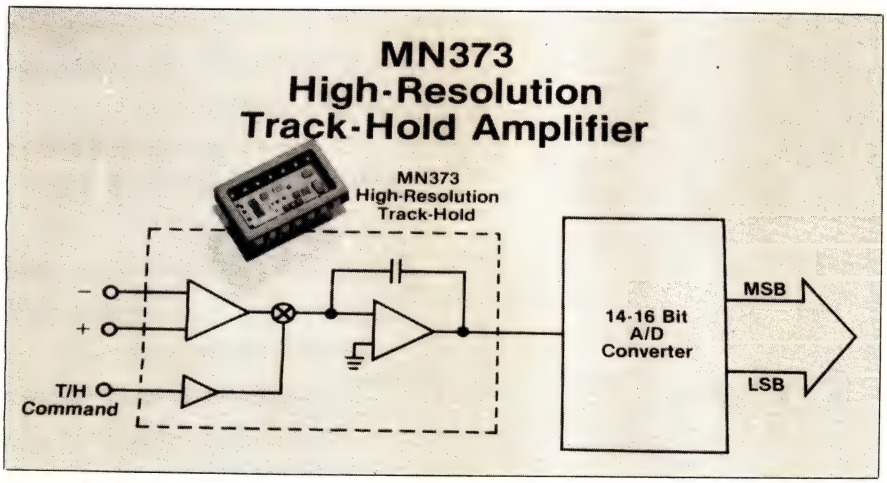
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Capable of mating with 14-bit A/D converters, *this T/H amplifier from Analog Devices boasts 0.001% typ nonlinearity.*



Containing an uncommitted input amplifier, *this T/H amplifier from Micro Networks features specs that qualify it for 14-bit systems.*

owes its origin to the charge the switching circuitry transfers to the hold capacitor during switching. And with the grounded-hold-capacitor configurations of (**a**), (**b**) and (**c**), the amount of charge transferred depends on the voltage on the hold capacitor.

On the other hand, in (**d**)'s integrating configuration the charge is always transferred to a 0V virtual ground and is therefore invariant with input voltage. Hybrid manufacturers have used the integrating approach for years; it's really the only way to overcome the pedestal-variation problem for high-resolution applications. It's evident that monolithic makers' adoption of this technique signals the approach of a new generation of 12-bit-and-better T/H amplifiers.

Before moving on to the new-generation -5320 and -585, consider the two remaining industry standards in **Table 1.** Precision Monolithics' SMP10 and -11 and Harris's 2420 are pin-compatible, low-cost T/H amplifiers, starting at approximately $3 (100). They're faster than the

TABLE 3—FLASH-CONVERTER TRACK/HOLD AMPLIFIERS

MODEL	HTS0010	MN379	SHM7	TP4865	UNITS
INPUT IMPEDANCE	10^5 TYP	10^4 TYP	10^4 MIN	10^{12} TYP	Ω
OUTPUT CURRENT	±40 MIN	±25 MIN	±30 TYP	NO SPEC	mA
GAIN	0.93 MIN	0.92 MIN	0.995 TYP	1 TYP	V/V
INPUT OFFSET	5 MAX	10 MAX	20 MAX	10 TYP	mV
FULL-POWER BANDWIDTH	40 MIN	25 TYP	40 TYP	NO SPEC	MHz
SLEW RATE	250 MIN	300 MIN	NO SPEC	NO SPEC	V/μSEC
APERTURE JITTER	5 MAX	2 MAX	10 MAX	5 TYP	PSEC
PEDESTAL	10 MAX	20 MAX	40 MAX	10 TYP	mV
TRACK-HOLD SETTLING TIME	14 MAX	15 MAX	20 TYP	10 TYP	NSEC
DROOP	100 MAX	5000 MAX	100 TYP	1000 TYP	V/SEC
FEEDTHROUGH	−62 MAX	−60 MAX	−66 MAX	NO SPEC	dB
ACQUISITION TIME TO 1%	15 MAX	20 MAX	25 TYP	25 TYP	NSEC
ACQUISITION TIME TO 0.1%	19 MAX	30 MAX	40 TYP	NO SPEC	NSEC
POWER DISSIPATION	1.75 MAX	1.575 TYP	1.8 TYP	1.4 TYP	W

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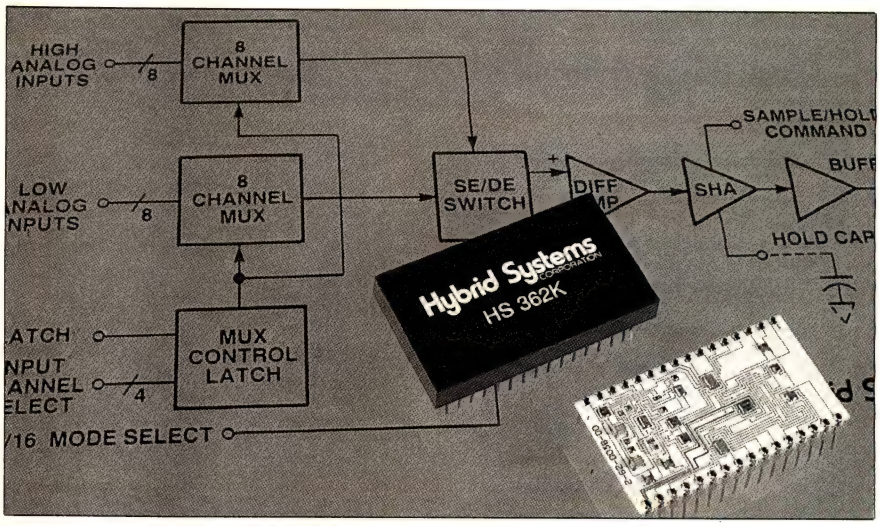
-198 Series: Typical acquisition time to 10 bits (±0.1%) is 3.5 μsec with a 5000-pF hold capacitor, vs the -198's approximately 10 μsec (extrapolated from data-sheet figures for 1000 and 10,000 pF).

According to the manufacturer, the SMP10's and -11's fast acquisition and track-to-hold settling times (7 and 1.5 μsec typ to 1 mV; not specified for the -198) issue from the "super charger" that charges the hold capacitor with 50 mA max. What's more, the output stage's bipolar input results in little variation of droop with temperature—0.05V/sec over temperature vs 0.02V/sec at 25°C for the SMP10, for example. The droop of other designs doubles with every 10°C rise.

Model HA2420-1 is a T/H amplifier with a twist: It's spec'd for performance to 200°C. The specs at 200°C are respectable, indeed. Offset voltage, for example, varies from 4 mV max at 25°C to 6 mV max at 200°C; input bias current only doubles, from 200 to 400 nA max. Droop, however, pays the price of the inevitable high 200°C leakage currents: With a 1000-pF hold capacitor, the 25°C spec of 0.05V/sec max becomes 220V/sec typ at 200°C.

More suitable than these older parts for high-resolution applications, the HA5320 and AD585 use the integrating configuration to eliminate input-dependent pedestal variations. Although pin compatible, the parts offer somewhat different specs. They're both fast: The -5320 specs a 1.2-μsec max acquisition time to 0.1% and 1 μsec typ to 0.01%; the -585 specifies only to 0.01%, 3 μsec max. The -585 specs 0.5-μsec track-to-hold settling time. The -5320 doesn't specify this parameter.

What's more, the two similar parts specify droop differently. They both spec droop with internal 100-pF hold capacitors. The -5320's 25°C figure is 0.08V/sec typ; the -585's, 1V/sec max. The former has typical high-temperature droop of



Serving as the front end *for a 12-bit data-acquisition system, this device from Hybrid Systems handles 16 single-ended or eight differential input channels.*

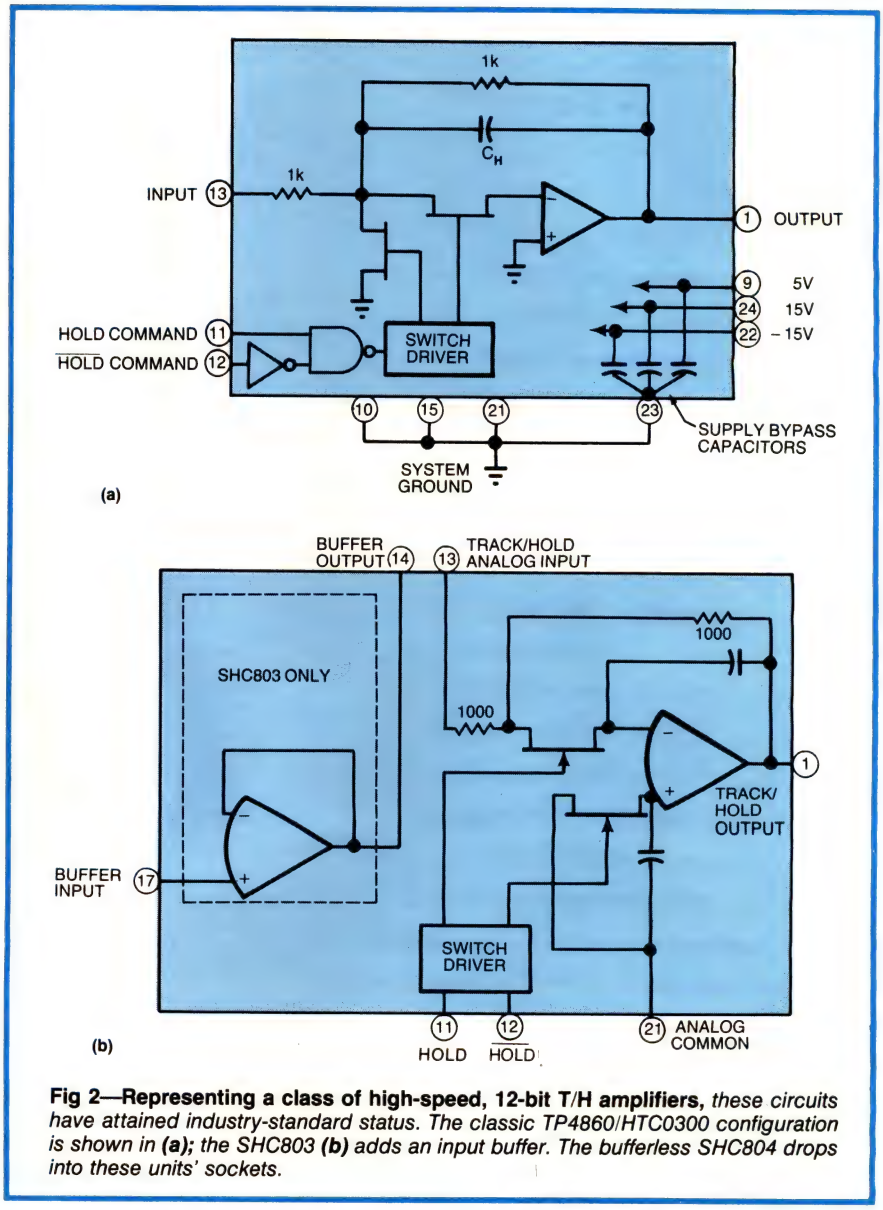
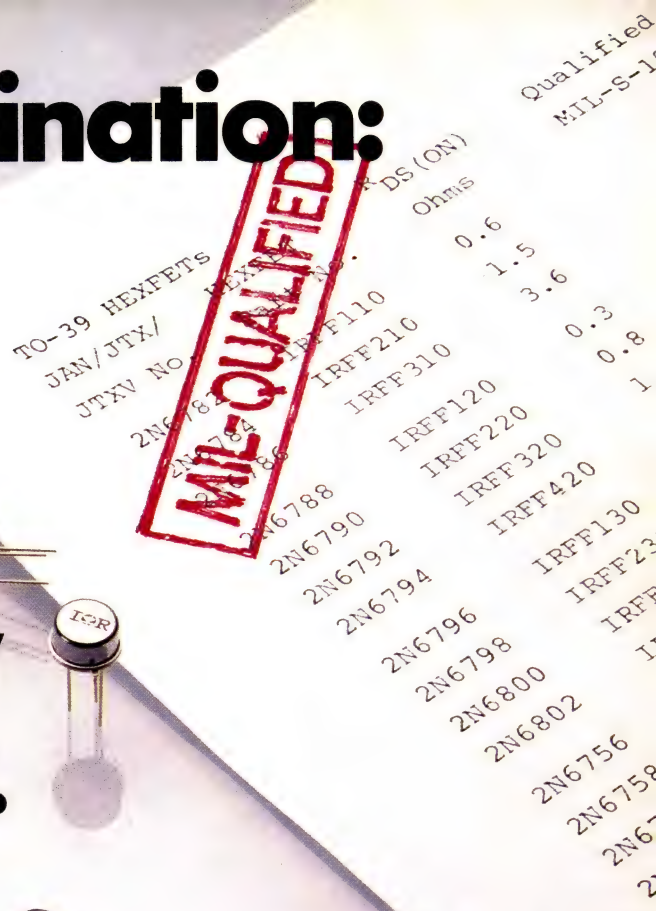


Fig 2—Representing a class of high-speed, 12-bit T/H amplifiers, *these circuits have attained industry-standard status. The classic TP4860/HTC0300 configuration is shown in* ***(a)****; the SHC803* ***(b)*** *adds an input buffer. The bufferless SHC804 drops into these units' sockets.*

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2N6790	IRFF220	0.8	/555	TO-39
2N6792	IRFF320	1.8	/555	TO-39
2N6794	IRFF420	3.0	/555	TO-39
2N6796	IRFF130	0.18	/557	TO-39
2N6798	IRFF230	0.4	/557	TO-39
2N6800	IRFF330	1.0	/557	TO-39
2N6802	IRFF430	1.5	/557	TO-39
2N6756	IRF130	0.18	/542A	T0-3
2N6758	IRF230	0.4	/542A	T0-3
2N6760	IRF330	1.0	/542A	T0-3
2N6762	IRF430	1.5	/542A	T0-3
2N6764	IRF150	0.055	/543A	T0-3
2N6766	IRF250	0.085	/543A	T0-3
2N6768	IRF350	0.3	/543A	T0-3
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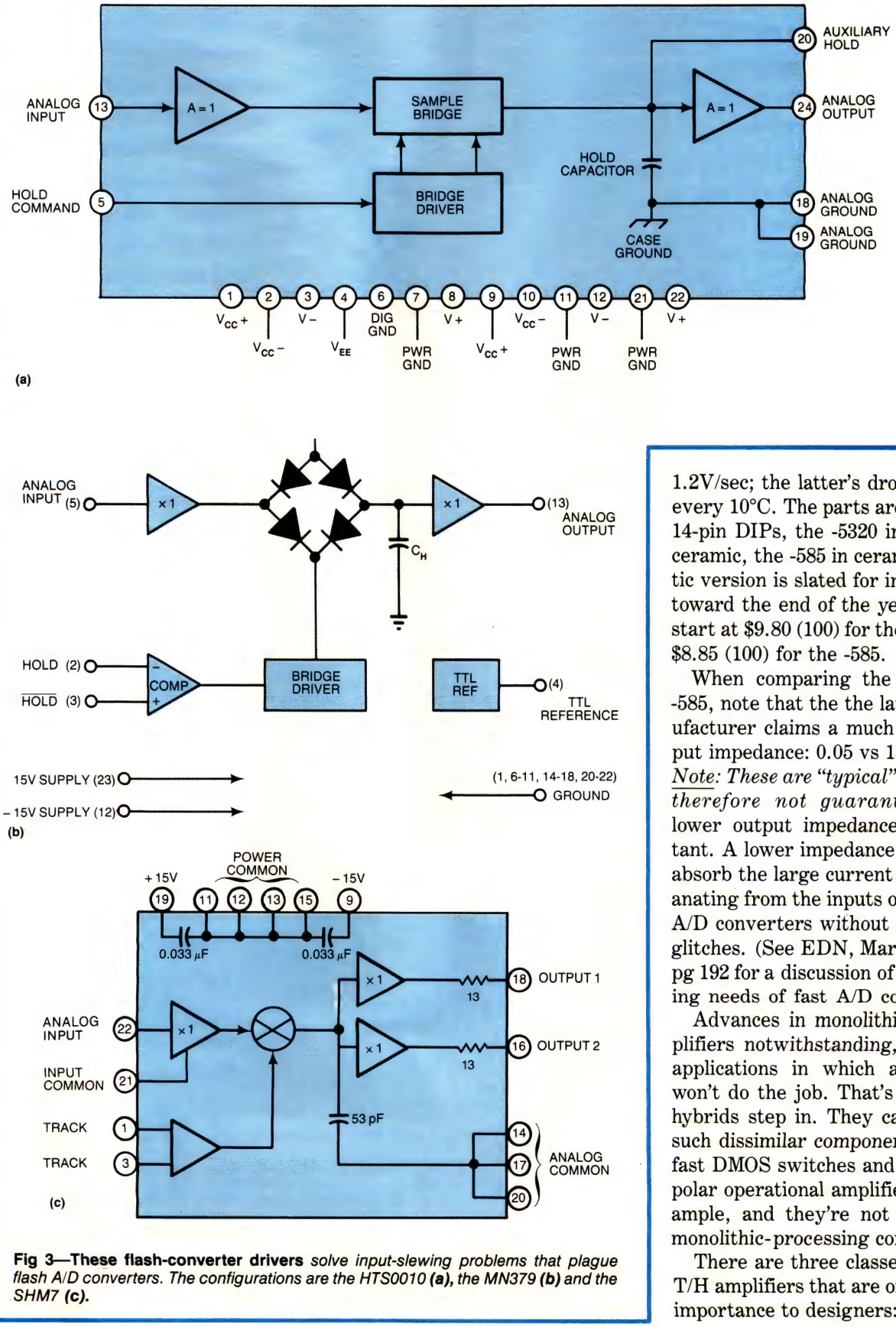


Fig 3—These flash-converter drivers *solve input-slewing problems that plague flash A/D converters. The configurations are the HTS0010* **(a)**, *the MN379* **(b)** *and the SHM7* **(c)**.

1.2V/sec; the latter's droop doubles every 10°C. The parts are housed in 14-pin DIPs, the -5320 in plastic or ceramic, the -585 in ceramic (a plastic version is slated for introduction toward the end of the year). Prices start at $9.80 (100) for the -5320 and $8.85 (100) for the -585.

When comparing the -5320 and -585, note that the the latter's manufacturer claims a much lower output impedance: 0.05 vs 1Ω typ. *(Ed Note: These are "typical" specs, and therefore not guaranteed.)* The lower output impedance is important. A lower impedance driver can absorb the large current spikes emanating from the inputs of some fast A/D converters without generating glitches. (See EDN, March 17, 1983, pg 192 for a discussion of input driving needs of fast A/D converters.)

Advances in monolithic T/H amplifiers notwithstanding, there are applications in which an IC just won't do the job. That's where the hybrids step in. They can combine such dissimilar component types as fast DMOS switches and speedy bipolar operational amplifiers, for example, and they're not subject to monolithic-processing constraints.

There are three classes of hybrid T/H amplifiers that are of particular importance to designers: fast 12-bit

units, 14-bit devices and ultra-high-speed, flash-A/D-converter drivers. The first family (**Table 2**) represents new additions to the industry-standard family comprising Teledyne Philbrick's TP4860 and Analog Devices' HTC0300.

Indicative of industry-standard parts, Micro Networks' MN376 and ILC Data Device's THA05203 follow Philbrick's specs very closely. Acquisition time to 0.01% is the same 200 nsec max; track-to-hold settling time, the same 100 nsec max. Housed in 24-pin double DIPs, the MN376 costs $137 (100), and the THA05203 costs $215 (in units; consult factory for higher quantities).

Staying with the TP4860/HTC0300 pinout, Micro Networks intends to introduce its MN377 toward the end of the year. The part will offer exactly twice the speed of the -376, at the expense of slightly compromised offset, pedestal and droop specs.

Although somewhat less speedy than the preceding parts, Burr-Brown's Models SHC803 and -804 offer several performance advantages. Gain nonlinearity, for example, is cut in half: 0.005 vs 0.01%. Initial pedestal, too, is vastly reduced: 5 vs 20 mV max. Pedestal drift specs 4-ppm/°C max (of full scale) vs 4 ppm typ. The compromise in speed? 350- vs 200-nsec acquisition time, 150- vs 100-nsec track-to-hold settling time, and 160- vs 300V/μsec typ slew rate.

Another improvement touted by Burr-Brown, and borne out by the specs, is the reduced track-to-hold transient: 150 mV max vs 180 mV typ. **Fig 2** shows the classic TP4860/HTC0300 block diagram (**a**) and the -803/804's diagram (**b**). The latter circuit applies compensation to the output amplifier's noninverting input to minimize the transient.

As an example of the addition of features for user convenience, the SHC803 offers an input-buffer amplifier that increases input impedance from the standard 1 kΩ to 10^8Ω. This feature, of course, re-

TABLE 4—14-BIT TRACK/HOLD AMPLIFIERS

MODEL	MN373	AD389	UNITS
INPUT IMPEDANCE	5×10^6 TYP	3×10^3 TYP	Ω
INPUT OFFSET	1 MAX	3 MAX	mV
GAIN ERROR	0.01 MAX	0.02 MAX	%
GAIN NONLINEARITY	0.003 MAX	0.001 TYP	%
SMALL-SIGNAL BANDWIDTH	0.4 TYP	1.5 TYP	MHz
PEDESTAL	2 MAX	4 MAX	mV
DROOP AT 25°C	0.25 MAX	1 MAX	V/SEC
DROOP AT T_{MAX}	7.5 MAX	10 MAX	V/SEC
FEEDTHROUGH	−84 TYP	−74 MIN	dB
ACQUISITION TIME TO 0.01%	9 MAX	3 MAX	μSEC
ACQUISITION TIME TO 0.003%	10 MAX	5 MAX	μSEC

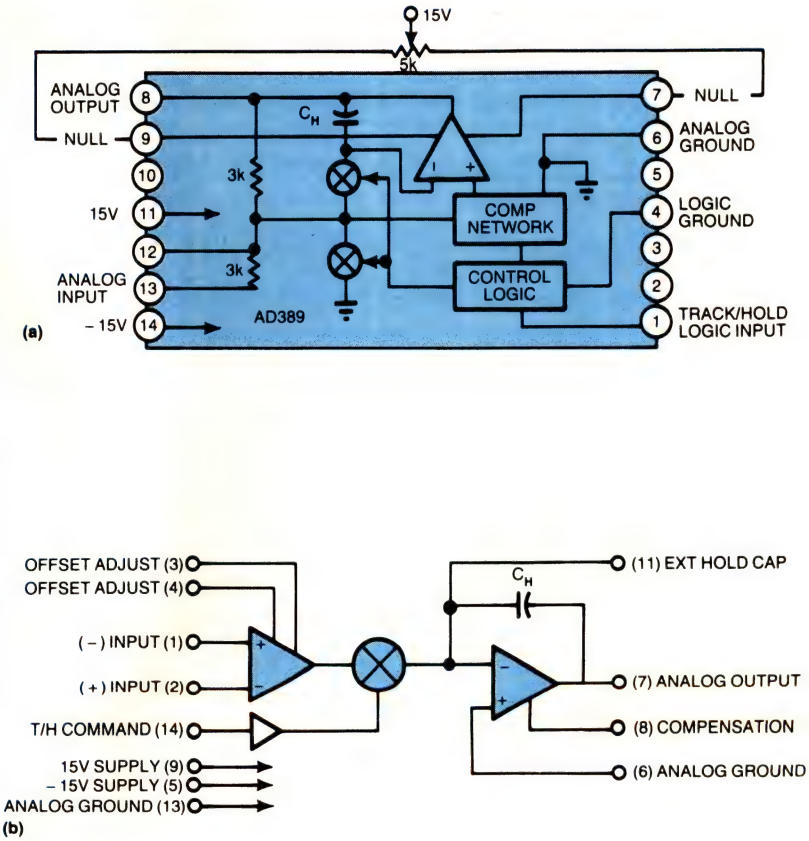


Fig 4—Boasting 14-bit linearity specs, *these T/H amplifiers mate with the highest resolution A/D converters. The block diagrams are for the AD389* **(a)** *and MN373* **(b).**

moves the part from pin compatibility with other industry-standard parts. Enclosed in 24-pin metal DIPs, SHC803 and -804 prices start at $133 and $115 (100).

Taming the flashers

As mentioned, it's often necessary to use a T/H amplifier at a flash converter's input in order to avoid slew-rate-related problems. **Table 3** gives the salient characteristics of four T/H amplifiers specifically designed for flash A/D converters. These are ECL-compatible units, and to attain their speed, they dissipate appreciable amounts of power.

The part with generally the tightest specs (and, accordingly, the highest price) is Analog Devices' $315 (100) HTS0010 (**Fig 3a**). This T/H amplifier, like all the others in this category, specs aquisition time to 1 and 0.1%, about 1 LSB at 7 and 10 bits, respectively. This parameter is quite fast: 15 nsec to 1% and 19 nsec to 0.1%.

The MN379 (**b**) from Micro Networks and Datel-Intersil's SHM7 (**c**) do battle on several fronts. As **Table 3** shows, the former wins on many parameters, but costs $149 vs the latter's $95 (100). Also, the SHM7's droop figure of 100V/sec typ improves on the -379's 500V/sec typ, 5000V/sec max.

Both Micro Networks' and Datel's parts contain some bells and whistles for user convenience. The former has a TTL-reference circuit that makes the part compatible with either ECL or TTL levels. Datel's device has two output-buffer amplifiers, rendering the unit especially suitable for 2-stage A/D conversion using flash A/D converters.

What about Philbrick's entry, the TP4865? Because the part is undergoing data-sheet characterization now, performance details are sketchy. The formal product announcement and data sheets are slated to appear shortly after this article is published. The price is projected to be $90 (100).

Improving resolution

With the advent of several A/D converters offering true 14-bit performance, there's a definite need for supporting T/H amplifiers. At this moment, there are two hybrids of very disparate conception that can fill this need. Note the block diagrams in **Fig 4:** Analog Devices' AD389 (**a**) and Micro Networks' MN373 (**b**) both place the hold capacitor in the output amplifier's feedback loop to eliminate murderous (at 14 bits) pedestal variations.

Table 4 compares the two T/H amplifiers' salient specs. The most striking difference, of course, is the 5-MΩ input impedance of the MN373, compared with the -389's 3 kΩ. The high value issues from the -373's uncommitted input amplifier. The AD389 wins, though, in acquisition time: 3 vs 9 μsec max to 0.01% (12 bits), and 5 vs 10 μsec max to 0.003% (14 bits).

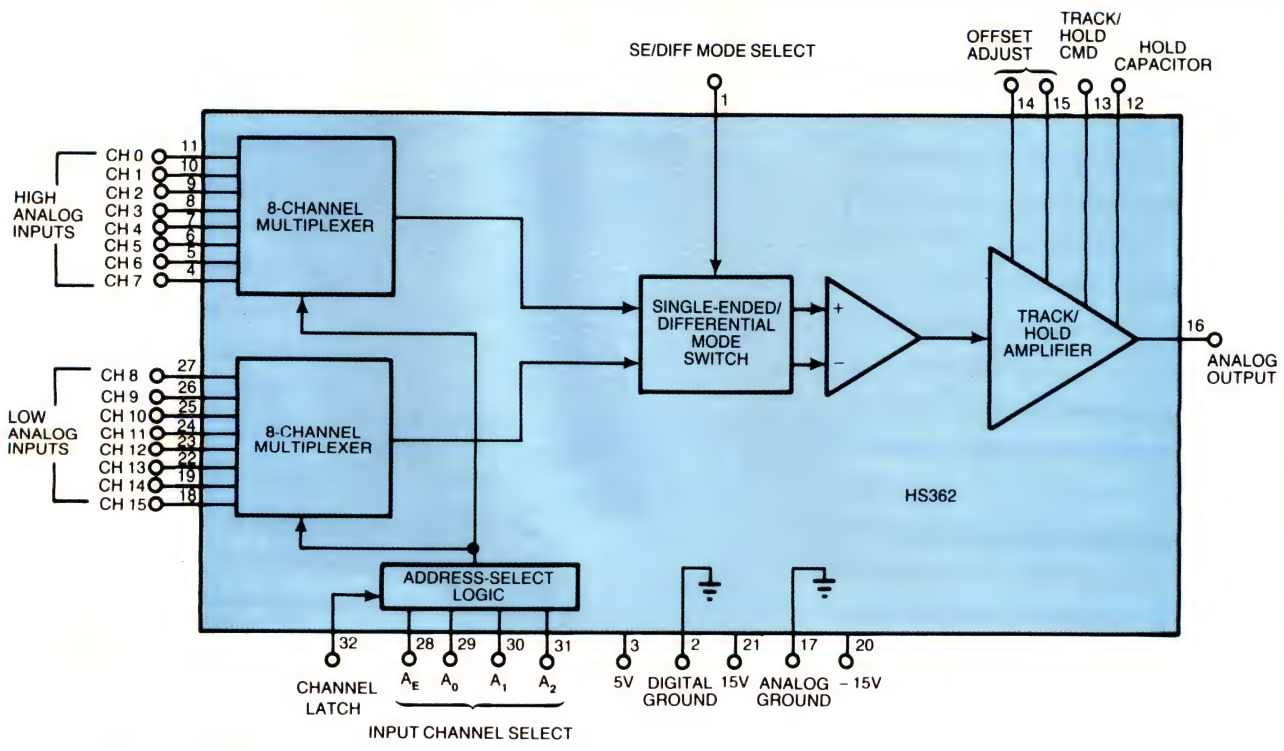


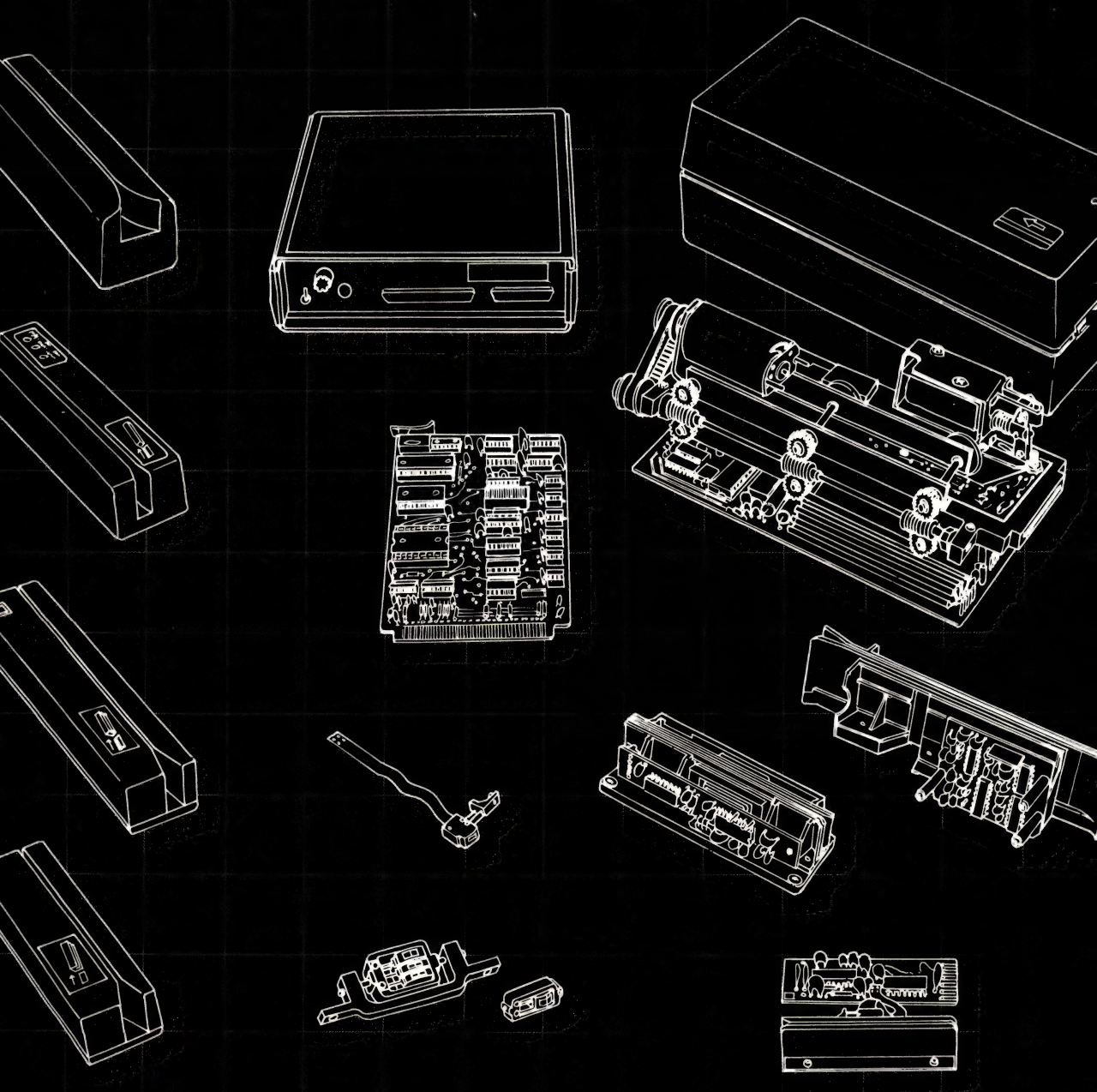
Fig 5—This multiplexed T/H amplifier *allows 16 single-ended or eight differential input channels. It can mate, for example, with a classic 574 A/D converter to produce a 30-kHz data-acquisition system.*

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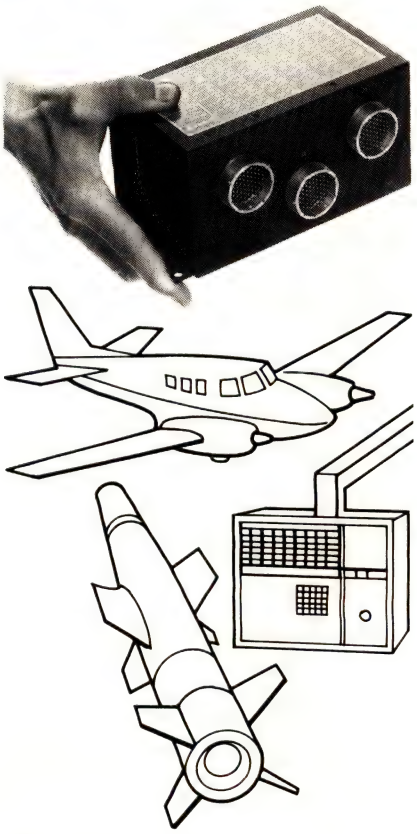
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The -389's acquisition-time victory is perhaps somewhat tempered by the slower track-to-hold settling time: 1.5 vs 0.2 μsec typ to 0.01%, and 2.5 vs 0.25 μsec typ to 0.003%. You should, however, look upon "typical" specs with some skepticism. They're a nonbinding nonguarantee of nothing. Note also that Analog Devices provides maximum figures for these specs (3 and 5 μsec). Micro Networks does not.

Housed in 14-pin ceramic DIPs, the AD389 and MN373 dissipate 500 and 390 mW max and cost $74 and $39 (100), respectively.

T/H amps multiplex inputs

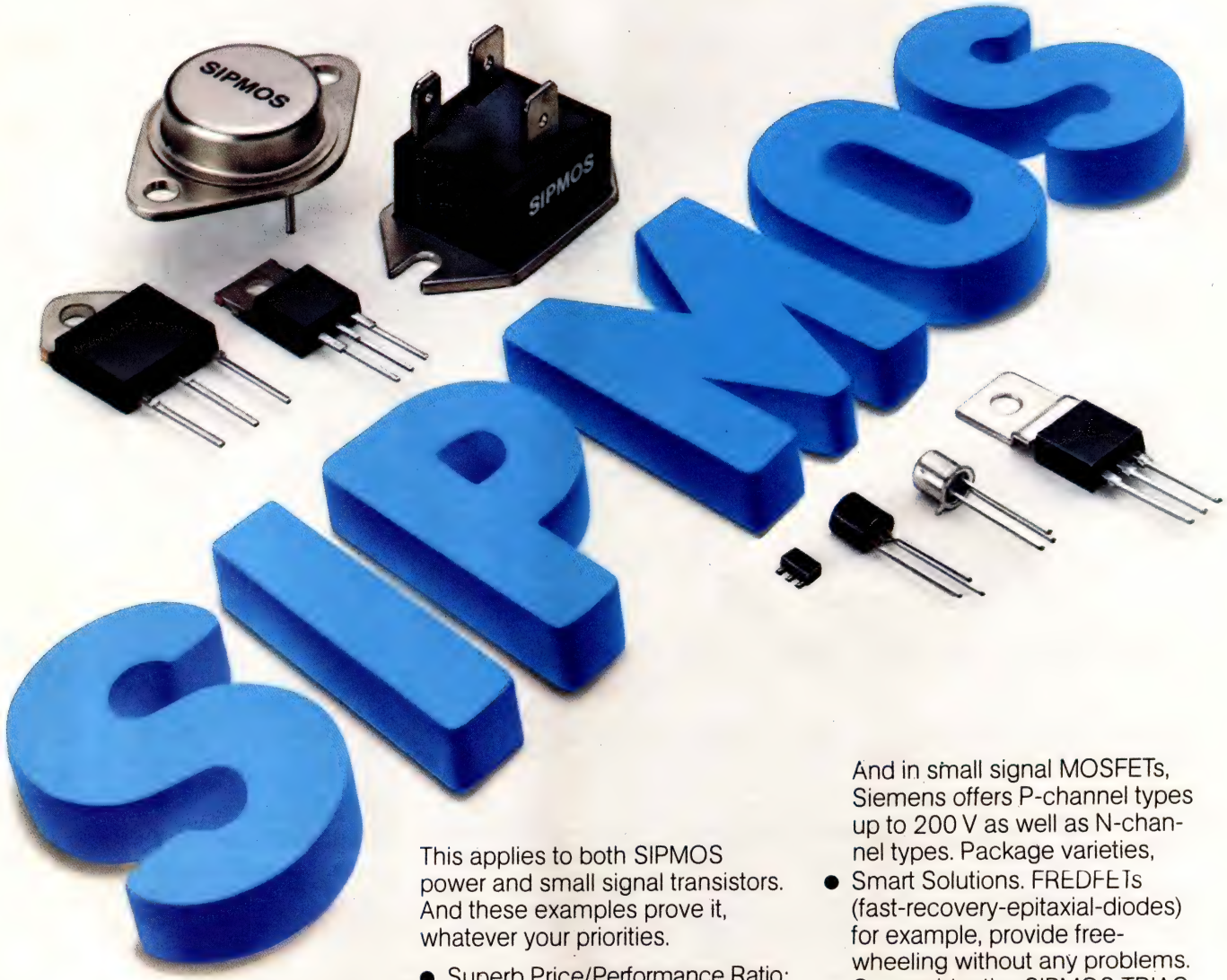
To round out the discussion of DIP-housed T/H amplifiers, consider a multichannel unit offered by Analog Devices and Hybrid Systems. Called the AD362K by the former and the HS362 by the latter, it incorporates two 8-channel multiplexers to accommodate either 16 single-ended or eight differential input channels. **Fig 5** is a block diagram of the device.

The HS362's data sheet indicates certain improvements over the AD362K's specs. Acquisition time is 12 vs 18 μsec max, and the HS unit specs a 600-nsec track-to-hold settling time; ADI's data sheet doesn't furnish a figure for the latter spec. When used with the supplied 2000-pF polystyrene hold capacitor and a 25-μsec, 12-bit A/D converter, the -362 forms a 30-kHz data-acquisition system. Housed in 32-pin triple DIPs, both parts list at $137.50 (100). **EDN**

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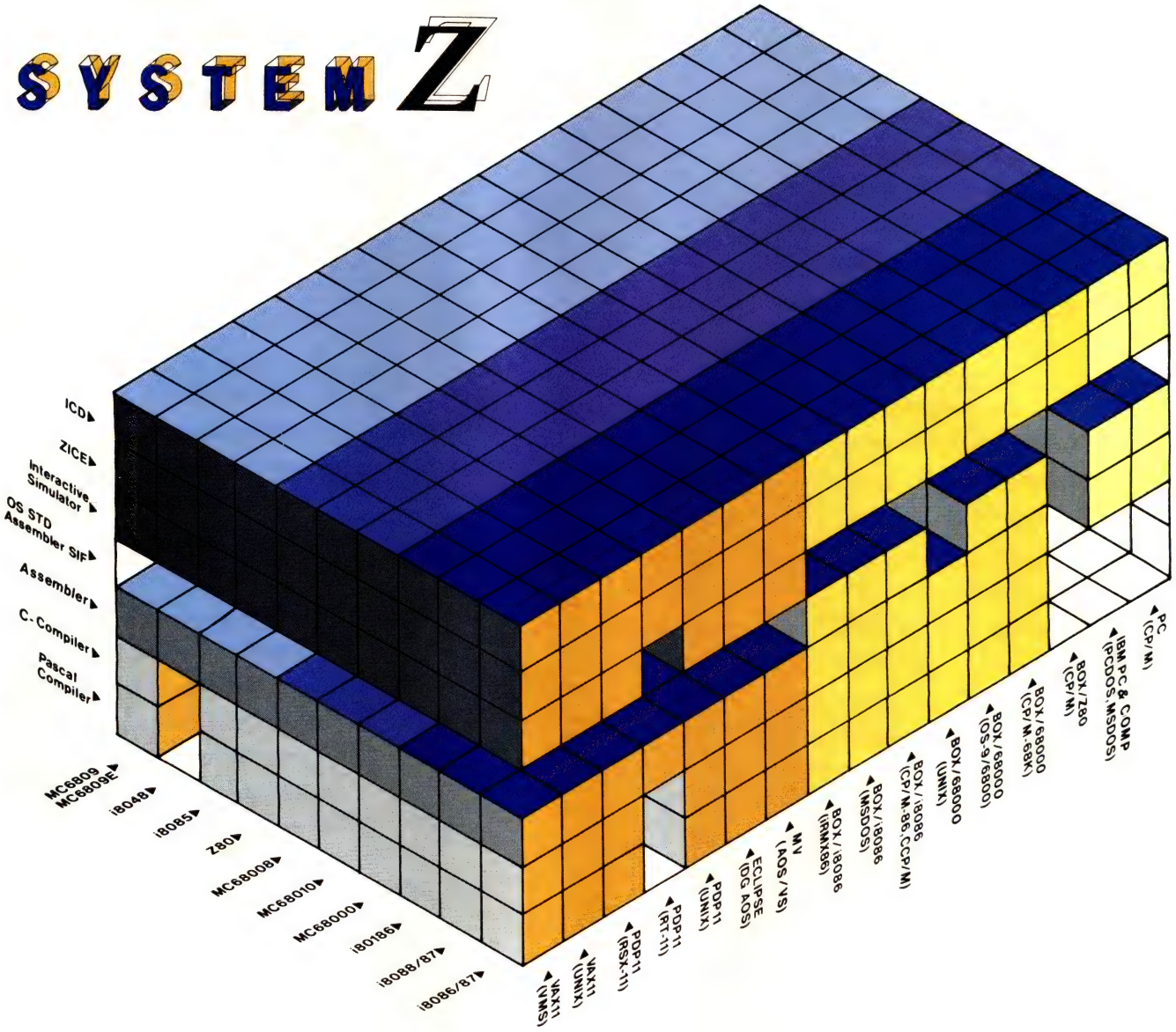
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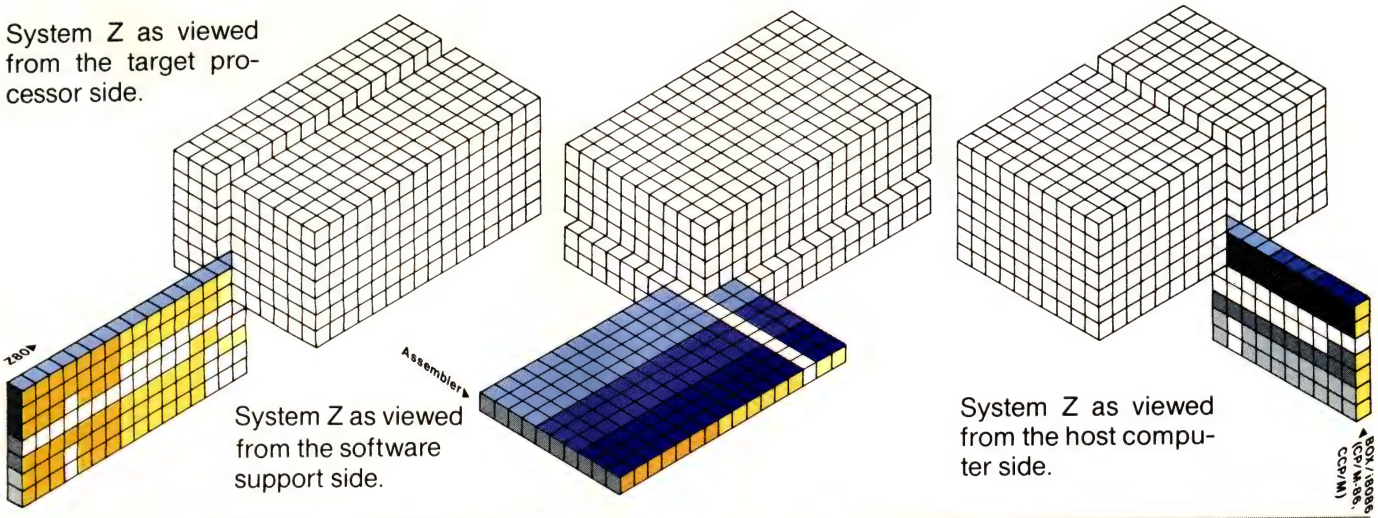
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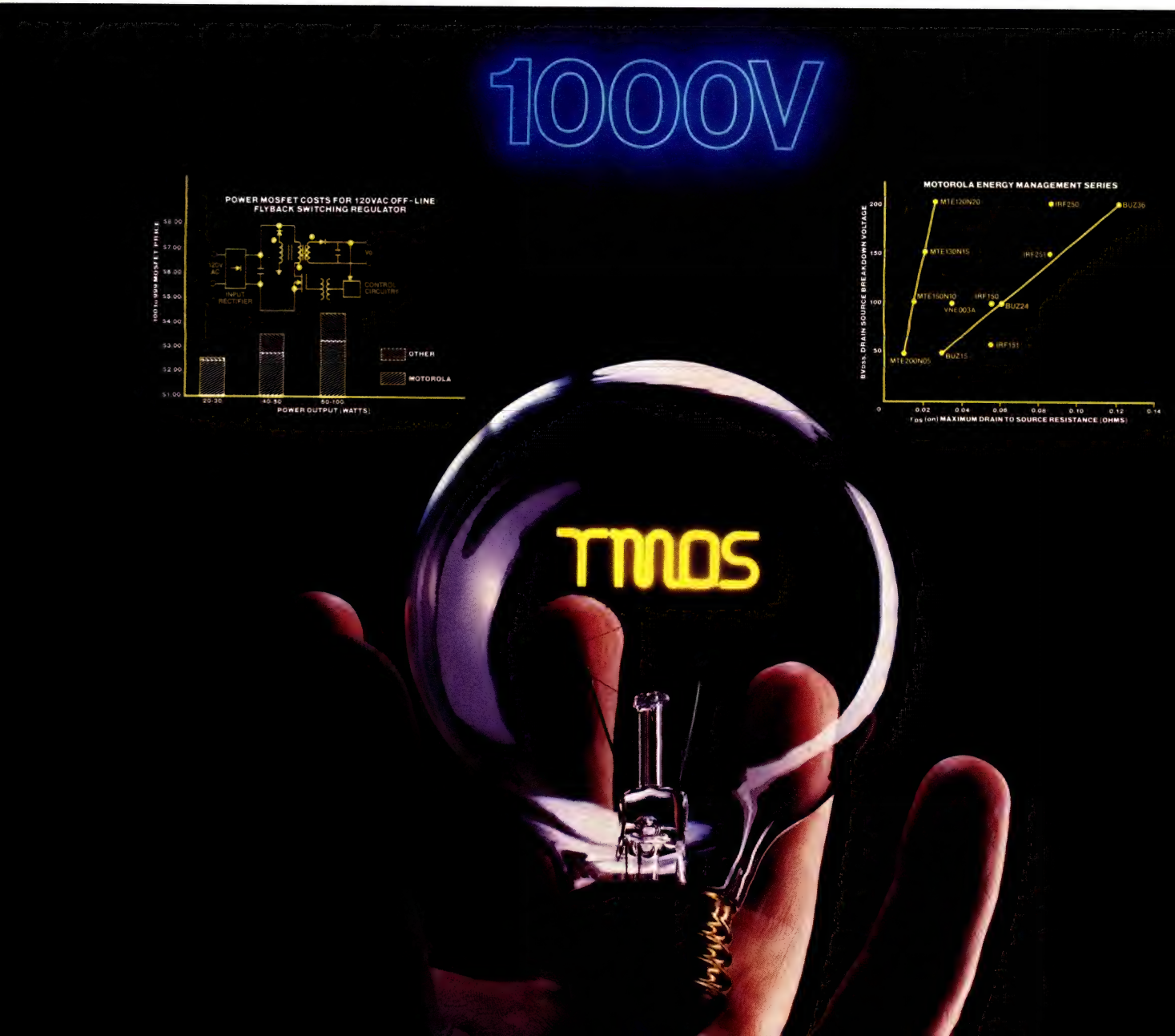
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While power MOSFET prices aren't yet head-to-head with bipolar, lower voltage (up to 500 V) TMOS is rapidly overtaking them. Motorola's new prices are typical examples of rapidly narrowing parity between TMOS and bipolar: The MTP5NO6 5 A/60 V, 0.5Ω TMOS unit has a new 100-up of $1.10.

Comparable bipolar is 69¢.

The MTM5N40, 5 A/400 V 1.0Ω TMOS type is 100-up priced at $3.50.

Bipolar is nearly as much—$3.00.

Our MTP5N40, 5 A/400 V plastic TMOS unit has a new 100-up of $2.25.

Bipolar is $1.60.

And comparable *competitive* MOSFETs remain at 100-ups exceeding $3.25.

Motorola's IRF730 and IRF830, 400 V and 500 V TMOS units sell for $2.50 at the 100-up level.

We'll furnish you either of these devices for $1.75 in 10K quantities. And make your system cost-effective right now.

Half the switching loss at 100 A.

Generally, anything with $r_{DS(on)}$ under 0.1Ω has been considered leading-edge efficient in holding down "on" losses. Taking advantage of the inherent power dissipation capabilities of its "Black Beauty" package, Motorola now offers the MTE-series of industrial-oriented, 500 W, TMOS power FETs with $r_{DS(on)}$ less than half that of others—9 milliohms (0.009Ω) at 100 A.

These 200 A units—first of their kind in the industry—offer a simple, unique and inexpensive way to realize optimized high power from power MOSFET technology. The price of one Black Beauty package is actually less than four TO-3s, in parallel, and installation of one single-sided package is *at least* 50% less.

"On" losses can be lower, in many cases, than bipolar units.

Switching losses are minimized, too, for low-voltage automotive, traction motor, solar and wind power converter/inverter applications. And, of course, they're excellent candidates for very efficient, high-speed switching, regulators, controllers and synchronous rectification.

The MTE200N06 is actually usable to beyond 500 KHz.

Twice the voltage.

With high-voltage TMOS, you can raise high-frequency, series-resonant power supply operating efficiencies to higher-than-you-thought-possible levels.

These 500-volt-to-l-kv MTP-MTM2N/3N/6N units can be directly driven from control ICs—typically capable of 100 mA—to control power supplies up to 100 W. A bipolar design requires 10 times more drive.

This TMOS figure of merit sparkles even more brilliantly when you consider TMOS uses its turn-on source only about 10% of the time for input capacitance charging, not continuously like bipolar.

If you're using one of the new, fast control ICs such as the MC34060 or TL494 sourcing 250 mA or designing slower, less speed-critical circuits, buffer stages can usually be eliminated—an additional saving.

Switching losses are lower with less required heat sinking and drive circuits are simpler. Size and weight of componentry shrinks.

And new applications for 2-phase, 220 V international and 230 V domestic use can now be implemented.

Motorola has 18 high-voltage TMOS units ranging from 550 V to 1 KV in plastic TO-218, TO-220 and metal TO-204 (TO-3).

We're just about the only ones that offer them with any degree of continuity.

All TMOS meets 100 ppm AOQL.



Twice the packaging.

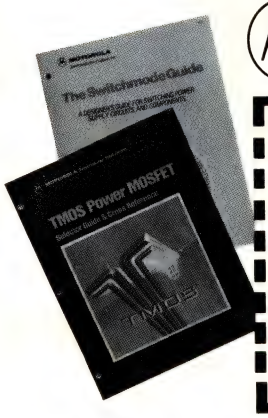
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We'll send you a copy of the new TMOS Selector Guide: a matrix and listing of the most outstanding power MOSFETs in the industry including a cross-index of comparable devices. And we'll include the popular Switchmode™ Guide, a designer's aid to switching power supply circuits and components according to application and performance comparison.

To the first 500 who respond on their company letterheads we'll send a new TMOS Data Book—unquestionably the latest, most comprehensive word on the finest technology of its kind.

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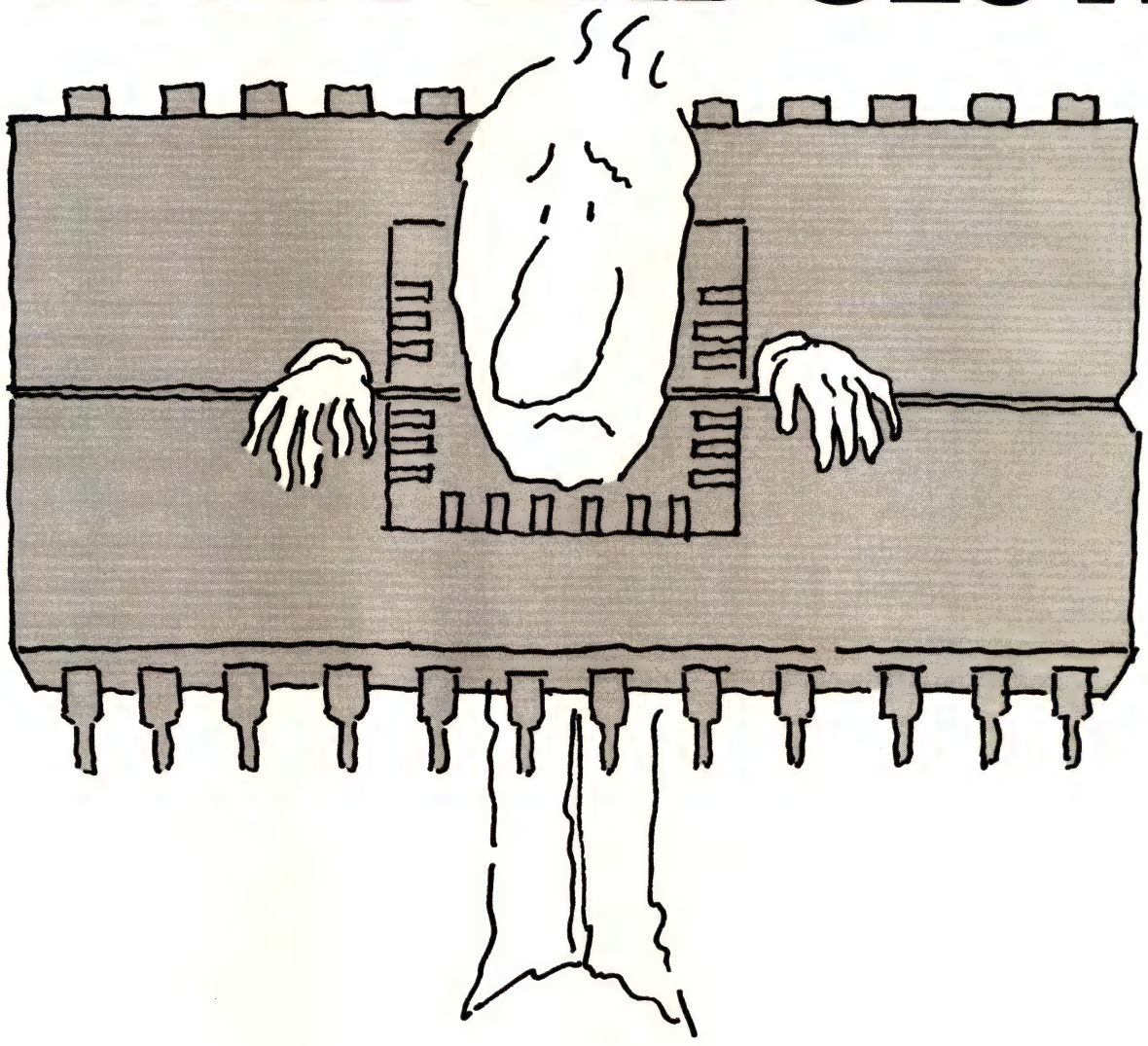
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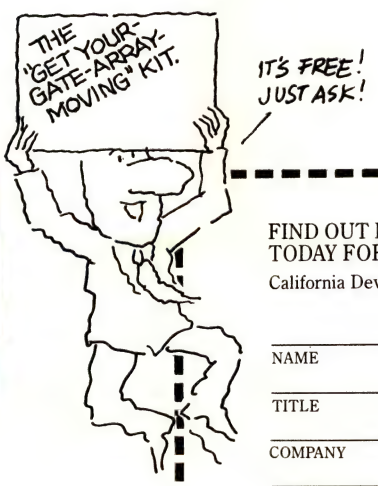


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The 4500 Digital Oscilloscope brings digital performance and accuracy to the analog world.

For capturing and correlating analog and digital signals, the Gould 4500 Digital Oscilloscope stands alone.

Suppose you're debugging a disk drive controller. And you need to look at analog signals generated by digital data. The 4500 can do that job, and others like it, better than any other instrument.

Unsurpassed accuracy and resolution

The 4500's unique acquisition techniques and precise Auto Calibration routine assure you of accurate measurements to within 1% of voltage. With time resolution to 10ns on two separate channels.

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Comprehensive signal processing.

With on board post-processing capabilities, the 4500 lets you easily make a variety of signal comparisons and measurements. For instance, you can add or subtract waveforms to see just how much they differ.

Or you may expand your traces vertically and horizontally for a more detailed look at waveforms.

And for good measure, there's our Signal Averaging feature. Which effectively improves the signal-to-noise ratio by a factor of 16.

One button set-up.

Now, with the 4500, you can concentrate more on the measurement. And less on the set-up.

That's because our Auto Set-up feature sets the controls for an optimum trace display—automatically.

Fully programmable.

For system applications the fully programmable 4500 has GPIB and RS-232-C interfaces for control and data transfer. Plus a separate DMA interface.

There's even an optional floppy disk drive for permanent storage of up to 40 waveforms and set-ups.

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As the leading name in digital storage oscilloscopes, Gould designs every instrument to be clearly the best in its class. And our 4500 is no exception. It's the only one that comes to grips with your analog/digital interface.

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United Kingdom: Gould Inc., Design & Test Systems Division, Hainault Operation, Roebuck Road, Hainault, Essex 1G6 3UE, United Kingdom. Phone: (44) (1) 500-1000.

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The 4500 Digital Oscilloscope captures and correlates analog and digital signals with push-button convenience and unequaled performance.

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CIRCLE NO 51

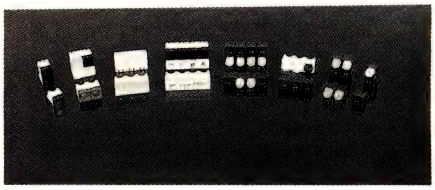
Novel packages for LEDs and LED arrays solve front-panel backlighting problems

PCT and PCV Series LEDs and LED arrays come in housings that can be chained together to create any desired array size for mounting parallel to the plane of a pc board. This chaining capability solves the traditional problems of backlighting and legend illumination.

Though many LED manufacturers offer standard array sizes (1×4 or 2×4, for example), you might have requirements that don't match these standards. With the PCV and PCT devices, you can readily configure a 2×5 array by combining standard parts. When interlocked, the array looks like a molded part. The lens or diffuser has the same capability.

All devices are available in T-1¾-size packages, but some are offered in T-1 housing styles. The injection-molded packages feature a base material that carries a 94V-0 UL rating. Because the material is flame retardant, the devices accommodate wave-soldering processes.

The LEDs are available in four colors, which you can mix within the same array. The arrays can be supplied with current-limiting resistors where required, and they operate from a 110V ac source in some cases. Standard brightness levels range from 2 mcd (for indoor operations) to 500 mcd (for visibility in direct sunlight). A 1×4 array typically costs $1.20 (1000), with a lens adding $0.40 per part. The lenses are available with optional custom legends.—***Maury Wright***



Simplify array customization *for panel-backlighting applications with the PCV and PCT Series of packaged LEDs. The devices provide selectable brightness and a range of color mixes.*

Ledtronics Inc, 4009 Pacific Coast Hwy, Torrance, CA 90505. (213) 373-5437.

Circle No 745

Thin-film-technology read/write heads directly replace ferrite heads

Most thin-film read/write heads have 2-wire coils, and most ferrite heads have 3-wire coils. Cyber 400 Series units come with a center tap that makes them plug-compatible replacements for the minicomposite and minimonolithic ferrite heads currently used in Winchester disk drives. As a result, you can install Cyber 400 Series heads in most Winchester disk drives without modifying the drive's read/write circuitry. The heads ensure complete compatibility with the standard 3-wire SSI 117 and SSI 104 and other microchips designed for the ferrite heads often used in 8-, 5¼- and 3½-in. Winchester disk drives.

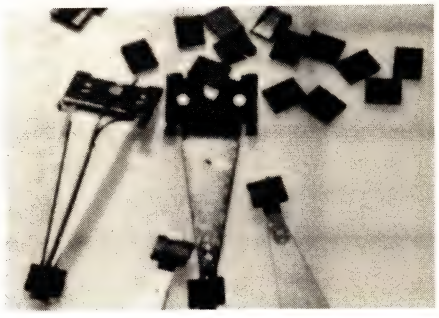
Cyber 400 heads feature 24 turns and a 30-μm gap in a double-layer Hepstead-type coil. The coil resistance is 20Ω max. The inductive thin-film transducer is deposited directly on a ceramic slider that has been machined to achieve extremely stable flight characteristics. The head flies at 12 μm with a 15g load force.

Using thin-film deposition gives the heads the performance-consistency characteristic of semiconductor devices.

The heads come in versions suiting four track densities to match the drive's requirements: 1200, 960, 800 and 500 tpi. At each density, the Cyber 400 Series heads afford resolution in excess of 70% at flux densities ranging from 8000 to 15,000 fci, depending on the characteristics of the media and read/write channel.

Outside track overwrite is better than −26 dB with a 50-mA write current. The head flies at 12 μm with a 15g load force.

The heads cost $100, and the minimum order is $1000 for 10 heads. Call the manufacturer for larger volume pricing or specifications of higher recording densities.



Advanced plating, sputtering, photolithographic *and lapping technologies combine to produce high volumes of thin-film read/write heads that can directly replace existing ferrite heads in small Winchester drives.*

—***Ed Teja***

Cybernex Corp, 6580 Via Del Oro, San Jose, CA 95119. Phone (408) 224-8010.

Circle No 743

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CAE SYSTEMS
CIRCLE NO 52

Rugged 4½-digit DMM reads 1500V dc, 1000V ac

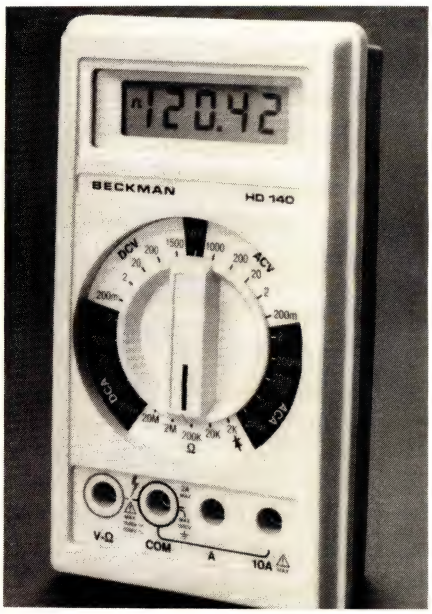
The Model HD140 handheld DMM is the only 4½-digit unit available in portable, ruggedized form. The $259 unit is waterproof, contamination-proof, and can withstand a 10-ft drop. It qualifies under Type II enclosure styles A and B of the MIL-T-28800B specification for test equipment.

The designers have reinforced the meter by shock-mounting its LCD, enabling it to withstand rough handling or dropping. Elastomeric (rubber) strips reside between the glass of the display and the pc board. Gold conductors pierce the elastomeric strip vertically. These conductors remain in contact with the pc board and conductors on the LCD's glass even when jolted.

The meter's single-knob switch is a proprietary design. The switch doesn't employ traditional wafers. Instead, the knob incorporates a cam that causes conductors to make contact at the various switch points. This means that the contacts of opened switches are not continuously under pressure and scraping against another surface. Tests show that the switch has a life of greater than 100k cycles.

A gasket seals the switch and all exposed surfaces to protect the meter from water and other contamination. The effects of water penetrating the unit's case are obvious, but dust contamination can also affect accuracy or cause damage to an instrument. A foam package restrains the battery to prevent its failure under shock.

The HD140 has some impressive measurement specs. When measuring dc voltage, the meter maintains an accuracy of 0.07%, ±2 least significant digits, at the highest (1500V) range. Lower ranges drop the figure to 0.05%. Circuitry protects the meter from overvoltage transients of less than 6 kV. Over all ranges, the unit's input impedance specs at 10 MΩ.



Durability and a 4½-digit display *combine in the HD140 handheld DMM to serve industrial and military applications.*

For ac voltages, the top range specs 1000V with true-rms capabilities at frequencies of 10 kHz and less. The DMM attains ac accuracy of 1%, ±40 digits on a 200V, 10-kHz signal. Lowering the frequency to 5 kHz brings the figures to 0.5%, ±30 digits.

In ac and dc modes, the meter measures current to 10A. The 10A input has separate overload protection to 10A, while the lower ranges withstand 2A at 600V. The top resistance range is 20 MΩ, and the unit has an instant-continuity function as well as an in-circuit diode test. The HD140 has a 1-yr calibration cycle and operates from a 9V battery.—***Maury Wright***

Beckman Industrial Corp, 630 Puente St, Brea, CA 92621. Phone (714) 773-8198.

Circle No 746



Question: How Do You Mate a 300 Pin Connector? Answer: With Great Difficulty! Solution: Hughes Low Insertion Force (LIF) Connectors.

L I F to the rescue! Our contacts are designed with super low forces—1½ oz. per contact. Connector breakage is thus eliminated due to the incredible ease of mating. And yet, good contact wiping action is maintained.

At the same time, there's no loss of electrical integrity, even under the stresses of vibration and shock, as evidenced by the use of our L I F 296-pin P C connector in the computer processor module of the B-1B.

The new Hughes L I F connectors do the job easily, quickly, efficiently—with no mating gadgetry. So if your application requires hi-density, multi-pin P C connectors, let us solve your L I F problem.

It could save you an awful lot of trouble.

For more information, contact your Hughes representative or phone Bob Torres at 714-660-5829. Or write Hughes Aircraft Company, Connecting Devices Division, 17150 Von Karman Avenue, Irvine, CA 92714. In Europe: Hughes Microelectronics, Ltd., Clive House, 12/18 Queens Road, Weybridge, Surrey KT13 9XD, England.

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CIRCLE NO 53

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CAESYSTEMS
CIRCLE NO 54

80286-based processor board improves PC performance

The IBM Personal Computer is finding its way into many scientific and engineering applications. Sometimes, however, the computer can't deliver the processing power required by a potential application. The PC286 processor board confronts that problem by furnishing a plug-in-and-run, 80286-based CPU board that runs at 4, 6 or 8 MHz. The new CPU completely replaces the 8088 μP, yet it maintains IBM bus compatibility, running existing PC - DOS software without any modification.

On-board circuits perform DMA arbitration, address decoding and data conversion between the 16-bit 80286 μP and the 8-bit system bus. A socket supports use of an optional 80287 math coprocessor for applications that require significant amounts of floating-point math.

To take full advantage of the 80286 μP's capabilities, the board comes with 256k bytes of 3-port RAM (expandable to 1M byte). The CPU, an on-board expansion connector and the PC's bus all have independent access to the memory.

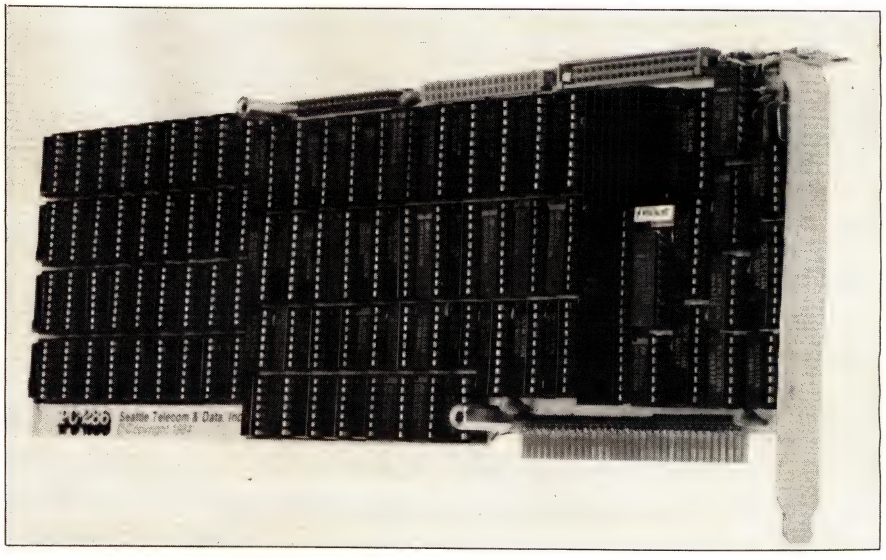
If 1M byte isn't enough memory for your application, the expansion connector lets you add more memory via a piggyback card which supports 512k to 2M bytes of RAM. An on-board latch lets the PC bus access the additional memory in 1M-byte increments, giving peripheral devices, such as DMA disk controllers, access to the full 16M bytes of address space.

In addition to providing for additional memory, the expansion connector makes available to the system fully buffered address, data and control lines from the CPU, as well as DMA request and acknowledge lines. Consequently, the expansion connector furnishes a means of communication between the bus and the expansion card located anywhere in the 24-bit address space.

Production quantities of the PC286 will be available in August. Single-quantity pricing begins at $2395.—***Ed Teja***

Seattle Telecom & Data Inc, 2637 151st Pl NE, Redmond, WA 98052. Phone (206) 883-8440.

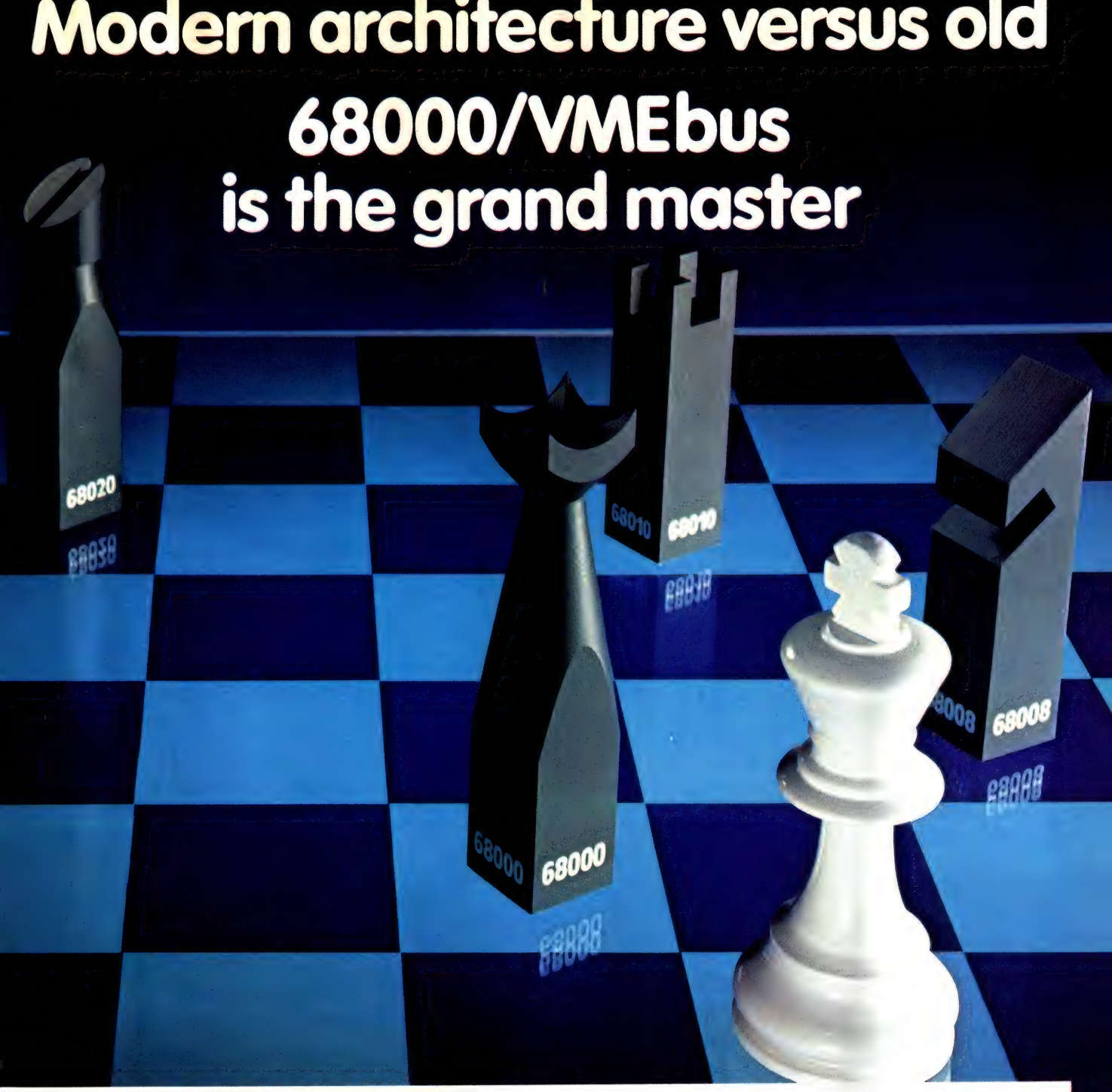
Circle No 740



Plug the PC286 board into an IBM PC *to obtain the increased performance of a system containing an 80286 CPU.*

Modern architecture versus old

68000/VMEbus is the grand master



Check architecture – not just benchmarks!

When you do you'll find that the Philips/Signetics S68000 microprocessor checkmates the rest. With 32-bit architecture and direct 16-Mbyte linear addressing, programmers love it. No wasted moves to overcome restrictive registers and addressing modes. A modern architecture that speeds development and gets your system on the market sooner.

And what's more, when you upgrade your systems you use the same software thanks to the true architectural compatibility within the S68000 family. A choice of 8 or 16-bits, with 32-bits just a move away. A family that lets you build any system right from simple controllers up to the most complex multiprocessor configurations. The edge you gain with S68000 architecture will be clinched in the end-game by the right bus specifications. VMEbus is the one that will keep you ahead right into the '90s and beyond, offering total compatibility through 8, 16 and 32-bits without unhandy 'bridges'.

The 68000/VMEbus is supported by full ranges of chips, boards, target software and software development tools.

For proof, contact

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PHILIPS

CIRCLE NO 191

Bipolar FIFO memory achieves 35-MHz speed

Taking advantage of an innovative, proprietary circuit design that doubles internal data-processing speeds, the 57/67413 first-in, first-out (FIFO) memory increases the maximum operating speed for such devices to 35 MHz. This performance opens up new areas of application in digital signal processing, floating-point processing and video and image processing.

You can also apply the device's added speed to higher speed tape and disk controllers and data-comm systems. In special cases, the device can replace a high-speed RAM.

The specialty of all FIFOs is data-rate matching between devices or systems, and the 67413's dc to 35-MHz shift-in/shift-out rate permits the widest range of possibilities. Organized as 64 words×5 bits, inputs and outputs operate asynchronously. The I/O pins are placed directly opposite each other on the package for ease in cascading. Parts can be cascaded to any word depth or, using a few external logic gates, any bit width. The unit also has output-enable, half-full, almost-full and almost-empty flags. The almost-full and almost-empty flags go High at 56 words and eight words, respectively, with decoding performed by the half-full flag.

The device is available in versions for the military temperature range (−55 to +125°C) as the 57413 or the commercial temperature range (0 to 75°C) as the 67413. The military part's shift rate is 25 MHz max with a power supply of 5V, ±10%. The 67413 has a 35-MHz shift rate using a 5V+5% supply. Data-fallthrough times for the 57413 and 67413 are 750 and 650 nsec, respectively.

Packaged in a 20-pin ceramic DIP and costing approximately $38 (1000), the 57/67413 has 3-state outputs, is TTL compatible and provides 24 mA of output drive. Maximum supply current over temperature specs at 240 mA.

—William Twaddell

Monolithic Memories Inc, 2175 Mission College Blvd, Santa Clara, CA 95050. Phone (408) 970-9700.

Circle No 742



Extending the speed range of FIFO memories to 35 MHz, *the 57/67413 3-state, 64×5 FIFO opens up new applications in signal and video processing. Moved into a 20-pin package, the device features output-enable, half-full, almost-full and almost-empty flags.*

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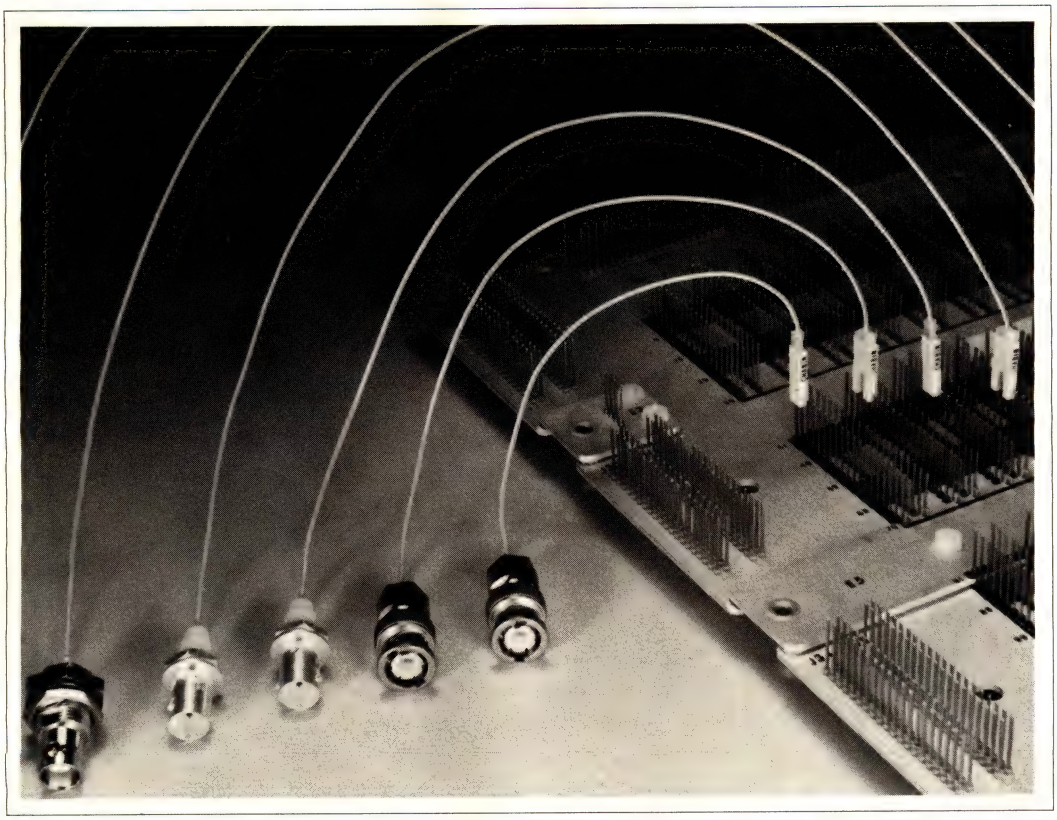
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CAE SYSTEMS™

CIRCLE NO 55

CHABIN BNC-TLA™ ...EASY TO ROUTE, PLUGGABLE BNC DATA TRANSFER LINES



Chabin's unique BNC Transmission Line Assembly (TLA) makes life easier whether you're in design, manufacturing or field service for applications requiring internal BNC/coaxial cables.

Now there's an alternative to the use of large, cumbersome, shielded coax that's tough to thread through your system.

And forget about your worries of stripping and soldering to obtain a strain relief to the pin field. We've added our strong, reliable Series 100 and 200 connector which mates with .025" round or square posts.

When the connector has to be removed, it can be done with ease... again and again.

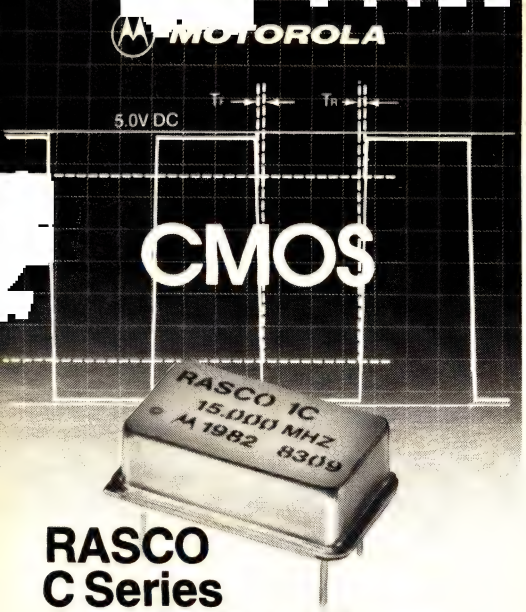
We've also incorporated a subminiature, drain wire coax that was specially designed for computer and instrumentation applications. It's ideal when low noise, controlled impedance and consistent propagation delay transmissions are top priority.

If your internal wiring calls for coaxial cables, Chabin makes your job easier.

Call or write us today for complete information. **CHABIN CORPORATION,** 890 Fortress Street, Chico, CA 95926; (916) 891-6410, TWX: 910-536-1001.
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Low Current Drain, compatible with high speed CMOS logic, capable of driving such devices as the 74HC series with highly capacitive loads.

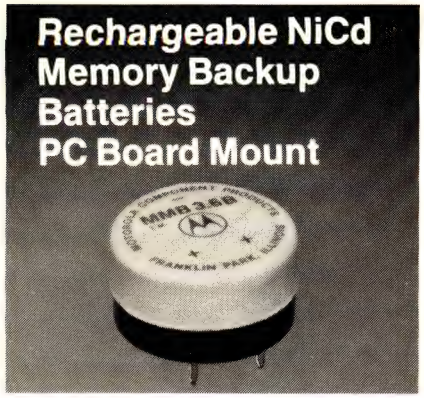
Precise Rise And Fall Times, rigidly controlled so as to meet the stringent requirements of high speed CMOS microprocessors.

High Reliability — drastically reduced internal parts count, fewer interconnects, thus greatly improved MTTF.

Enable/Disable optionally available. Contact factory for application information.

All-Metal, Welded Package — provides full hermetic seal for resistance to heat/humidity extremes. Pin 7 is case ground for improved shielding, helping to meet FCC EMI specifications.

CIRCLE NO 198



MMB series batteries feature a unique, patented electrode configuration that minimizes the "memory effect." NiCd MMB batteries are thus capable of maintaining a cycle of constant trickle charge when power is on, slow discharge when power is off, with a typical life expectancy in excess of 5 years.

Easy PC board mount — can be wave soldered (5 sec. max) directly to the printed circuit board; no tie-down straps are needed. MMB batteries take up less than 1″ diameter board space and have low seated height (only .524″ for 3.6V models).

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MOTOROLA INC.
Components Division
2553 N. Edgington
Franklin Park, Ill. 60131 312/451-1000
TWX: 910-255-4619 Telex: 4990104

CIRCLE NO 199

Fluorescent color filters enhance LCD brightness

These fluorescent - illuminated LCDs form a bright multicolor display, overcoming the dull appearance and washout problems that have historically kept liquid-crystal technology out of many applications. Though more colorful negative-mode displays have put some life into LCD products, they've done so at the expense of high power consumption. These color LCDs feature a hybrid configuration that enhances presentation capability without exacting a power-consumption penalty.

The displays use the transflective properties of positive-mode reflective displays to retain vivid presentations in the reflective mode for bright ambients. The key to color brightness, however, comes from transmissive fluorescent color filters. Unlike ordinary filters, fluorescent filters convert higher energy light into the desired colors.

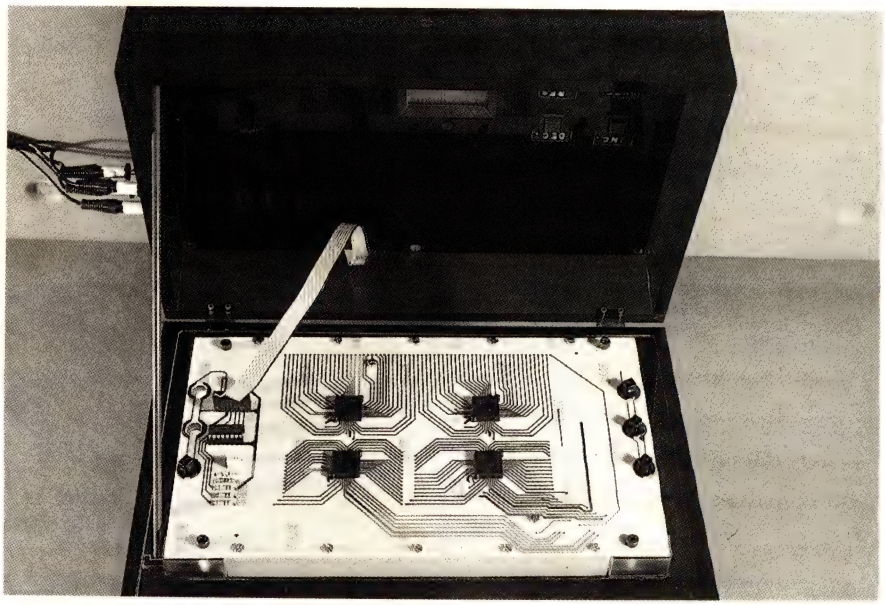
The displays are available in a wide range of hues, and you can specify multiple colors within the viewing window. Yellow, red and orange are the most efficient colors for fluorescent filters. Blue and green also make for attractive displays, but they do *not* perform as well in bright ambients.

Low-power performance stems from the use of a proprietary light-pipe design that provides maximum efficiency with minimum light loss. You can evenly illuminate a display with a 5×7-in. active area with less than 3W of incandescent lighting. According to the manufacturer, this figure represents one-third to one-fifth the power required by competitive units. Light-pipe efficiency allows a single lamp in any corner of the display to illuminate the display's entire active area.

Though the product is basically custom in nature, the manufacturer projects a $25 price for a 4-digit module.—***Tom Ormond***

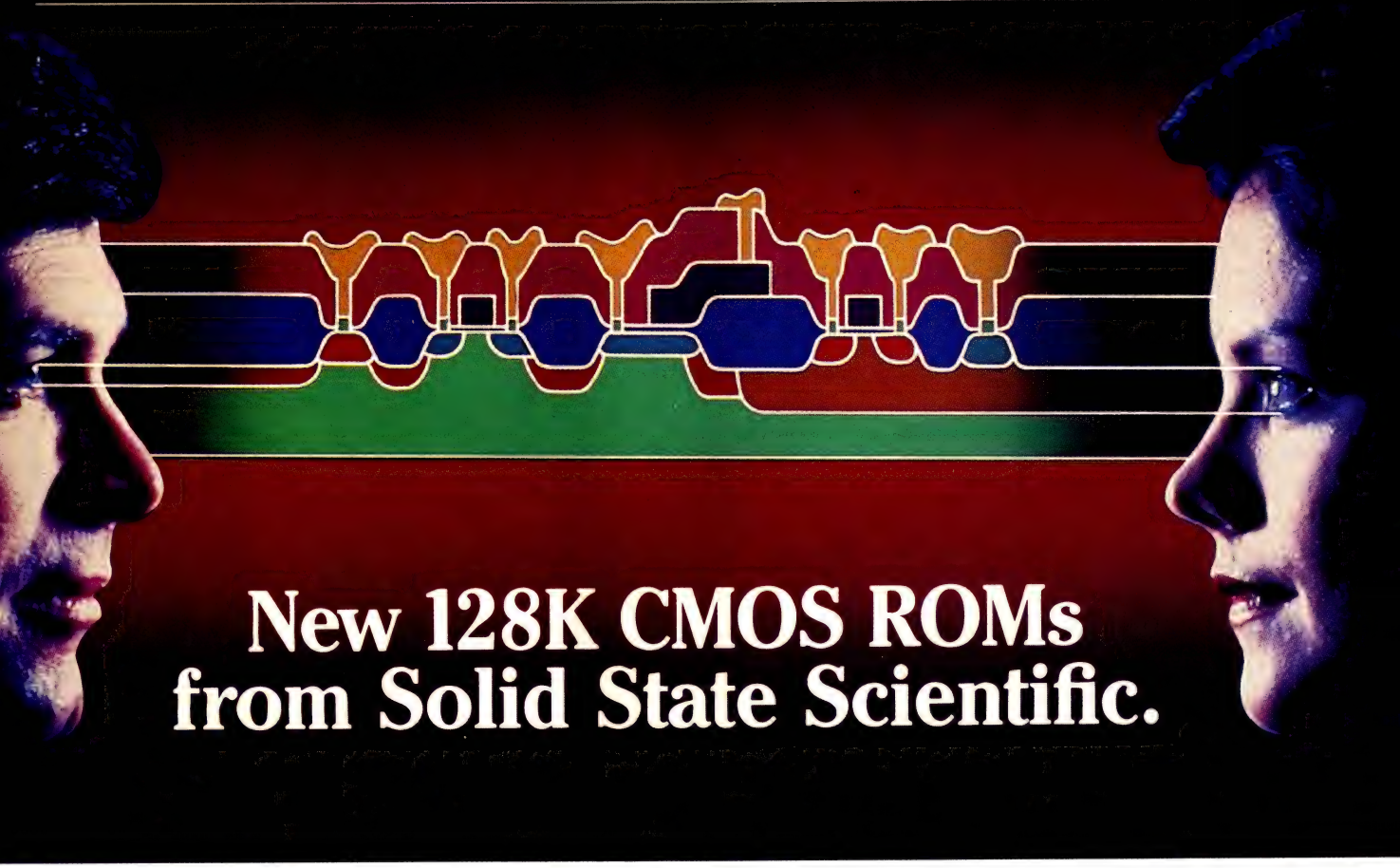
Printed Circuits International Inc, 1145 Sonora Ct, Sunnyvale CA 94086. Phone (408) 733-4603.

Circle No 741



Reducing the high current and washout problems *that have historically plagued the technology, these LCDs use transmissive fluorescent color filters to achieve enhanced color performance at low power.*

CMOS is a Solid State of mind.



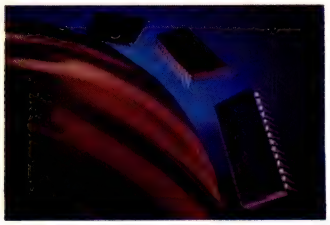
New 128K CMOS ROMs from Solid State Scientific.

Fast access times (100 ns max.)
Faster system execution.
Fastest turnaround times in the business.

Solid State Scientific has a new 128K CMOS ROM. The 23C128. It's extremely fast—75 ns typical or 100 ns worst case. So you can use it with the world's fastest microprocessors. It has the low power and high reliability of our state-of-the-art CMOS technology. It's available now at prices that make it as cost-efficient as it is technically superior. Production volumes take only 7 weeks, prototypes just 3 weeks.

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If you're using NMOS ROMs, our new 23C128 can give you far better speed and reliability. If you're using EPROMs, our pre-programmed fast ROMs can speed your system execution by eliminating wait states. With much faster turnaround, too. And, at a cost more than 25% below EPROMs.



Quick specs on the 23C128

3 Speeds: 150, 120 and 100 ns max. **Standby Current:** 50 microamps max. **Operating Current:** 10 milliamps max. LSTTL-compatible inputs and outputs. 28-pin JEDEC standard. Military versions, too.

Much more CMOS memory coming from SSS

In case you didn't know it, SSS delivered more 32K and 64K CMOS ROMs than any domestic supplier last year. And we're out to do the same with our new 128K CMOS ROM. Other new CMOS memory devices, including a new 256K CMOS ROM, are on the way.

So why wait?

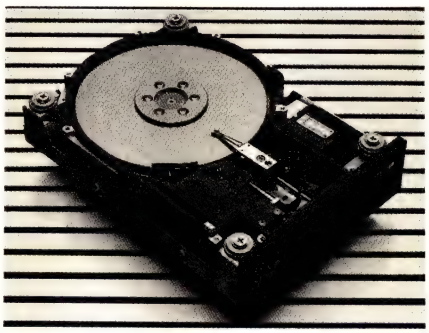
For details on our new 23C128 CMOS ROM or any of our other CMOS memories or logic devices, just call or write. And find out why CMOS *is* a Solid State of mind. Solid State Scientific, 3900 Welsh Rd., Willow Grove, PA 19090. (215) 657-8400.

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CMOS ResponsAbility™

CIRCLE NO 57

Rugged Winchester drive runs portable μCs

A plated medium, a balanced linear actuator and a thermally isolated stepper motor all promise high reliability for the HH-725 disk drive, according to its manufacturer. Intended for the harsh environments of transportable computers, which are larger than battery-powered briefcase computers but still portable, the drive stores 25.5M bytes of data unformatted and 20M bytes formatted.



Designed for ruggedness and equipped with diagnostics *that ensure it stays reliable, Model HH-725 packs 20M bytes in a half-height package.*

A closed-loop servo-positioning system with an embedded servo keeps the heads centered on the track to ensure the reliability of read/write operations, regardless of thermal deformation of the disk or hysteresis of the stepper motor. Thermal isolation of the stepper motor keeps it from transferring heat to the hard-disk assembly. A buffered seek operation allows average-access times of 80 msec; track-to-track access time is 3 msec.

Processor monitors performance

An internal processor takes care of maintaining the quality of data stored on the drive. During power-up, for example, the processor performs a self test, and during normal operation it continues to monitor quality by executing a set of diagnostics. A green LED on the front panel indicates the exact error by flashing a 4-bit code. The in-drive processor also controls the servo's position and monitors the drive's interface status.

All of the drive's electronics come on a single pc board, which saves space inside the half-height drive package and eliminates interconnections that can affect system reliability. Using LSI on the pc board reduces the amount of heat generated.

A new brushless-dc spindle motor helps to keep noise levels down and drive vibration low. But the drive handles vibration whether impressed internally or externally. The firm claims vibration tests on the drive indicate it withstands 5- to 30-Hz 0.4-in. p-p vibrations without damage and shock waves of 40g (20 msec).

The media's the thing

The manufacturer uses a plated medium in the drives to ensure reliability. If the drive is bounced around, the surface of the disk won't flake away, taking your data with it. As a bonus, the plated medium provides higher resolution than conventional media and allows the drive to store 648 tpi and 9680 bpi.

You can mount the drive in almost any orientation to suit your package. The 4-lb drive consumes 18W to allow it to operate on the power supply available in most μCs. The HH-725 costs $999 (1000).—***Ed Teja***

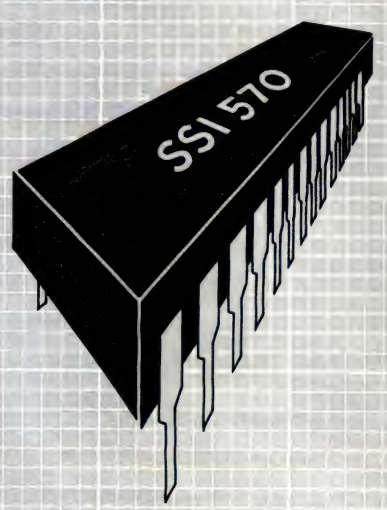
Microscience International Corp, 575 E Middlefield Rd, Mt View, CA 94043. Phone (415) 961-2212.

Circle No 744

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NEW HI-PERFORMANCE FLOPPY DISK CIRCUIT



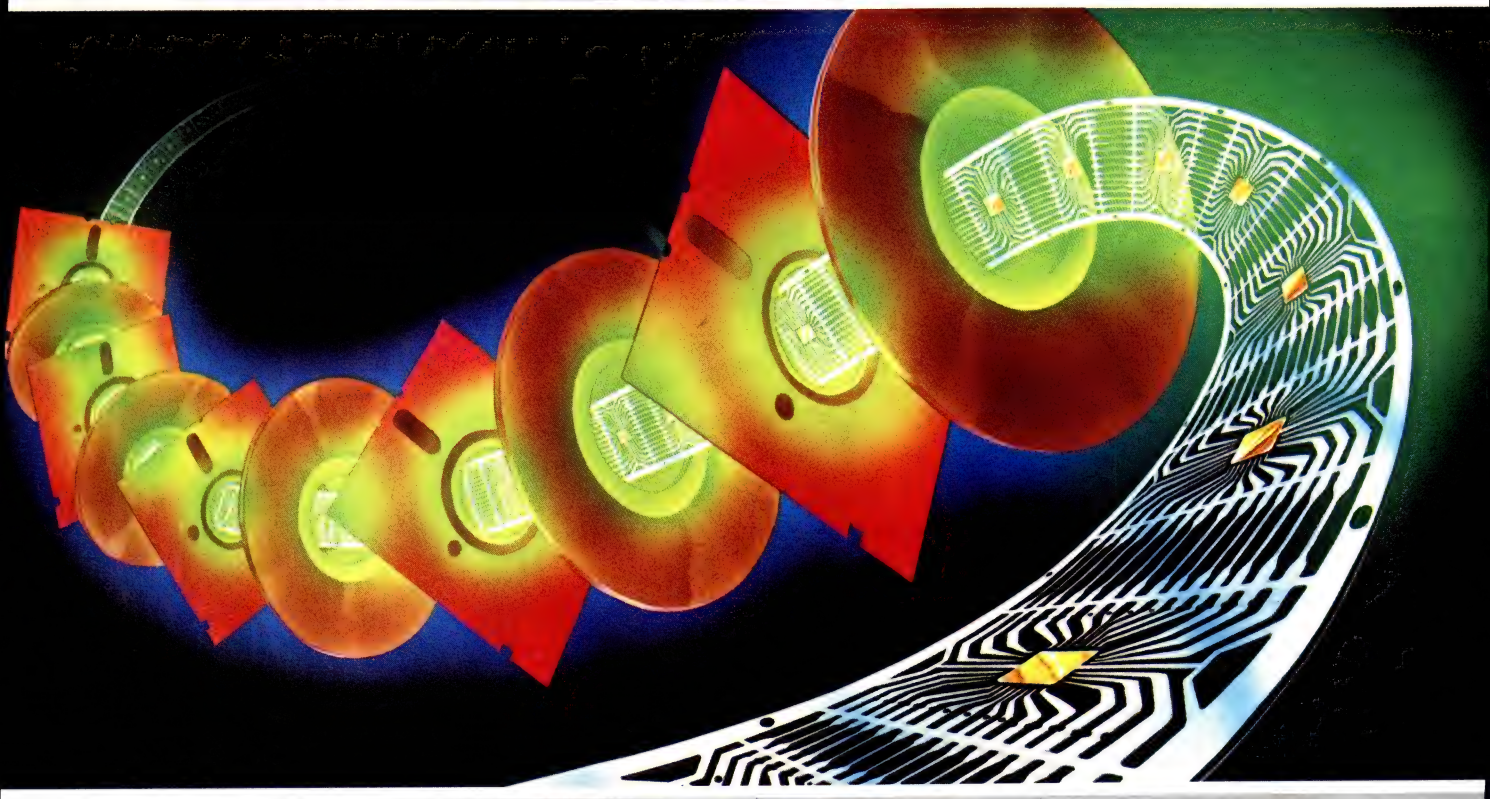
Silicon Systems' latest innovation in disk drive integration is the SSI 570. This creative design by Silicon Systems engineers integrates both the read and write data processing functions on one, 2-channel, monolithic IC. The circuit is designed for use with 8", 5-1/4", and 3-1/4" double-sided floppy disk drives.

The write data circuitry includes the erase head drive with programmable delay and hold times, and the read data circuitry includes low noise amplifiers for each channel. This TTL compatible circuit operates on +5 and +12 volts and is provided in a 28-pin plastic DIP package.

For more information on this new advanced product from the leader in disk drive integration, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680, **(714) 731-7110** Ext. 575.

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For more information on our standard products and custom capabilities, send for our "Rotating Memory Integrated Circuits" brochure.



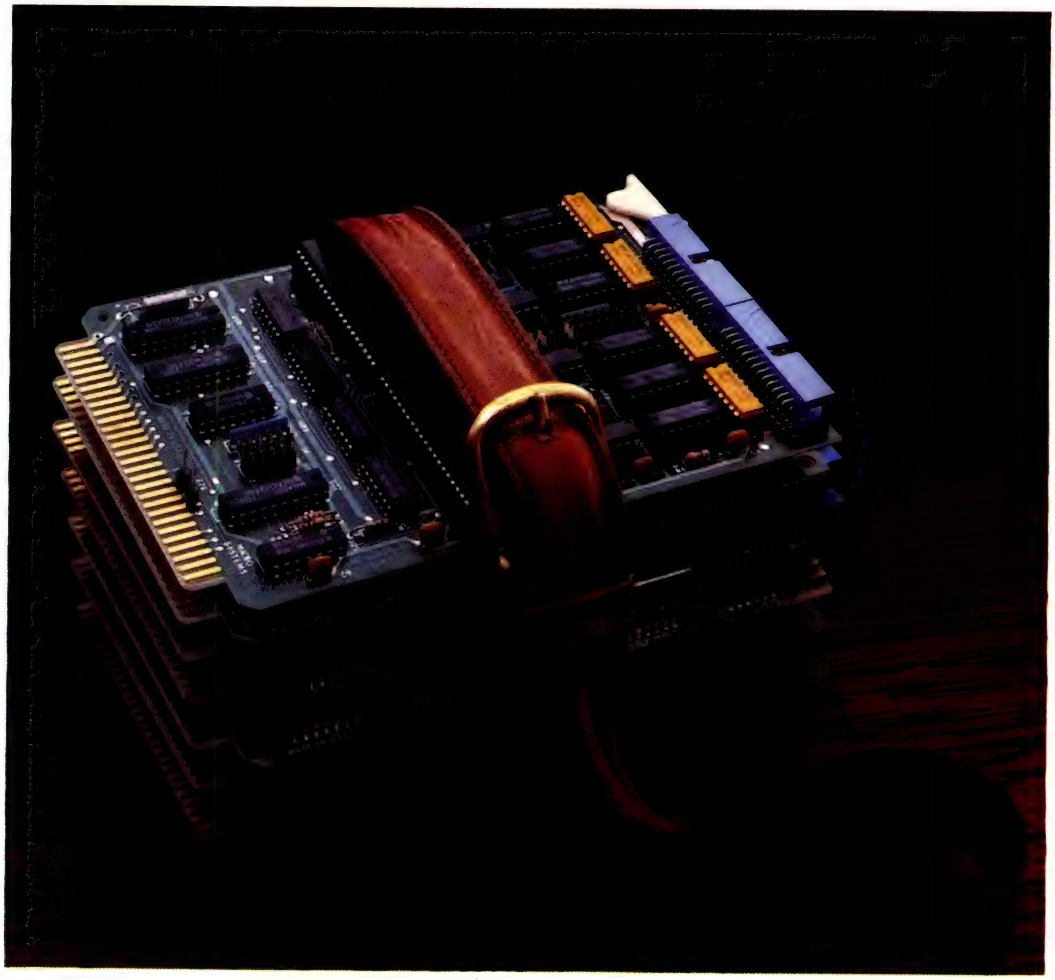
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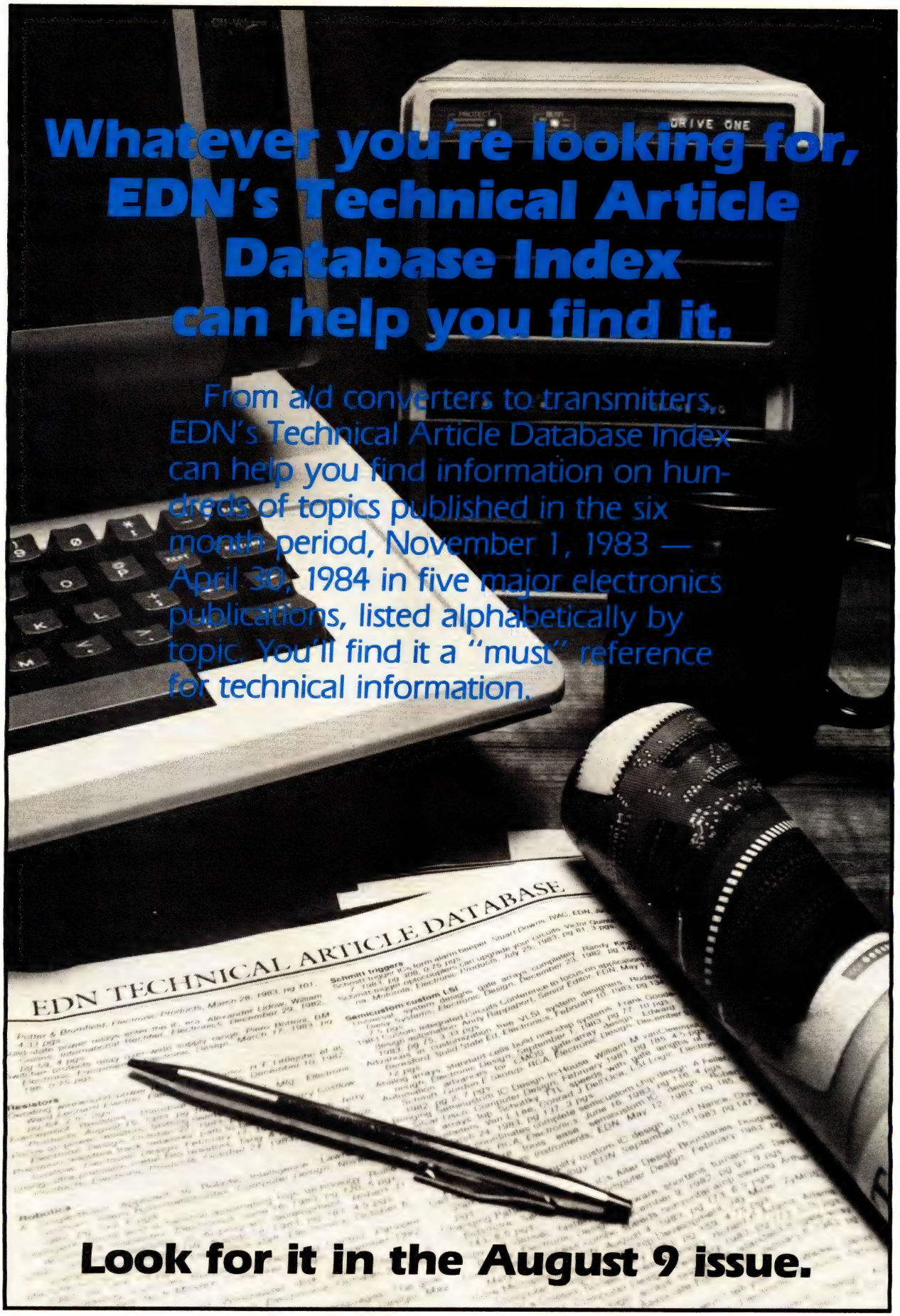
What's more, the STD-BUS is fully expandable. Which makes it simple and economical to add, delete, or interchange boards when you want to redesign or upgrade.

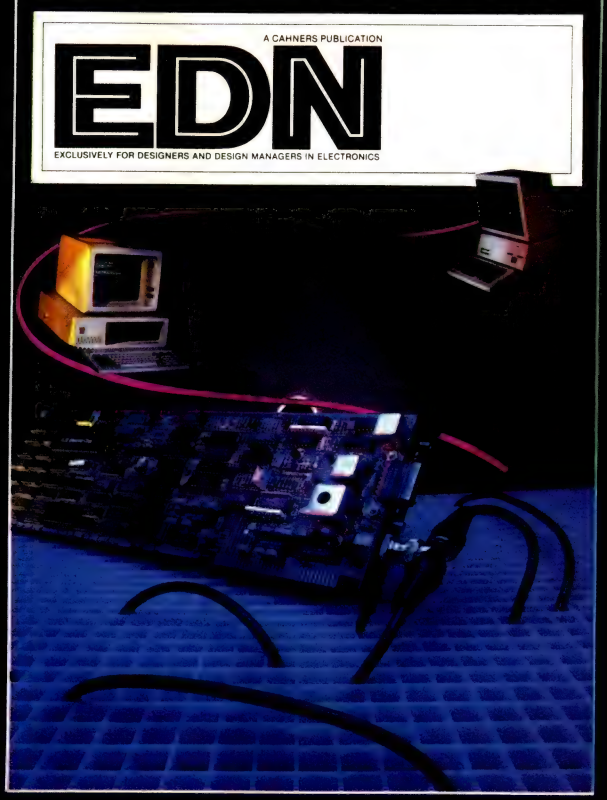
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And our new SDL connector is as hard-working as it is good-looking. Selective gold plating gives it a high cycle life, with easy insertion, secure retention, simple release.

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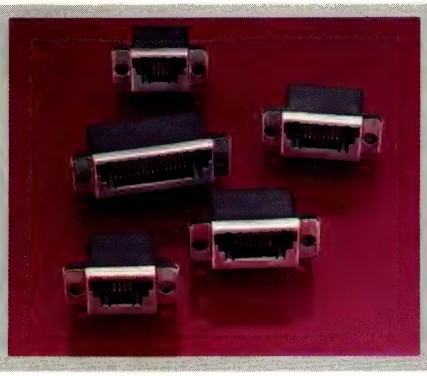
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Top or side entry pcb receptacles, for complete design flexibility.



Round shielded cable terminates in just two steps– one for the conductors, one for the shield.

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LEADTIME INDEX

Percent of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last months average (weeks) Average (weeks)	
TRANSFORMERS								
Toroidal	9	9	27	46	9	—	12.0	9.8
Pot-core	—	30	20	40	—	10	11.7	11.9
Laminate (power)	—	23	29	23	15	—	10.4	9.9
CONNECTORS								
Military panel	—	—	66	17	17	—	12.4	14.8
Flat cable	—	25	50	25	—	—	8.5	5.4
Multi-pin circular	—	42	33	25	—	—	7.5	11.8
PC	15	23	47	15	—	—	6.6	6.5
RF Coaxial	14	57	—	29	—	—	5.8	4.3
Socket	13	20	47	20	—	—	7.4	6.0
Terminal blocks	27	7	46	7	13	—	8.3	5.9
Edge card	6	13	43	38	—	—	9.8	7.6
Subminiature	—	42	29	29	—	—	7.8	12.3
Rack & panel	—	40	40	20	—	—	7.2	7.4
Power	—	33	67	—	—	—	6.0	10.4
PRINTED CIRCUIT BOARDS								
Single-sided	5	29	33	33	—	—	8.5	5.1
Double-sided	—	9	59	32	—	—	10.0	8.4
Multilayer	—	—	25	75	—	—	14.0	11.4
Prototype	8	76	8	—	8	—	4.2	5.2
RESISTORS								
Carbon film	22	41	26	11	—	—	4.7	5.0
Carbon composition	6	44	39	11	—	—	5.8	4.4
Metal film	20	33	33	14	—	—	5.5	5.0
Metal oxide	10	40	30	20	—	—	6.4	5.2
Wirewound	—	27	40	33	—	—	9.0	7.6
Potentiometers	—	27	23	45	—	5	11.1	7.6
Networks	—	33	13	54	—	—	10.3	8.5
FUSES	38	37	25	—	—	—	2.7	2.7
SWITCHES								
Pushbutton	17	44	28	11	—	—	4.9	6.4
Rotary	7	21	51	21	—	—	7.9	6.9
Rocker	11	33	45	11	—	—	6.0	8.2
Thumbwheel	—	45	44	11	—	—	6.2	7.3
Snap action	11	22	67	—	—	—	5.8	6.5
Momentary	11	44	45	—	—	—	4.5	7.1
Dual-in-line	—	25	50	25	—	—	8.5	6.7
WIRE AND CABLE								
Coaxial	—	73	27	—	—	—	3.6	4.0
Flat ribbon	17	44	33	6	—	—	4.5	4.1
Multiconductor	15	46	31	8	—	—	4.7	5.4
Hookup	47	37	16	—	—	—	2.0	2.5
Wire wrap	30	60	10	—	—	—	2.0	2.9
Power cords	29	42	29	—	—	—	3.2	4.3
Other	—	—	34	33	33	—	16.6	4.0
POWER SUPPLIES	8	8	53	31	—	—	9.4	8.2
CIRCUIT BREAKERS	—	30	30	30	10	—	10.4	8.4
HEAT SINKS	12	29	53	6	—	—	5.8	7.2

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last months average (weeks) Average (weeks)	
RELAYS								
General purpose	—	28	36	36	—	—	9.2	5.5
PC board	—	16	38	38	8	—	11.5	7.9
Dry reed	—	—	57	43	—	—	11.4	10.7
Mercury	—	14	57	29	—	—	9.5	7.0
Solid state	—	8	46	46	—	—	11.2	6.9
DISCRETE SEMICONDUCTORS								
Diode	8	16	40	20	12	4	11.1	9.7
Rectifier	6	28	28	38	—	—	8.9	8.8
Thyristor	—	23	23	46	8	—	11.7	11.9
FET	—	25	25	42	8	—	11.3	13.2
Zeners	4	26	26	18	26	—	12.2	10.9
INTEGRATED CIRCUITS, DIGITAL								
CMOS	—	—	24	24	28	24	20.5	17.4
TTL	—	—	13	26	26	35	22.8	18.1
LS	—	4	4	25	38	29	23.3	22.6
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	—	—	11	45	33	11	20.1	14.5
OP amplifier	—	10	30	35	15	10	12.1	13.7
Voltage regulator	—	—	60	20	15	5	13.5	12.7
MEMORY CIRCUITS								
RAM 4K	—	—	18	18	55	9	21.4	19.3
RAM 16K	—	9	18	27	37	9	18.4	18.6
RAM 32K	—	—	—	25	62	13	24.2	19.6
RAM 64K	—	—	18	9	55	18	22.8	21.1
ROM/PROM	—	—	17	42	33	8	19.1	18.6
EPROM	—	7	7	27	52	7	20.7	17.2
EEPROM	—	—	17	17	66	—	21.2	19.2
DISPLAYS								
Panel meters	11	11	33	45	—	—	10.1	6.2
Flourescent	14	14	43	29	—	—	8.4	6.4
Incandescent	14	29	43	14	—	—	6.3	7.4
LED	9	26	39	22	4	—	8.2	5.5
Liquid crystal	—	15	31	31	23	—	13.7	9.0
MICROPROCESSOR ICs	—	—	6	24	29	41	24.6	21.7
FUNCTION PACKAGES								
Amplifier	—	—	40	60	—	—	12.8	10.3
Converter, analog to digital	—	—	33	45	22	—	15.6	11.0
Converter, digital to analog	—	—	37	50	13	—	14.3	11.4
LINE FILTERS	—	50	17	—	17	16	11.7	8.4
CAPACITORS								
Ceramic	21	18	25	36	—	—	8.1	6.9
Ceramic, monlolythic	5	32	27	36	—	—	8.6	7.5
Ceramic, disc	10	30	30	30	—	—	7.8	6.3
Film	12	24	46	18	—	—	7.1	7.0
Electrolytic	13	13	39	26	9	—	9.9	8.8
Tantalum	13	22	17	44	4	—	9.9	8.9
INDUCTORS	—	14	43	43	—	—	10.6	6.4

Source: *Purchasing* magazine's electronic business survey

When reliability is imperative.



Photo courtesy of Lockheed California Company

NEW! 3-phase, 400 Hz, Mil-Spec Linear Power Supply

For demanding airborne applications, such as acoustic data processing, electronic surveillance and countermeasures equipment, Abbott's new WL Series of compact power supplies deliver:

MORE POWER IN LESS SPACE. WL Models provide power densities of up to 3.67 watts per cubic inch, with a maximum case height of just 2.5 or 2.75 inches, depending on output power. This permits a space savings of up to 60%, since a balanced ac power distribution system can now be maintained without resorting to three single-phase supplies or costly custom designs.

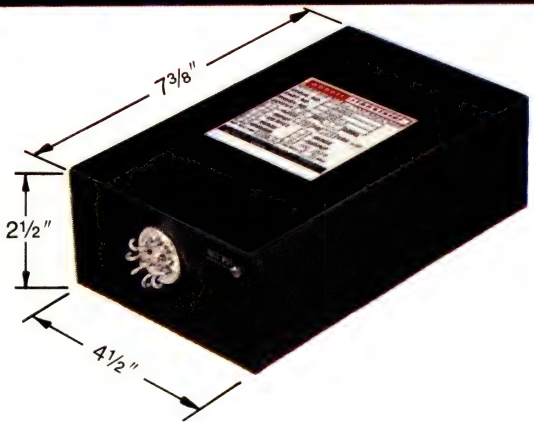
ENVIRONMENTAL PERFORMANCE. Ruggedly built WL Models are fully encapsulated and hermetically sealed to protect against salt spray, high humidity, shock, vibration and other applicable environmental conditions defined in MIL-STD-810C.

ELECTRICAL PERFORMANCE. The low EMI of these power supplies ensures compatibility with sophisticated electronics. All units meet applicable requirements of MIL-STD-461B for emissions and susceptibility. They are also protected against input transients of up to 180 Vrms for 100 ms, in accordance with MIL-STD-704.

ABBOTT RELIABILITY. Design engineers have been specifying Abbott power supplies for 23 years...whenever reliability is imperative. The consistent performance that has made the Abbott single-phase Model W the most popular 400 Hz power supply in airborne applications is now available in our new 3-phase WL and WWL Series. Please contact Abbott Transistor Laboratories, Inc., Power Supply Division.

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- Input: 105-125 Vrms, 380-420 Hz, 3-phase "delta" std. 3-phase "Wye" input optional
- Single and dual outputs, 5-28 Vdc
- Output power 48 to 420 Watts
- Low ripple of 5 mVrms, peak-to-peak 25 mV
- High 55% efficiency
- Load regulation: 0.1% from no-load to full-load
- Operating temperature range −55°C to +100°C

HIGH RELIABILITY:
MTBF CALCULATED PER MIL-HDBK-217D

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Ground benign	164,406 hours	883,580 hours
Air-inhabited	25,633 hours	94,956 hours

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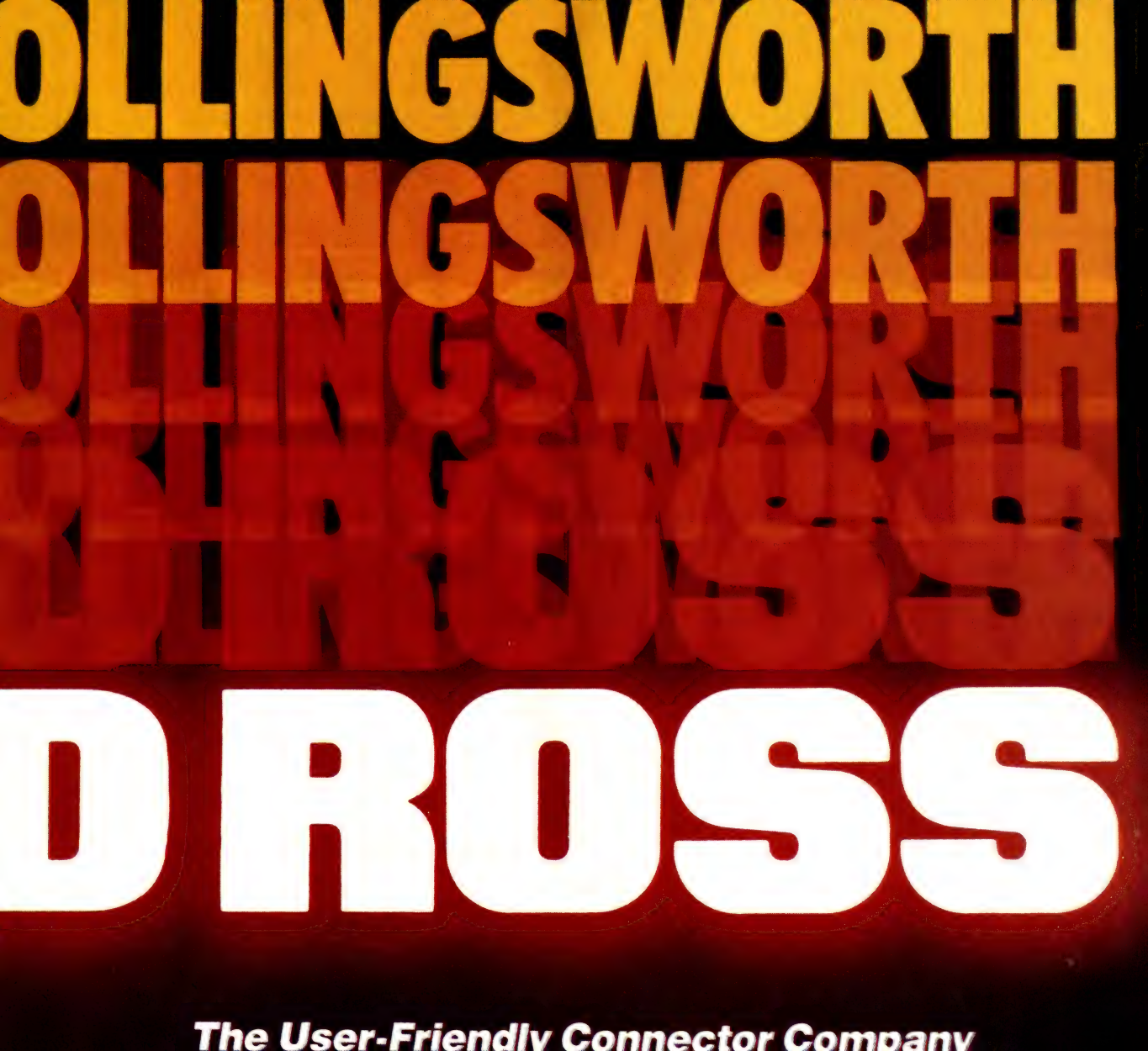
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FCC Class B EMI filtering • From $49



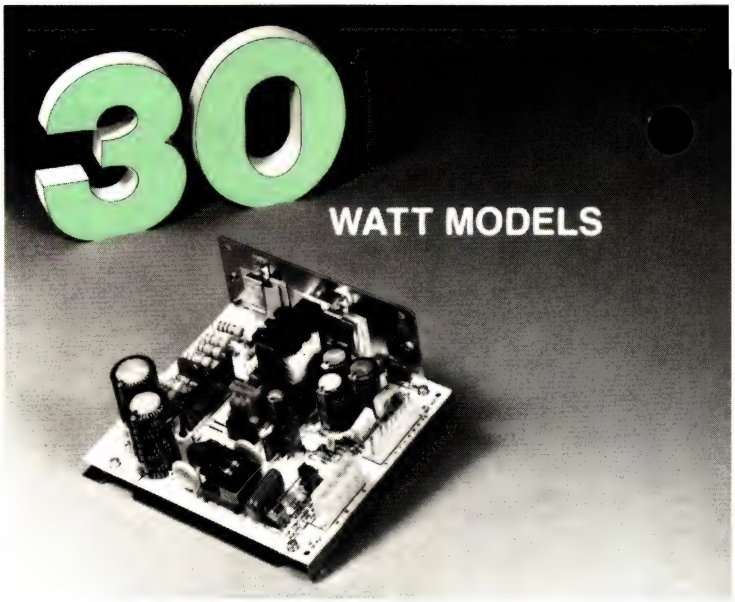
Two proprietary hybrid microcircuits provide control and current limit functions. These reduce parts population, increasing MTBF and lowering cost.

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Optional steel enclosures

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KEPCO/TDK SERIES ERX™



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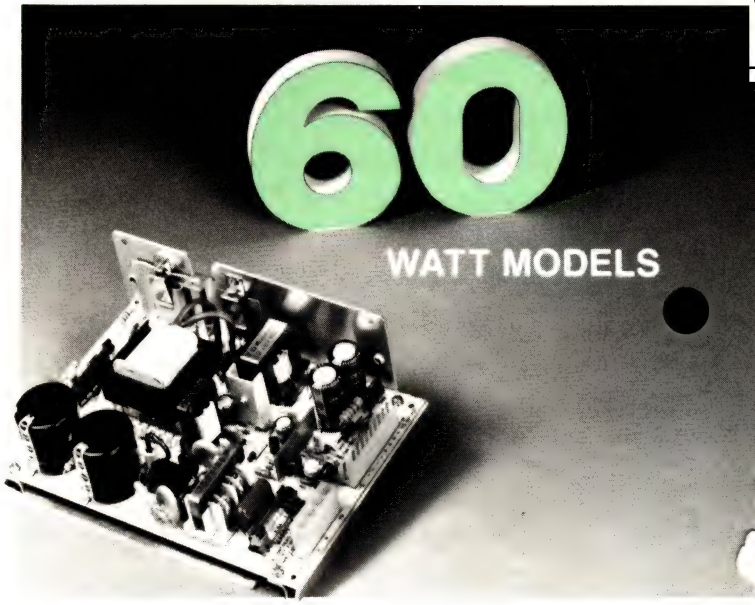
We call them ERX. You'll call them the answer to the problem of finding cost-effective power supplies that meet international safety and EMI standards.

Our series ERX consists of 12 models...from 5V to 24V in three sizes; 30 Watts, 60 Watts and 120 Watts. They provide well-stabilized adjustable d-c outputs, protected by a current limiter and over voltage protector, with remote error sensing available to compensate for the connecting wire's voltage loss. A flying lead allows you to select either 115V a-c or 230V a-c operation.

The built-in EMI filter attenuates conducted noise below the limits of FCC 20780 for Class B computing devices and meets VDE 0871 as well. An optional enclosure reduces radiated noise below VDE 0875/7.71 (level N) — a useful option if you will use the power supply in a non-metallic enclosure.

The series ERX has the clearance/creepage spacings and meets the hi-pot ratings of IEC 380 and VDE 0806. And, of course, meets both UL478 and CSA C22.2-154. It is truly an international design.

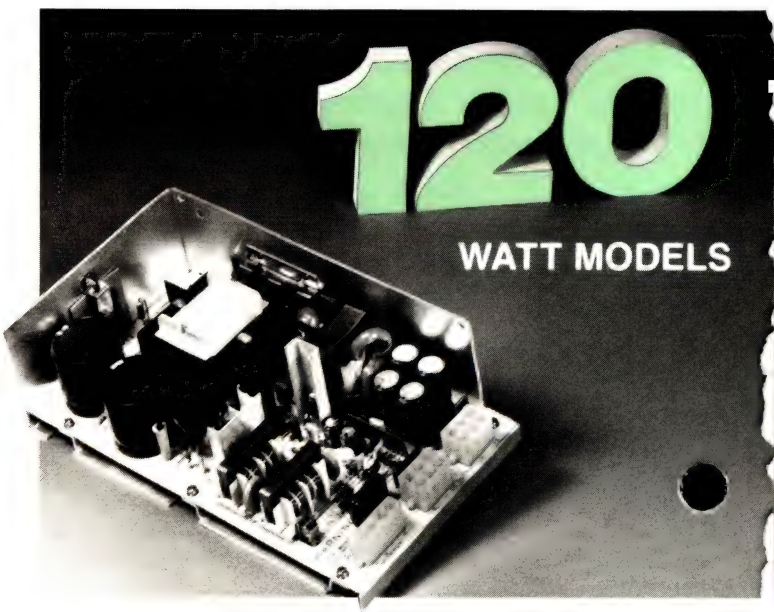
To make room for the greater spacings and larger transformer needed to meet VDE/IEC requirements, we designed two custom hybrid microcircuits, chip components bonded to a ceramic substrate. As the close-up photography reveals, these hybrid microcircuits contribute to a clean, un-cluttered layout.



Best of all is the price:

Single unit price	Optional enclosure
$ 49.00 . . . 30W	CA-15 . . .$9.00
$ 75.00 . . . 60W	CA-16 . . .$9.00
$129.00 . . .120W	CA-17 . . .$9.00

Quantity discounts are available to OEM buyers.



This KEPCO product is backed by a firm **1-YEAR WARRANTY**

Data subject to change without notice

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Model Number	ERX 5-6	ERX 12-2.5	ERX 15-2	ERX 24-1.3
Output Volts	5V	12V	15V	24V
Adjustment Range	4.5-5.5	10.8-13.2	13.5-16.5	21.6-26.4
Output Current, Amperes 40°C	6	2.5	2.0	1.3
Output Current, Amperes 50°C	4.8	2.0	1.6	1.0
Output Current, Amperes 60°C	3.6	1.5	1.2	0.8
Output Current, Amperes 70°C	2.4	1.0	0.8	0.5
Current Limit (Amps)	6.3~7.8	2.6~3.3	2.1~2.6	1.4~1.7
OVP Setting (Volts)	5.8~6.9	13.7~15.7	17.0~19.0	27.0~30.5
Ripple & Noise (1) (mV, p-p)				
source (typ)	5	20	20	30
source (max)	10	40	40	50
switching (typ)	40	40	40	40
switching (max)	70	80	80	100
spike noise (2)	150	300	300	400

Input Current (at 40°C, nominal input voltage):
- typical — 0.6/0.3A
- maximum — 0.8/0.4A
- input fuse value — 2.5A
- surge current (thermistor limiter) — 41/82A
- efficiency (typ) — 68%

(1) Source component 2x source frequency, and switching component approximately 30-100 KHz.
(2) Measured with a 50 MHz bandwidth, p-p.

Model Number	ERX 5-12	ERX 12-5	ERX 15-4	ERX 24-2.5
Output Volts	5V	12V	15V	24V
Adjustment Range	4.5-5.5	8.4-13.2	10.5-16.5	16.8-26.4
Output Current, Amperes 40°C	12	5	4	2.5
Output Current, Amperes 50°C	9.6	4.0	3.2	2.0
Output Current, Amperes 60°C	7.2	3.0	2.4	1.5
Output Current, Amperes 70°C	4.8	2.0	1.6	1.0
Current Limit (Amps)	12.6~15.6	5.2~6.5	4.2~5.2	2.6~3.3
OVP Setting (Volts)	5.8~6.9	13.7~15.7	17.0~19.0	27.0~30.5
Ripple & Noise (1) (mV, p-p)				
source (typ)	5	20	20	30
source (max)	10	40	40	50
switching (typ)	30	40	40	40
switching (max)	50	80	80	100
spike noise (2)	150	300	300	400

Input Current (at 40°C, nominal input voltage):
- typical — 1.4/0.7A
- maximum — 1.6/0.8A
- input fuse value — 3.15A
- surge current (thermistor limiter) — 41/82A
- efficiency (typ) — 72%

(1) Source component 2x source frequency, and switching component approximately 50 KHz.
(2) Measured with a 50 MHz bandwidth, p-p.

Model Number	ERX 5-24	ERX 12-10	ERX 15-8	ERX 24-5
Output Volts	5V	12V	15V	24V
Adjustment Range	4.5-5.5	8.4-13.2	10.5-16.5	16.8-26.4
Output Current, Amperes 40°C	24	10	8	5
Output Current, Amperes 50°C	19.2	8	6.4	4
Output Current, Amperes 60°C	14.4	6	4.8	3
Output Current, Amperes 70°C	9.6	4	3.2	2
Current Limit (Amps)	25.2~31.2	10.5~13.0	8.4~10.4	5.2~6.5
OVP Setting (Volts)	5.8~6.9	13.7~15.7	17.0~19.0	27.0~30.5
Ripple & Noise (1) (mV, p-p)				
source (typ)	5	20	20	30
source (max)	10	40	40	50
switching (typ)	40	40	40	40
switching (max)	70	80	80	100
spike noise (2)	150	300	300	400

Input Current (at 40°C, nominal input voltage):
- typical — 2.3/1.2A
- maximum — 2.8/1.4A
- input fuse value — 5A
- surge current (softstart limiter) — 17/34A
- efficiency (typ) — 74%

(1) Source component 2x source frequency, and switching component approximately 50 KHz.
(2) Measured with a 50 MHz bandwidth, p-p.

SPECIFICATIONS

INPUT CHARACTERISTICS

Source voltage: 85-132V a-c or 170-264 V a-c. jumper selectable.
Source frequency: 47-66 Hz, single phase.
Brownout voltage: 80/160V a-c.
Typical efficiency vs loading: (see Fig. 1)
Holding time: for the nominal input voltage and 40°C loading current — 30 msec typical, 20 msec minimum.
Conducted noise: built-in input filter attenuates the conducted noise below the limit of FCC Part 15 Class B.
Radiated noise: an optional shielded metal enclosure is available. With this cover, the radiated noise is below VDE 0875/7.71 (level N)

OUTPUT CHARACTERISTICS

Voltage adjustment range: See tabulated adjustment range.
Current limit: the current limit setting is tabulated for each model. It is fixed by an internal resistor with the threshold of the current limit within the tabulated limits. Shape approximately rectangular (not foldback type), so there is no difficulty driving non-linear loads or using multiple power supplies in series. Recovery is automatic. The change in the current limit threshold for temperature and source input is ±10%.
Recovery Characteristics: a step load change from 50% to 100% produces less than 4% output excursion; recovery occurs to within 1% of the original setting within 1 millisecond (for a step load rise time >50μsec).
Overvoltage Protection: an overvoltage sensor shuts down the switching oscillator drive and reduces the output. It is reset by turning the source power off for approximately 60 seconds. The OVP threshold is tabulated for each model.
Remote Error Sensing: jumper wires are provided between the output and terminals marked ±S. If these jumpers are cut, and separate wires are run to the load, the ERX power supply can compensate for voltage drops in the load wires up to 0.35V per wire.

STABILIZATION

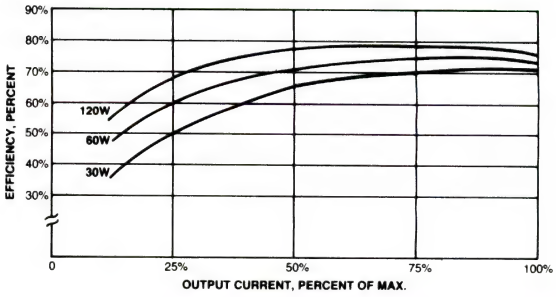
Specification	Condition	Typical	Maximum
Source effect	min-max	0.6%	1.0%
Load effect*	10-100%	0.6%	1.0%
Temperature effect	0-70°C	1.0%	2.0%
Combined effect	envelope	2.2%	4.0%
Time effect	8-hr drift @ 25°C	0.1%	0.5%

*load effect is measured between +S and −S terminal

GENERAL

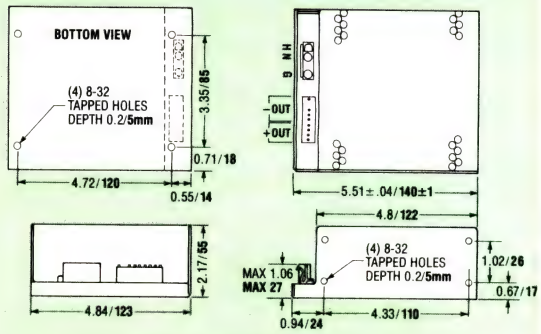
Ambient operating temperature range: 0-70°C.
Storage temperature range: −20 to +75°C.
Humidity: 85%RH, noncondensing.
Isolation: (at 25°C, 65% relative humidity):
between input and output terminals:
3750V a-c, 1 minute
between input and chassis:
1250V a-c, 1 minute
between output terminals and chassis:
500V d-c, 100 megohms
Vibration:
5-10 Hz: 10mm, 3 axes. 10-55 Hz: 2g, 3 axes.
Shock: 20g, 3 axes (11 ±5 ms pulse duration)
Safety: All models are designed to meet UL 478 • CSA 22.2-154 • VDE 0806 • IEC 380
Dimensions: See outline drawings.

Fig. 1 — TYPICAL EFFICIENCY VS. LOADING



Decimal dimensions in light face type are in inches, **dimensions in bold face type are in millimeters.**

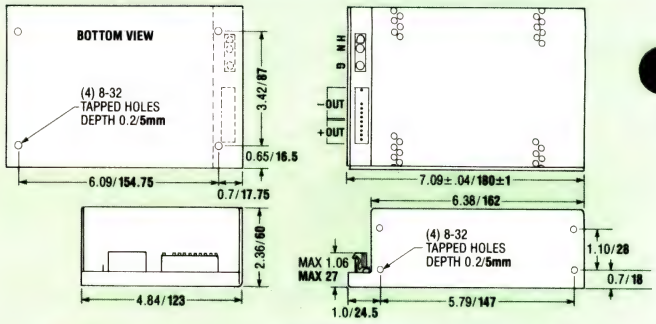
Tolerances 0.03 inches/ **0.7 millimeters.**



30 WATT MODELS

WEIGHT: English 1.5 lbs. / Metric 0.7 Kg

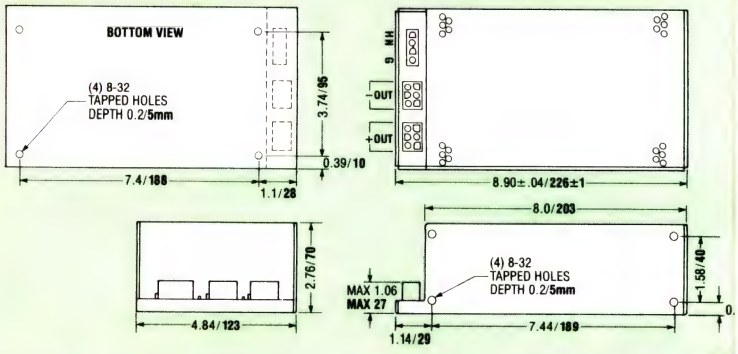
	Wafer	Housing	Terminal	Maker
INPUT	5219-04A	3191-04R1	1381 ATL	Molex
OUTPUT	5277-8A	5196 Series	5194 Series	Molex



60 WATT MODELS

WEIGHT: English 1.5 lbs. / Metric 0.7 Kg

	Wafer	Housing	Terminal	Maker
INPUT	5219-04A	3191-04R1	1381 ATL	Molex
OUTPUT	5277-10A	5196 Series	5194 Series	Molex



120 WATT MODELS

WEIGHT: English 3 lbs. / Metric 1.4 Kg

	Wafer	Housing	Terminal	Maker
INPUT	5219-04A	3191-04R1	1381 ATL	Molex
OUTPUT	5219-06A	3191-06R1	1381 ATL	Molex

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For microcomputers, minis and mainframes, Airpax magnetic circuit breakers assure positive protection. They're unaffected by ambient temperature, and serve the dual function of power switch and overload protection.

And Airpax thermostats monitor cabinet temperatures, and shut down systems instantly when overheat threatens sensitive circuits.

You can select from our thousands of standard models. Or we'll create a custom model for you, and produce a few dozen for prototypes, or millions for a production run.

Ask us for engineering data. Airpax Corporation, a North American Philips Company, W. Johnson Ave., Box A, Cheshire, CT 06410. (203) 272-0301.

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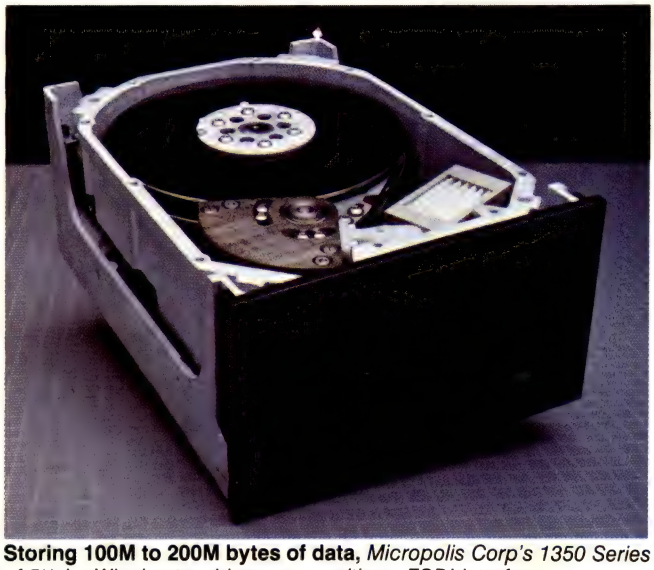
CIRCLE NO 63

Winchester



disk drives

Winchester-disk-drive manufacturers continue to make technological innovations, pushing capacities, performance and packaging densities to significant new levels.



Storing 100M to 200M bytes of data, *Micropolis Corp's 1350 Series of 5¼-in. Winchester drives come with an ESDI interface.*



Three drive families, *the XT-1000, XT-2000 and EXT-4000, from Maxtor furnish 380M bytes (unformatted) of data storage in a 5¼-in. form factor.*

Manufacturers of 5¼-in. Winchester disk drives *are finally delivering what they promised—high-capacity units in production volumes. (Photo courtesy Vertex Peripheral Corp)*

Edward R Teja, *Western Editor*

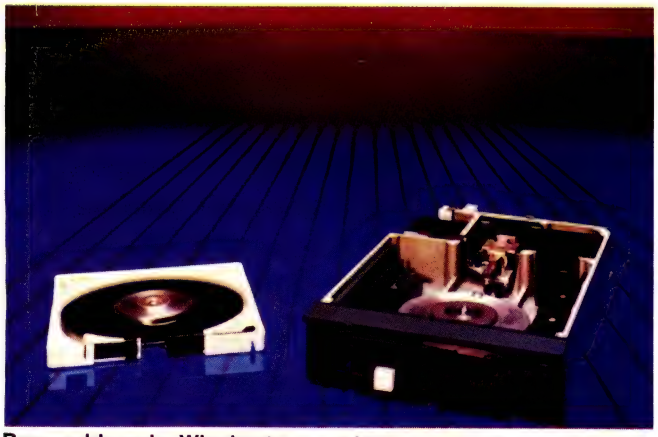
Despite some technological false starts and credibility gaps that premature product announcements create, Winchester-disk-drive manufacturers have reached the critical and requisite step toward device stability—volume production. Today most of the high capacities touted for 5¼-in. drives are available. Indeed, you can buy 5¼-in. Winchesters that store from 5M to 320M bytes of formatted data.

Along with storage-capacity improvements comes the equally impressive progress that manufacturers are making in lowering prices. Pricing depends to a large extent on drive capacity. A half-height 10M-byte drive, for example, typically costs around $500, and a 320M-byte drive sells for about $4250. The larger drive, while costing much more, can actually prove more economical in terms of price/megabyte—$13.28/megabyte compared with $50/megabyte on the smaller-capacity drive. Knowing your system's requirements is imperative if you're going to choose the most cost-effective drive. (**Fig 1** shows the price/megabyte curve for the high-capacity 5¼-in. drives covered in this article.)

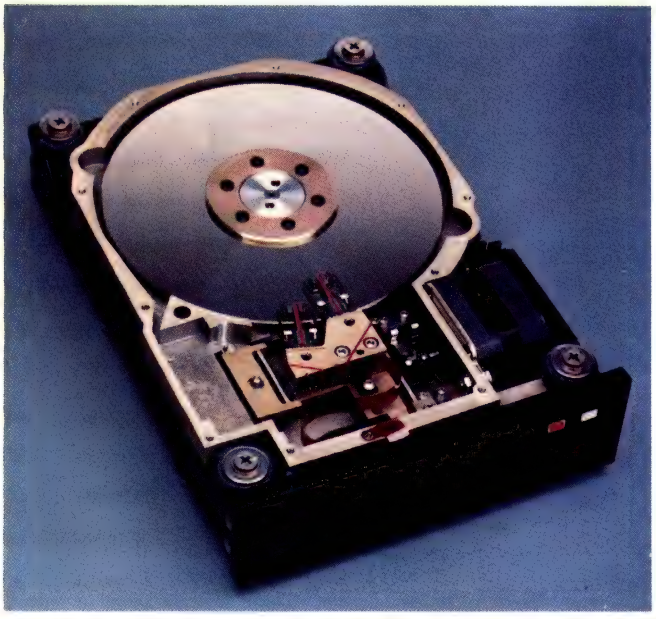
Beyond system requirements, you'll also have to understand the changing terminology manufacturers use to classify their drives. Nowadays, low-capacity 5¼-in. drives are those that offer less than 40M bytes storage. Similarly, manufacturers refer to drives with an average access time in excess of 35 msec (some vendors use 40 msec) as being low performance. In general, your final choice of drive will most likely depend on

- disk capacity
- access time
- cost effectiveness
- future needs (eg, expansion for additional users).

Disk drives have become complex system components



Removable-only Winchester cartridges *using 100-mm-diameter media let Syquest Technology's SQ306RD store 5M bytes in a small package space.*



Promising high performance in a half-height 10M-byte drive, *Microscience International Corp's HH-612 ($999) uses two head assemblies to achieve 55-msec average access times.*

What all this means is that you can't talk about drives by themselves any more. They aren't simple components to be specified in bulk with no thought to future use. The division of drives into low- and high-performance categories, for example, only exists in terms of their applications. Otherwise, such divisions make no sense. Disk drives are complex components, and each drive's true capabilities become clear only when you take a look at its role in the overall system.

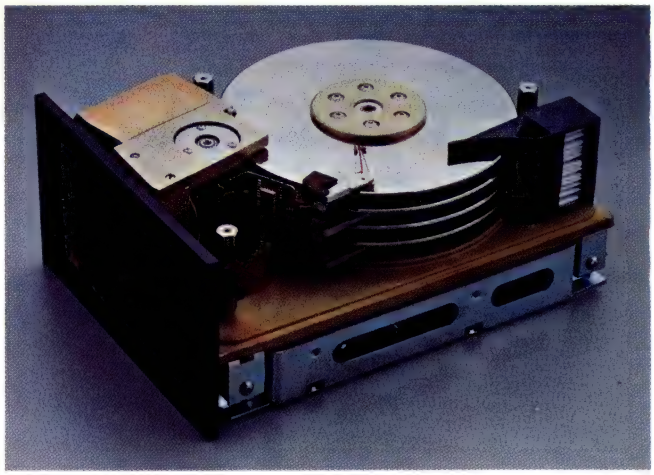
Table 1 puts some of the drive's most important performance characteristics into perspective, listing key specs for some of the high-performance, high-capacity drives currently available. Arranging the specifications of the drives you're considering in this tabular manner quickly discloses whether a candidate meets your basic cost/performance requirements. But remember that most OEM prices are negotiable. Don't let price differences of a few dollars deter you from talking to vendors of higher-priced drives.

But before you begin your selection process, keep in mind that the choice of native interface (the one the disk controller will have access to) can actually dictate some significant drive characteristics, such as storage capacity. Priam's 5¼-in. Winchester, for example, uses one set of electromechanical components to meet several capacity needs. Its Model 504 costs $1850 (OEM) and comes with the ST-506/412 native interface currently used by most drives. Equipped with its ST-506/412 electronics, Model 504 stores 86M bytes of data. The same drive with Priam's own native interface becomes the 111M-byte Model 505 and costs $2300 (OEM). Both models have six platters.

The difference in capacity between the two models results from one of the ST-412 specification's characteristics rather than any technology changes. At any given disk-rotation speed, the interface standard's data-transfer rate of 5M bps limits a drive's linear storage density—the number of bits it can store linearly along each track—to 9212 bpi. On a 5¼-in. disk, this figure works out to 10,416 bytes/track after the disk is formatted. An interface that doesn't restrict the data-transfer rate to such a low level permits higher linear densities. In the case of the Model 505, that higher linear density turns out to be 11,886 bpi or 13,440 bytes/track.

The fine art of specsmanship

The difference in linear densities that accrues from a change in the interface is a good indication of the difficulty inherent in selecting a drive strictly from its data sheet. While not impossible, to compare one drive to another, you must follow a rough and rocky road.



Right on the line between technology and manufacturability, *Vertex's drives use thin-film media and under-the-bubble preamps for maximum performance.*

One of the the most critical and often confused drive specs is average access time. The access time is literally the time it takes to access information on the disk. But this figure represents a *typical* access time, assuming that your data is distributed randomly on the disk surface and you don't know ahead of time how many cylinders the head will have to move. Thus, the average access time proves a critical measurement in determining how well a particular drive meets the needs of multiuser and multitasking systems.

The track-to-track access time is the time it takes a drive to move its heads from one track (or cylinder) to

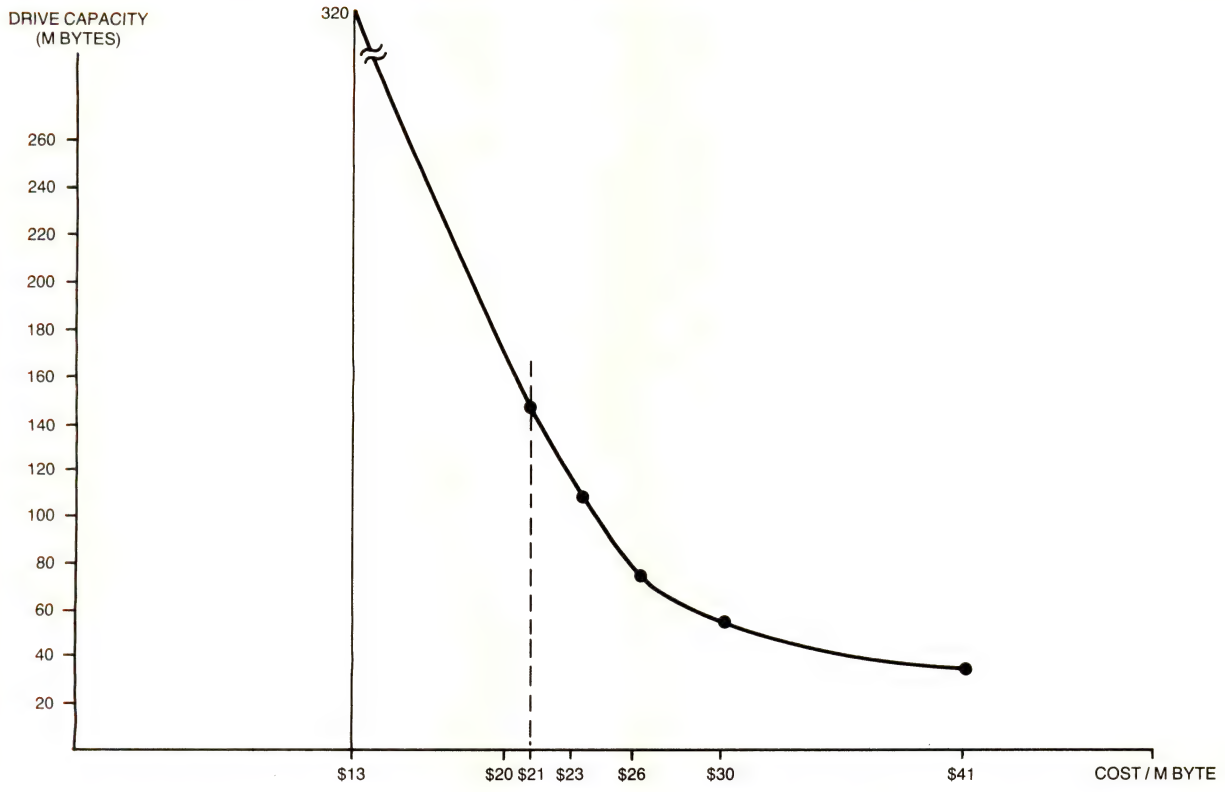
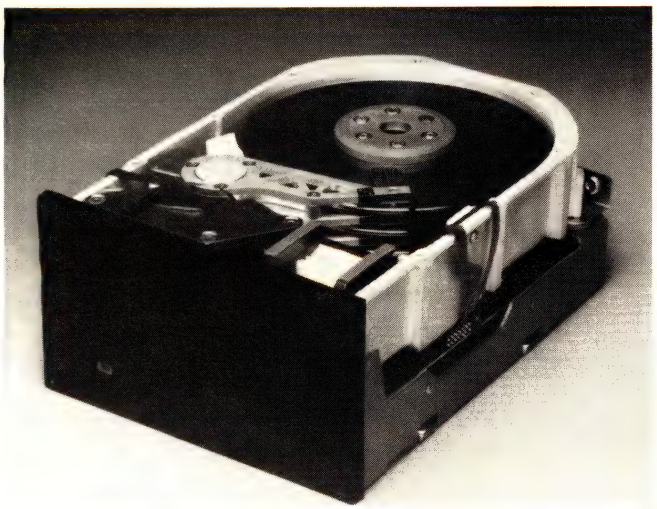
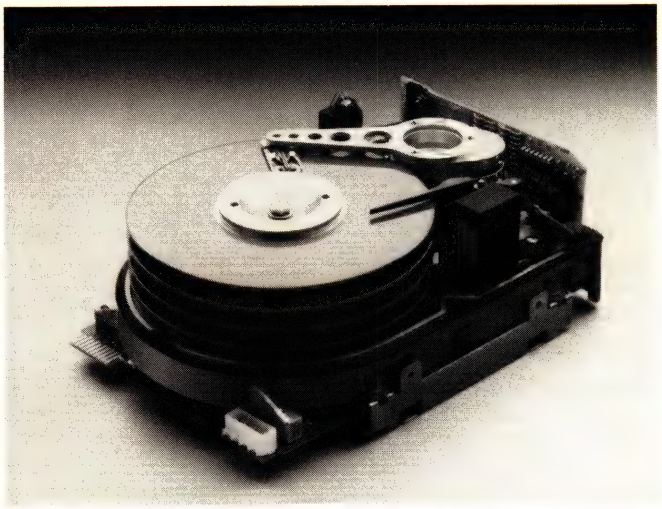


Fig 1—As the storage density increases, *the cost/megabyte falls, making the higher capacity drives cost effective despite their seemingly high price tags.*



Using plated media, *Tandon Corp's Model TM705 stores 50M bytes of data and costs less than $1000 in large OEM quantities.*



You can choose from 20M to 50M bytes of storage *with Quantum Corp's Q500 Series of 5¼-in. drives.*

the next. This time represents the best but unlikely case where the data resides on adjacent tracks. To calculate a more typical time, given that data storage is random, drive vendors assume that the drive will, on the average, have to move ⅓ of the maximum number of tracks in a random seek operation.

In addition to describing the time it takes to move the heads to the desired cylinder, the average access time must include settling time—the time allotted for the heads to settle down to ensure reliable reading and writing. Unfortunately, there is more than one measurement method used to determine the average access (or seek) time. Some methods measure only part of the time that must elapse before the drive can read or write.

Properly defined, the average seek time is the time that the Seek-Complete interface signal on an ST-506 drive remains False. This line goes False when the step pulse is sent to the drive and stays there until the heads are positioned for reading or writing. Thus, measuring average seek time by this standard includes all of the time it takes for the drive to get ready to take care of system business.

For high-performance computer systems, the average access time might be the most important drive specification outside of price. **Fig 2** shows the relationship between a drive's average seek time and the amount of disk activity it will support. A disk drive with a 30-msec average access time will allow slightly more than 90,000 seek operations/hr. But if the access time increases to 40 msec, data-access capability falls to approximately 70,000 seek operations/ hr.

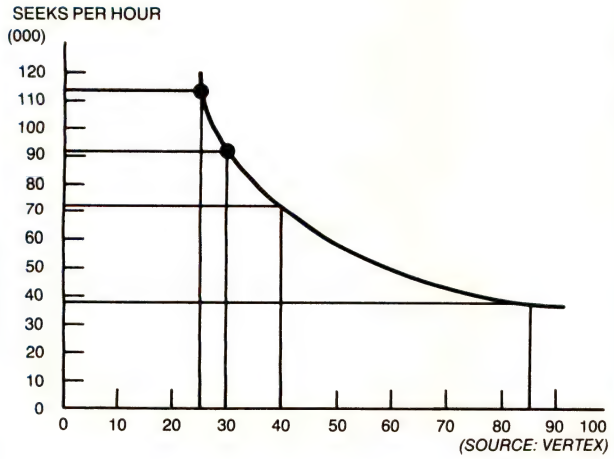


Fig 2—The drive's average access time, *measured in milliseconds, determines the amount of disk activity the system can support, measured in the number of seek operations/hr. (Courtesy Vertex Peripheral Corp)*



Formatted as 306 cylinders *to maintain compatibility with IBM PC/DOS software, Cogito Systems' Model CG912 half-height Winchester uses less than 12W.*

Translating the number of seek operations/hr to a system application with a large number of users gives a clear indication of how this spec limits system operation. For instance, an 8-user system that employs a disk drive with an 85-msec average access time would limit each user to less than 500 seeks/hr—8.3 seek operations/min. In a large 32-user environment, each user could go to the data well only 125 times an hour—two times a minute. This is clearly an unrealistic figure. Any disk-intensive application such as software development or business software using overlays, like spreadsheet and word-processing packages, can place heavier access demands on a system. Micropolis suggests that a 30-msec-access-time drive in a multiuser UNIX system couldn't support more than eight to 10 users. Because of the file structure, it takes seven to 30 seek operations to access a single record under UNIX, and studies indicate that users won't tolerate more than a 2-sec wait for a response. Thus most vendors place the single-user/multiuser demarcation line for drives at 30 or 35 msec.

Three techniques increase capacity

The race by disk-drive manufacturers to increase storage capacity is taking place in three product-development arenas. The brute-force mechanical approach involves adding more disks and heads to existing

TABLE 1—HIGH-PERFORMANCE 5¼-IN. WINCHESTERS

MANUFACTURER	MODEL	CAPACITY[1]	PRICE[2]	COST[3]	HEADS	DISKS	TRACK DENSITY	LINEAR DENSITY	AVG ACCESS TIME	INTERFACE
ATASI	30333	26	$1500	$58	5	3	800	8780	30	ST-506/412
	3046	36.4	$1600	$44	7	4	800	8780	30	ST-506/412
	3065	51.6	$1850	$36	7	4	980	9490	24	ST-506/412
	3075	59.0	$1950	$33	8	5	980	9490	24	ST-506/412
COMPUTER MEMORIES INC	CM-7660	47.22	$1310	$28	6	3	1173	9275	40	
	CM-7880	62.97	$1505	$24	8	4	1173	9275	40	
	CM-6640	31.5	$1045	$33	6	3	720	9275	40	
CONTROL DATA CORP	9415-36	36.29*	$1250	**	5	3	800	9000	45	ST-506/412
	9415-86	8.96*	$1845	**	9	5	960	9540	35	ST-506/412
FUJITSU AMERICA LTD	M2241AS	24.7	$1600 (100)	$65	4	3	760	10,200	30	ST-506/412
	M2242AS	43.2	$1800 (100)	$42	7	4	760	10,200	30	ST-506/412
	M2243AS	67.8	$2000 (100)	$30	11	6	760	10,200	30	ST-506/412
MAXTOR	XT-1065	52.5	$1635 (500)	$31	7	4	980	9875	30	ST-506/412
	XT-1140	112.5	$2915 (500)	$26	15	8	980	9875	30	ST-506/412
	XT-2085	70.2	$1795 (500)	$26	7	4	980	11,155	30	ST-506/412
	XT-2190	150.4	$3205 (500)	$21	15	8	980	11,155	30	ST-506/412
	EXT-4075	70	$1490 (500)	$21	3	2	980	22,310	30	ESDI
	EXT-4380	320	$4250 (500)	$13	15	8	980	22,310	30	ESDI
MEMOREX	512	30	$1680 (100)	$56	3	2	970	9912	25	ST-506/412
	513	50	$2005 (100)	$40	5	3	970	9912	25	ST-506/412
	514	70	$2390 (100)	$34	7	4	970	9912	25	ST-506/412
MICROPOLIS CORP	1302	20.4	$975	$48	3	2	960	9077	30	ST-506/412
	1303	34	$1095	$32	5	3	960	9077	30	ST-506/412
	1304	40.8	$1195	$29	6	4	960	9077	30	ST-506/412
	1323	33.5	$1175	$35	4	3	1000	9824	30	ST-506/412
	1324	50.2	$1335	$27	6	4	1000	9824	30	ST-506/412
	1325	67	$1470	$22	8	5	1000	9824	30	ST-506/412
PRIAM	502	55	$1550	$28	7	4	960	9212	32	ST-506/412
	503	71	$1750	$25	7	4	960	11,886	32	PRIAM/ANSI
	504	86	$1850	$22	11	6	960	9212	32	ST-506/412
	505	111	$2300	$21	11	6	960	11,886	32	PRIAM/ANSI
QUANTUM	Q520	16.8	$895	$53	4	2	591	9200	45	ST-506/412
	Q530	25.2	$995	$40	6	3	591	9200	45	ST-506/412
	Q540	33.6	$1095	$33	8	4	591	9200	45	ST-506/412
RODIME	RO206	31.5	$995	$32	6	3	600	8192	60	ST-506/412
	RO208	42	$1115	$27	8	4	600	8192	60	ST-506/412
TANDON CORP	TM703	31*	<$1000	**	5	3	600	10,000	39	ST-506/412
	TM705	50*	<$1000	**	5	3	1000	10,416	39	ST-506/412
VERTEX CORP	V130	24.3	$1100	$45	3	2	960	9920 (MAX)	30	ST-506/412
	V150	40.4	$1400	$35	5	3	960	9920 (MAX)	30	ST-506/412
	V170	56.6	$1650	$29	7	4	960	9920 (MAX)	30	ST-506/412
	V2100	78.7	$1750	$22	7	7	960	16,310 (MAX)	25	ST-412HP

NOTES
1. FORMATTED CAPACITY IN MEGABYTES; ASTERISK DENOTES UNFORMATTED CAPACITY
2. UNLESS NOTED, PRICES IN 1000-UNIT QUANTITIES
3. PRICE/CAPACITY
** NOT APPLICABLE—CAPACITY INDICATED IS UNFORMATTED

Vendors use three approaches to increase maximum capacity

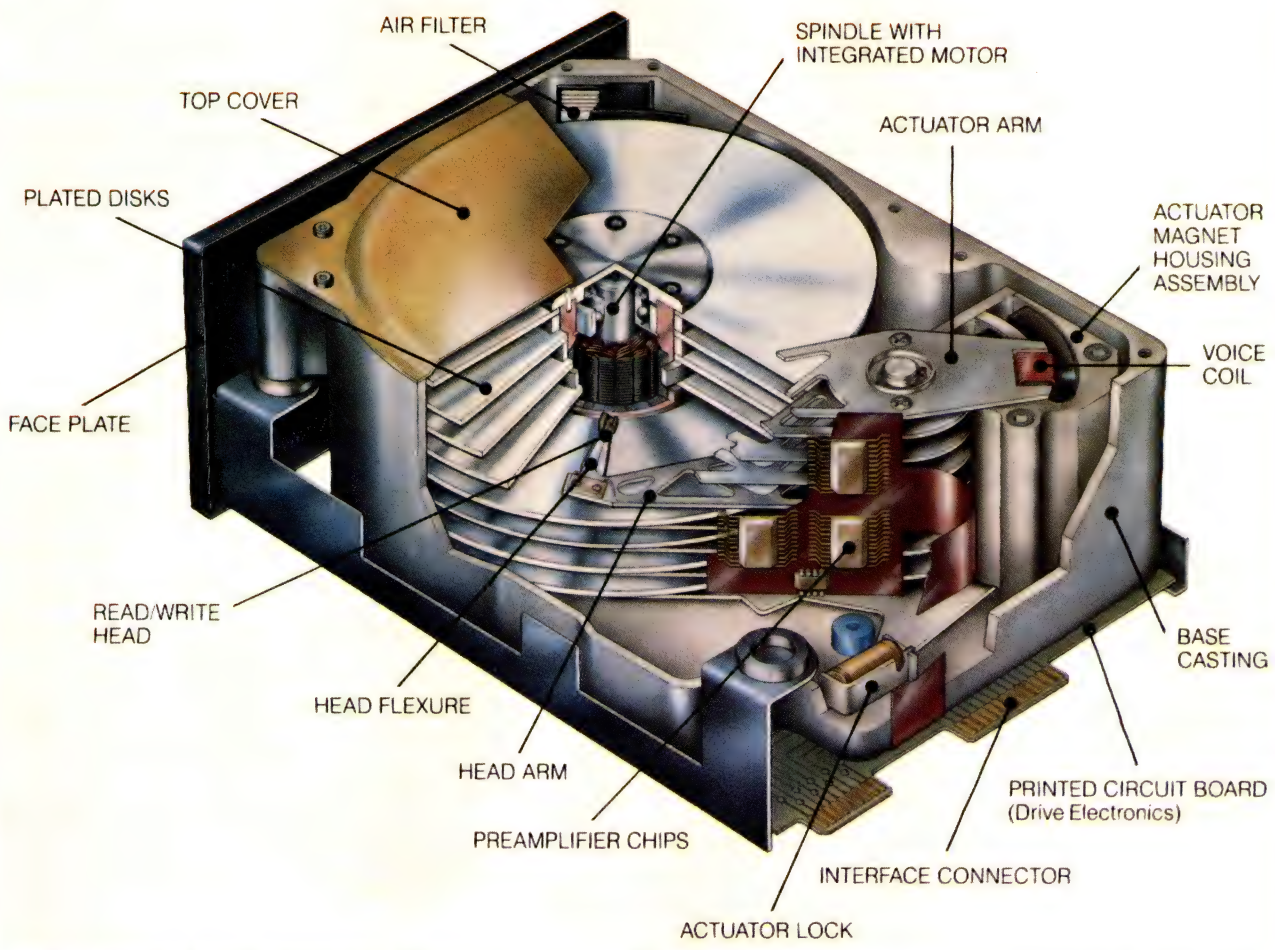


Fig 3—Putting as many platters and heads *in a package as the laws of physics allow, Maxtor's drive squeezes the most out of every inch of space.*

drives. At any technological level, more platters and more heads will produce more storage space. This technique isn't limited to low-end drives. Maxtor manages to push technology and still take advantage of this approach in its tightly packed (enhanced) drives. The firm has a unique spindle motor built into the disk's hub that allows as many as eight platters to sit (closely spaced) within a 5¼-in. package in its EXT-4000 family of drives. The drive also uses a rotary actuator, which takes less space than a linear actuator. **Fig 3** shows the mechanical aspects you need to increase capacity from 75M to 380M bytes in this package size. The 75M-byte version costs $1490 (500); the 380M-byte version costs $4250 (500).

The problem with simply adding heads and platters to gain capacity is that it adds to the mechanical complexity of the drive without necessarily adding any sophistication. Mechanical complexity can reduce reliability. You don't get any particular performance benefit. You might, however, get a cost benefit from putting more storage in one package. But according to Jim Adkisson, executive vice president of Vertex Peripherals, at any given capacity, the most economical and reliable solution involves the fewest heads and disks.

Another method of increasing disk capacity is to increase the density of data tracks. The closer together the tracks are, the more tracks you can record on the disk. The efforts in this area focus on precision positioning mechanisms (the more tracks there are in a given area, the narrower and harder to track they become), better read/write channels and higher resolution media, usually plated media. State-of-the-art 5¼-in. drives exhibit a track density of 1000 tpi max, typically 960 to 980 tpi (**Table 1**). Computer Memories Inc provides an exception—its CM 7000 family boasts 1173 tpi. Computer Memories attributes its unusually high track density to a swing-arm actuator and a closed-loop servo system. To accommodate narrow track widths,

The intelligent disk drive

The push for higher disk-drive capacity makes sophistication within the peripheral important to the success of the application. System throughput increases by allowing a drive to take over disk housekeeping functions now handled by a host CPU, such as error detection and correction, automatic retries and self arbitration.

All rigid disk drives have some media defects. The standard method of handling the inevitable defects that appear on disk surfaces is to provide the customer with a list of locations on each platter which can't be used (**figure**). In microcomputer systems, the system integrator must enter these locations into the system. Unfortunately, as additional platters are added to increase the drive's storage capacity, the number of media defects also increases. With as many as eight platters, the job of entering the defect locations can get out of hand. But there are other ways to handle the problem.

Higher capacity drives require defect mapping, a function easily provided in intelligent drives. Defect mapping makes the location of defects transparent to the system. The drive puts data into good locations and keeps track of where it stores things. Thus, the host computer neither knows nor cares the physical location of data on the disk.

Although intelligence in drives and interfacing has largely been a panacea for large-capacity drives on powerful computer systems, it isn't restricted to those applications. Even in lower capacity drives like Shugart Corp's 706S and 712S, intelligence proves useful. In this particular case, the intelligence ensures that the drives speak the language of the SCSI interface and obviate interfacing to the drive on the native-interface level. The host processor then spends less time dealing with file I/O and has more time for computational tasks. All of the valid arguments in favor of intelligent drives on a large computer system, Shugart contends, apply equally well to a small system where computational power is at a premium.

ERROR MAP MLC-1

CYLIND.	HEAD	BYTE FROM INDEX	CYLIND.	HEAD	BYTE FROM INDEX
128	4	3163			
139	2	7337			
505	2	3613			
801	2	158			
866	1	1208			

An error map *provides the location of every hard defect at the time the drive is shipped.*



Full-height 5¼-in. drives *from IMI store 12M to 51M bytes.*

the drive uses gap-length manganese heads. These narrower-than-normal heads allow the drive to read and write thinner tracks.

The last method of improving storage capacity involves increasing linear density, the density of bits along a track. Given a fixed number of tracks, the more bits you can store in the track the more data you get on the disk. In this arena, 12,000 bpi tends to be a magic number. High-quality thin-film media and quality read/write channels make these barriers reachable in the newer drives, but as the resolution of the media increases, read/write channels must improve to match.

Some data-compression techniques make linear density the easiest target of the three capacity-increasing techniques for drive manufacturers to pursue. Termed run-length-limited coding (RLL), such encoding schemes let the drive store more bits on a track than it has flux reversals. Normally it takes a flux reversal to store a bit. But with RLL, after you've reached the limit of increasing the number of flux changes/in. (fci) in the media, you haven't reached the storage limit of the drive. RLL compresses the data so that it takes fewer bits written on the disk to store a certain number of data bits. Each bit written represents more than one data bit.

RLL codes compress data to achieve a density increase

Maxtor's EXT-4000 family proves the point. This drive incorporates the (2,7) RLL code dictated by the ESDI (enhanced small-disk interface) specification. The drive's combination of plated media and high-performance read/write channel supports 14,873 fci, yet the drive stores 22,310 bpi through (2,7) encoding. Because this scheme depends on an efficient encoding of data rather than a technological development, the technique is available to all manufacturers without incurring an additional large development or manufacturing cost. It is the most economical approach to higher capacity.

Micropolis Corp's newest 5¼-in. Winchester drive also takes advantage of (2,7) coding. Its 1350 Series sports the ESDI interface and storage capacities ranging from 85M to 170M bytes. This indicates an avowed trend toward RLL among high-capacity disk vendors with the exception of Computer Memories. Its CM 7000 drives feature a low 9275-bpi linear density but push track density to the limit.

The high-capacity drives listed in **Table 1** use these three techniques in varying degrees to reach their particular storage level. Some manufacturers, such as Micropolis and Priam, loudly announce that they aren't on the leading edge of any technology but follow closely behind with proven (ie, manufacturable in high volume) technology. This they find a safe, yet competitive, course to follow. Of all the manufacturers, only Maxtor chooses to assault all three techniques with vigor.

Going upscale for performance

Some manufacturers, meanwhile, are also increasing disk storage capacity, but are doing so without adopting the newest technologies. For instance, Seagate Technology, an established front runner in low-capacity 5¼-in. Winchesters, chose to move to an 8-in. form factor for its entry into the multiuser-system marketplace. Putting the requisite capacity and performance into an 8-in. drive, while keeping costs down, proved much simpler than accomplishing the same feat in a 5¼-in. package. Seagate wanted to incorporate a drive that could store 100M bytes (unformatted) of data and furnish an average access time of 30 msec into a half-height package. The result was the highly manufacturable ST8100. The $1500 (OEM) drive uses the firm's own ST-412HP interface (and its ST9100 controller) to transfer data at 10M bps.

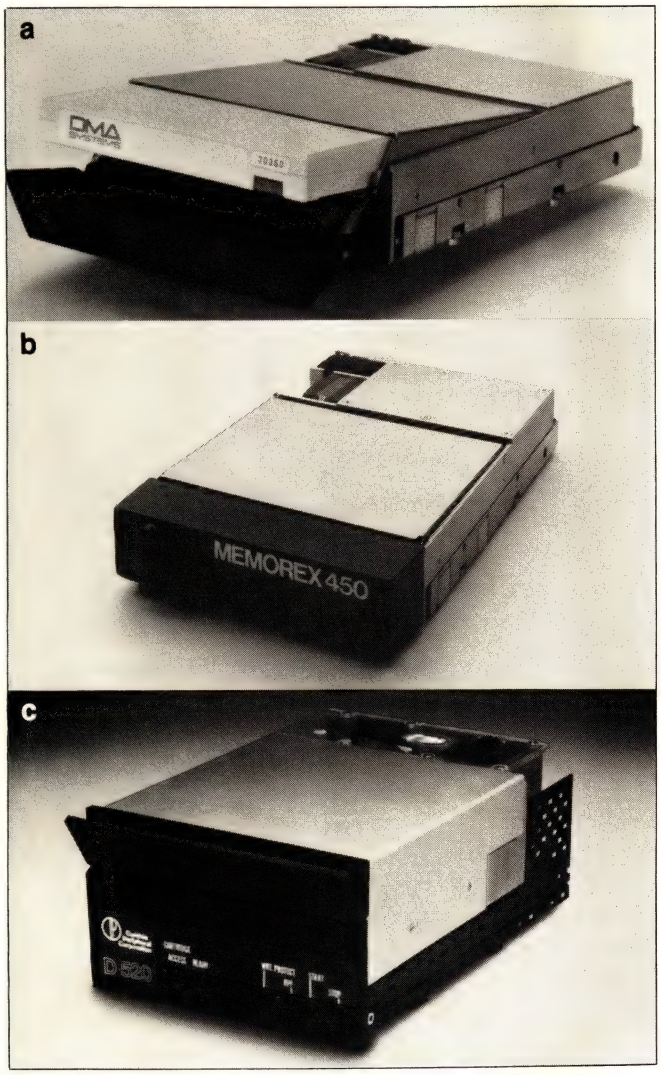
Seagate isn't the only manufacturer turning to 8-in. drives as cost-effective alternatives to 5¼-in. units. In fact, firms such as Priam, Micropolis and Quantum moved to 5¼ in. only after establishing themselves as vendors of 8-in. drives. More important, many of these firms also possess 14-in.-drive technology. As a result, these vendors are transferring much of the technology they've perfected for larger drives to the smaller packages. And according to Larry Jacobs, Priam's product marketing manager, vendors who have been in the large (8- and 14-in.) Winchester drive business for a while bring something else to the party: a knowledge of the requirements of multiuser systems. That knowledge pays dividends in getting things right the first time. "User feedback is no substitute for good design," says Jacobs.

It's important to keep in mind that some manufacturers choose to remain in the larger drive market and

Analyzing disk-drive specifications

Disk-drive specs can be confusing. Understanding them can go a long way toward ensuring that the drive you ultimately select meets your system needs. Bob Mortenson, product requirements manager at Micropolis Corp, offers the following advice when dealing with disk-drive manufacturers to help you get through this critical phase:

- Ask about the drive's capacity and compare formatted capacities rather than unformatted. Drives with equal unformatted capacities can differ in their actual storage capacity.
- Check the physical size. Some drives exceed the 8-in. length requirement for the 5¼-in. form factor, Mortenson warns. Check the mounting orientations that the manufacturer permits while you're at it. Some drives must be mounted along one or two of the three possible mounting axes.
- Look for separate reliability specs for the HDA (head/disk assembly) and the electronics. Circuit boards are field replaceable, but a failure in the HDA will mean that the drive returns to the vendor—quite likely destroying all the data stored on the disk in the process.
- Ask manufacturers how they measure average access time. Many data sheets *don't* define the term "average." The most widely accepted method is to use the time of a ⅓-length seek; the average distance is considered to be ⅓ of the total number of cylinders. Look for a drive's ability to seek and buffer step-pulses simultaneously (allowing the drive to begin its seek operation when it receives the first step pulse). This will produce faster seeks in real system operation.



Some drives provide their own means of data backup. *The DMA 360* ***(a)*** *from DMA Systems Corp and Model 450* ***(b)*** *from Memorex Corp furnish only removable cartridges. Cynthia Peripheral's Model D520* ***(c)*** *combines both the cartridge and a fixed disk.*

resist the temptations of the 5¼-in. format. Their offerings shouldn't be ignored in planning your system design. The 8-in. form factor offers sufficient space to incorporate high-performance technologies without significantly impacting price. Northern Telecom's Mercury Series of drives, for example, provide average access times of 20 to 25 msec and capacities ranging from 35M to 174M bytes. The drive has an SMD interface.

The Kennedy Company is also introducing a new 8-in. drive, the Model 73160, at the National Computer Conference in Las Vegas next month. The $4695 drive furnishes 165.9M bytes of (unformatted) storage and features a new rotary actuator with four fixed rare-earth magnets, which allows an average access time of 20 msec. You can choose SMD, ANSI or PICO native interfaces for the drive to suit your needs.

In spite of the hoopla over high capacities, it's the low-capacity Winchesters that have created the marketplace for the 5¼-in. form factor, and their capacity and performance continues to increase. Today's 10M- and 20M-byte drives typically come in smaller (half-height) packages than the space-wasting, full-height 5M- and 10M-byte drives of not too long ago. What's more, system integrators can find in the smaller drives a flexible alternative to more expensive high-capacity drives. Some of the more sophisticated controllers on the market will let you interleave seeks on multiple disks to achieve faster performance and larger capacities than you can obtain from single 5¼-in. drives.

Not all low-capacity drives, however, use 5¼-in. media. The demand for rigid disk drives for portable and transportable computers is causing vendors to look at even smaller media and package sizes—sub-4-in. drives to be specific.

Good examples of sub-4-in. developments are the Models SQ312, -325 and -338 drives from Syquest, which use 3.9-in. (100-mm) media with a proprietary ChromaFlux overcoating to store 10M, 20M or 30M bytes of data. The entire package measures 1.625×4.8×8 in., including the pc board, and weighs 2.9 lbs. Much of Syquest's design effort focuses on preparing its drives to face the shocks of working in the transportable world. The manufacturer runs fragility tests on a shock-test machine to ensure that failures due to shock are well understood and that the drive will withstand reasonable impacts. Both a step-acceleration test (simulating dropping the drive onto a stiff surface) and a shock-transmission test, where the machine pulses the drive with a 15g and 20g, 11-msec, ½-sine shock pulse, are employed to determine the drive's ability to withstand battering under normal handling.

In an even smaller package size, you'll find Rodime's Model RO350 Series of 3½-in. Winchesters. These drives incorporate as much as 10M bytes in a 1.625×5.75×4-in. package. Featuring average access times of 90 msec, the tiny Winchesters interface to an ST-506 controller.

Half-height drive—full-height performance

In the larger 5¼-in. disk format, the emphasis is currently on half-height drives. A half-height Winchester, combined with a half-height floppy disk or cartridge tape drive, packs a lot of storage in the space formerly allocated to a single disk drive.

Shugart Corp puts 5M and 10M bytes in its Model 706 and 712 half-height Winchester drives for a mere $444 (OEM) and $499 (OEM), respectively. The half-height 5¼-in. form factor has been around for some time now and is understood sufficiently so that reliability problems are almost nonexistent. Shugart's 700 Series

Holographic testing of disk drives

Rudy Garza, *Newport Corp*

As track densities pass the 1000-tpi mark, head-positioning problems associated with vibration and thermal deformation become major concerns. How do you measure mechanical movements of 5 to 10 μm? How do you characterize resonance in the flexure when the mass of an accelerometer is large enough to change both the resonant frequency and mode shape? One answer is holography. Recent advances in holography make it simple and convenient to measure and record such data.

Thermal deformation

Most drives have the carriage and spindle mounted on a common base plate. Heat from internal components and the environment can cause differential expansion or warpage of the base plate, resulting in a misalignment of the carriage and spindle. Holographic interferometry records these changes in real time.

The first step is to make a hologram (essentially a 3-dimensional laser photograph) of the base plate using a test setup such as the one shown in **Fig A.** This becomes the reference pattern. After applying thermal stress (you heat the drive), take a second picture, and superimpose it over the reference pattern. This produces a double exposure in real time that records the changes that have taken place in the base plate under thermal stress. The black and white fringes shown in **Fig B** are interference patterns produced by changes in the base plate.



Fig A—A stable test setup *lets you create a double-exposure holographic image.*

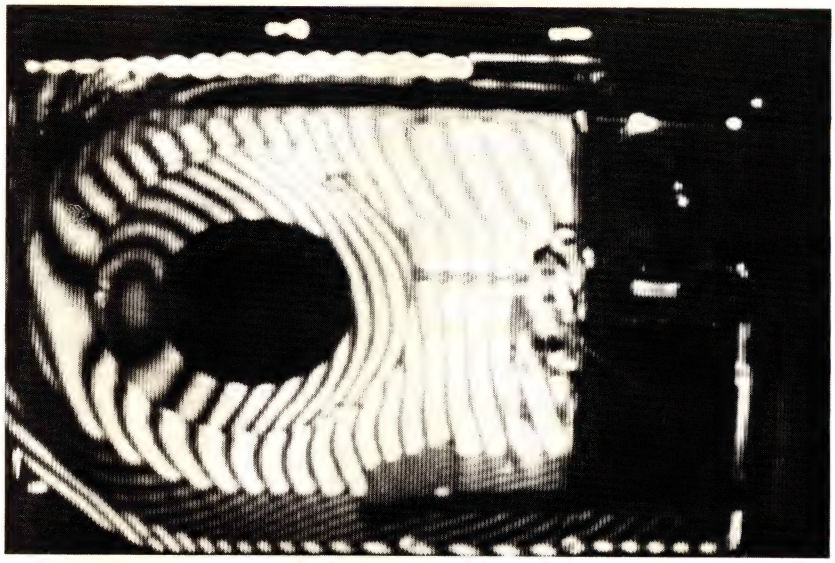


Fig B—Interference patterns *show changes in the base plate due to thermal stress.*

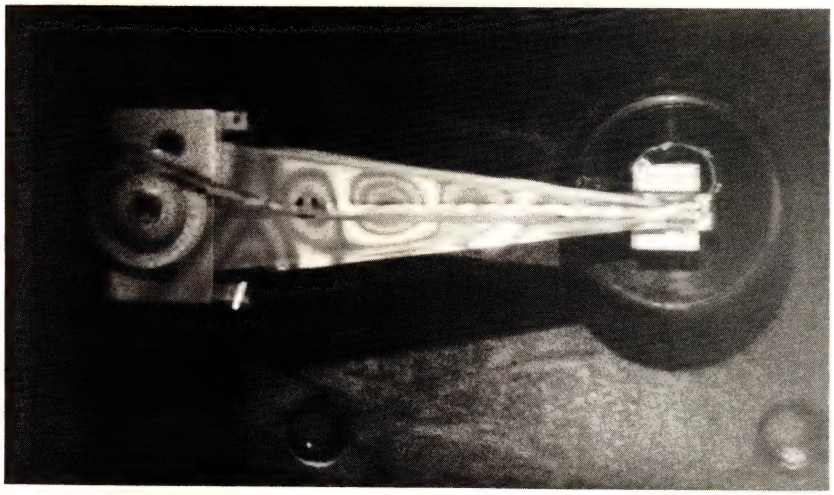


Fig C—When you see fringes *across the time-average hologram of the flexure, you've found one of its resonant frequencies.*

You can read the amount of stress by interpreting the fringes as you would contour lines on a topographical map. The elevation between successive fringes is ½ the wavelength of a helium-neon laser, 12.4 μm. The bullseye pattern is a bulge in the bottom of the plate.

This noncontact measurement technique works as well for vibration as it does for heat. With a hologram you can watch the entire flexure vibrate and identify various resonant frequencies. By vibrating a flexure assembly across various frequencies until you see a standing wave in the double exposure as shown in **Fig C.** The fringes represent an incremental 9- to 13-μm vibration (depending on the laser's wavelength).

Rudy Garza *is manager of technical marketing development for the Fountain Valley, CA-based Newport Corp.*

Lower technology in 8-in. drives furnishes high performance

TABLE 2—LOW-CAPACITY WINCHESTER DISK DRIVES

MANUFACTURER	MODEL	FORMATTED CAPACITY (M BYTES)	HALF HEIGHT	PRICE (1000)	COST ($/M BYTE)	AVERAGE ACCESS TIME (MSEC)
COGITO SYSTEMS	CG-912	10	YES	$585	$59	85
IMI	2306H	5	YES	$420	$84	85
	2312H	10	YES	$515	$52	85
MICROSCIENCE INT CORP	HH-612	10	YES	$810	$81	85
RODIME	RO 351	5	YES	$470	$94	92
	RO 352	10	YES	$590	$59	92
SEAGATE TECHNOLOGY	ST 406	5	NO	*		65
	ST 412	10	NO	*		65
	ST 419	15	NO	*		65
	ST 425	20	NO	*		65
	ST 212	10	YES	*		65
SHUGART CORP	706	5.24	YES	$444	$85	85
	712	10.49	YES	$499	$48	85
SYQUEST TECHNOLOGY	SQ325F	20	YES	$700		<100
	SQ338	30	YES	$850		<100
TANDON CORP	TM251	5	YES	$425	$85	85
	TM252	10	YES	$500	$50	85
TULIN CORP	TL-226	20	YES	$850	$43	95
	TL-240	30	YES	$1055	$35	95

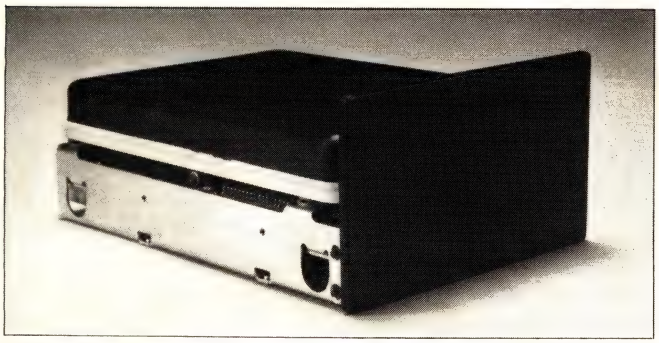
*MANUFACTURER REQUESTS THAT OEMs CONTACT THEM DIRECTLY FOR PRICING.

drives boast 20,000-hr MTBFs.

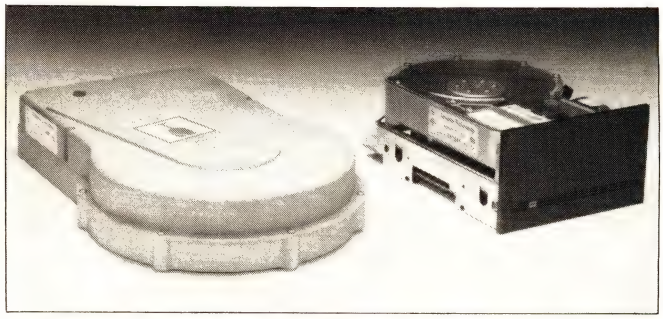
To reduce interfacing and system housekeeping problems, you can even specify intelligent versions of these drives, designated Model 706S and 712S. These drives feature the SCSI interface as your access point to the drive. On-board intelligence tackles logic jobs normally handled by the disk controller. The price for intelligence? Model 706S costs $661 (OEM) and the 712S costs $716 (OEM). The intelligence in the drive takes care of such tasks as disk formatting, error detection and correction and defect mapping.

Meanwhile, Seagate Technology's half-height ST212 drive not only provides 10M bytes of storage, but also uses two heads on each platter to furnish an average access time of 65 msec. Seagate is so confident of the quality of its products that it gives OEMs a 105% guarantee. If you buy more than 500 drives for US delivery and one of the drives fails incoming inspection, Seagate will repair and return the drive and issue you an additional 5% credit.

Because not everyone wants or needs a half-height drive, in addition to its ST212, Seagate meets a wider



Putting intelligence within the drive, *Shugart Corp's 700S Series of drives provide 5M or 10M bytes of storage and an SCSI interface.*



Two faces of data storage *are Seagate Technology's 100M-byte half-height 8-in. ST8100 Winchester and its 12M-byte 5¼-in. ST412 Winchester.*

Half-height low-capacity drives drive larger units upscale

range of system storage requirements, from 5M to 20M bytes, with its full-height ST400 family of drives.

International Memories Inc has also put its marketing faith in half-height drives for 5M- and 10M-byte packages. Its 2306H and 2312H offer 85-msec average access times for as little as $420 (1000) for the 5M-byte 2306H.

One newcomer to the disk-drive market, Tulin Corp, is pushing the limits of half-height packaging by providing as much as 30M bytes (Model TL-240) with a 95-msec average access time. If you don't need quite that much capacity, the company also makes the TL-226 and TL-213 drives at 20M or 10M bytes, respectively.

Although drive manufacturers like those mentioned are aiming products at broad application areas, some firms have chosen to customize their units for particular systems. The current spotlight is on storage systems and modules for IBM PCs, but there are other dedicated systems as well. Texas Instruments, for example, makes drives for its Professional Computer. Its full-height 10M-byte drive suits use in the desktop computer, and its half-height 10M-byte drive fits either the desktop or transportable computer. Intended for end-user markets, either drive retails for $2295 and has an 85-msec average access time.

Table 2 compares the particulars of a cross section of low-capacity drives in order to illustrate the tradeoffs in package size, capacity and performance that are available.

Cartridges create portable data

Once you have decided on a particular disk drive for your application, you might want to consider some sort of backup storage system. Like choosing drives, choosing the optimum system is not as simple as looking through a product catalog. Although the issue of which method is best to back up the data stored on a Winchester might never be resolved, the manufacturers of cartridge drives continue to push their products as viable alternatives to floppies or tape. The rationale behind using cartridges is the ultimate convenience that they offer. Backup is quick: One cartridge backs up one similar-sized fixed disk and you have only a single peripheral to deal with.

The smallest cartridge drive comes from Syquest. Its Model SQ-306RD measures a mere 1.625×4.8×8 in. and weighs 2.4 lbs. Its Q-Pak cartridge is less than 5 in. wide and less than ½ in. thick, letting you stash the media in a coat pocket. Where space is a problem (space in the system for the drive and space to store data cartridges), the SQ-306RD excels. These cartridge drives cost $480 (1000). Each data cartridge ($60 in 1000s) stores 5M bytes (formatted) in 306 cylinders, and the drive features an average access time of 90 msec.



Imported to the US from Scotland, *Rodime's RO 208 drives store 53.3M bytes and feature a 50-msec average access time.*

But this drive has *only* removable storage. You might need to add a fixed disk to obtain the performance your system requires and let the cartridge act as a backup device only.

In a slightly larger format, you'll find DMA Systems' Model 360 provides more removable storage capacity. For applications where costs must be kept low, this removable-only half-height drive packs 7.5M bytes on a 5¼-in. cartridge for less than $500 (OEM). Its average access time is 98 msec.

To pack even more data storage in the same size package, consider the Memorex 450 5¼-in. cartridge drive. It stores 12.75M bytes (unformatted) on two data surfaces and furnishes an average access time of 98 msec. Priced at $960 (100), Model 450 fits in the footprint of a half-height 5¼-in. floppy drive and consumes 25W typ; it uses the ST-506 interface.

Another cartridge candidate in this capacity range is Cynthia Peripheral's D520 drive. Priced at $1380 (OEM), the unit combines 10M bytes (formatted) of removable cartridge storage with 10M bytes (formatted) of fixed-disk storage. If its price tag is higher than the other cartridge drives, so is its performance—a 40-msec average access time.

DMA Systems also provides the fixed/removable combination. Its Micro-Magnum 11/11 combines 11M bytes of fixed storage with the same amount of removable-cartridge storage. Compatible with and intended for use with the IBM PC/XT, the Micro-Magnum 11/11 costs $1525 (1000); the removable-only version, the



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Micro-Magnum 11R, costs $1190 (1000).

Yet another manufacturer, Athenaeum Technology Inc, provides its Aegis 1010 for applications requiring 11.47M bytes of fixed and removable storage. A linear voice coil, shock isolated from the casting to prevent ringing errors, furnishes a 40-msec average access time. The drive costs $1300 (1000) (an evaluation unit costs $2500) and uses standard 5¼-in. cartridges. **EDN**

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

References

1. Gibeau, F C and Brown, S F, "Wringing higher performance from 5¼-in. Winchesters," *Mini-Micro Systems*, February 1983.
2. Teja, E R, *A designer's guide to disk drives*, Reston Publishing Co, 1984.
3. "The average seek time: Fact or fiction?," The IRIS Connection, Vol/No 1, Point 4 Data Corp.

Manufacturers of Winchester disk drives

For more information on the disk drives mentioned in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Ampex Corp
Computer Products Div
10435 N Tantau Ave
Cupertino, CA 95014
(408) 255-4800
Circle No 711

Atasi Corp
2075 Zanker Rd
San Jose, CA 95131
(408) 995-0335
Circle No 712

Athenaeum Technology Inc
105 Bay State Dr
Braintree, MA 02184
(617) 848-8388
Circle No 713

Cogito Systems
2355 Zanker Rd
San Jose, CA 95131
(408) 942-8262
Circle No 714

Computer Memories Inc
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Chatsworth, CA 91311
(818) 709-6445
Circle No 715

Control Data Corp
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Minneapolis, MN 55440
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Circle No 716

Cynthia Peripheral Corp
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Circle No 717

DMA Systems
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Manufacturers of 8-in. drives mentioned in this article:

Kennedy
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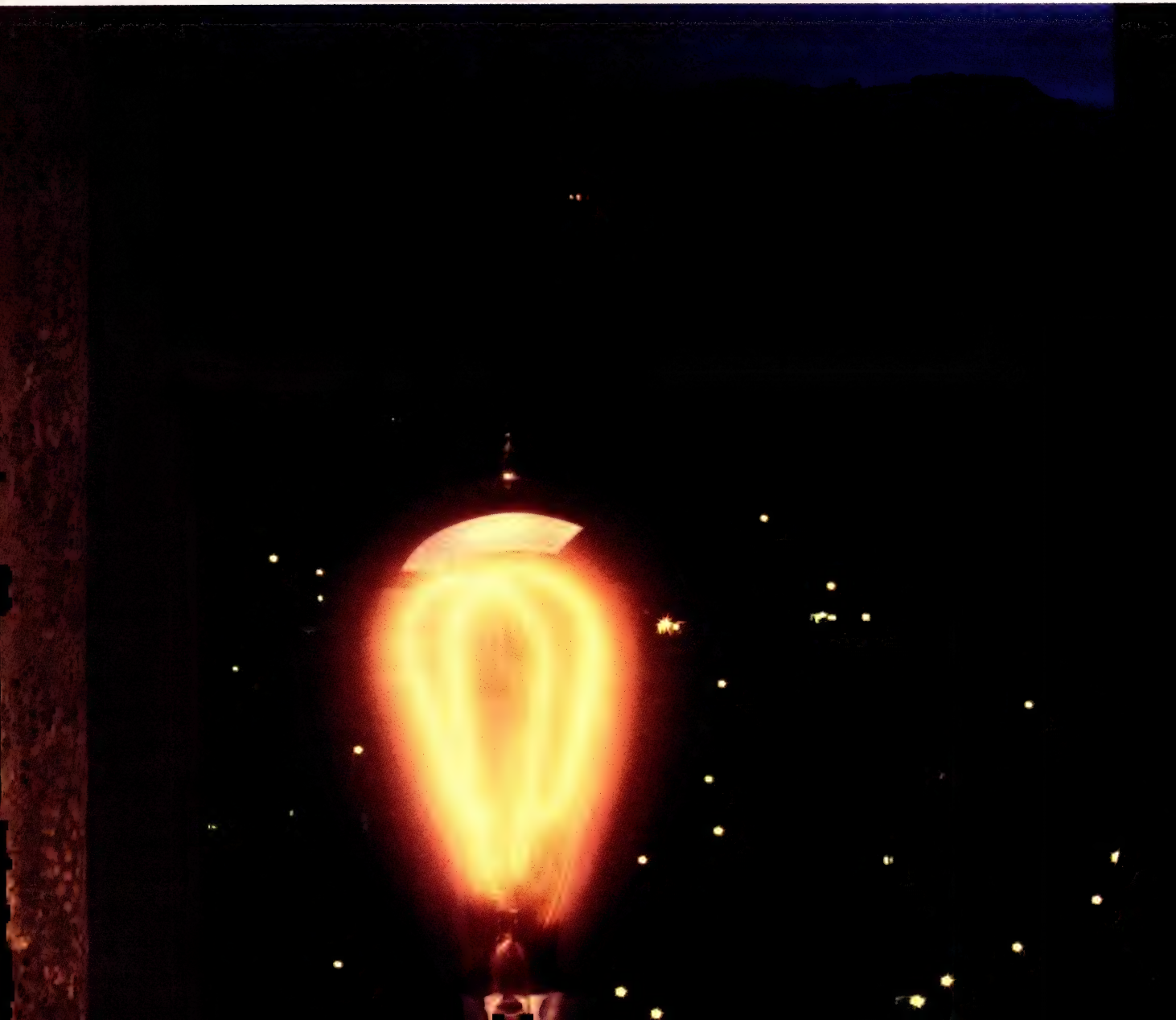


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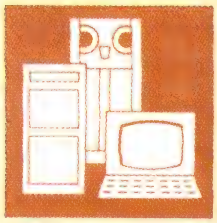
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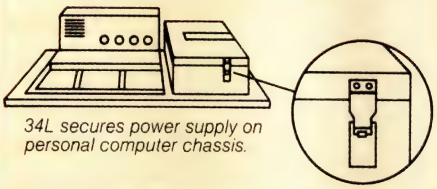
Latches for Electronic

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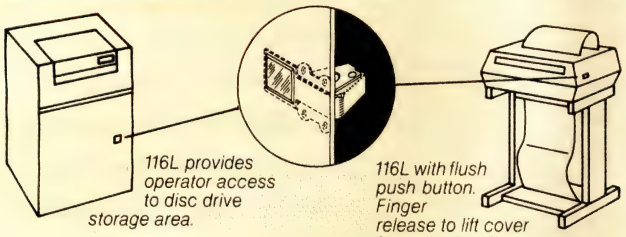
Typical Applications



Electronic Computing

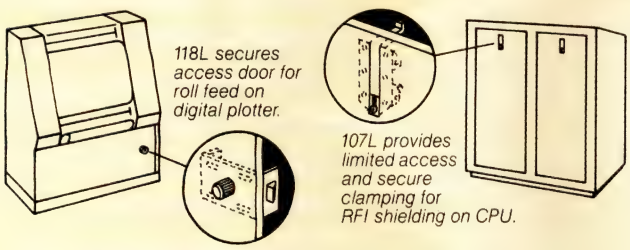


34L secures power supply on personal computer chassis.



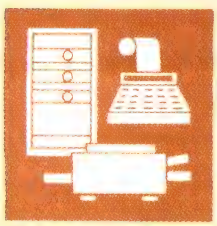
116L provides operator access to disc drive storage area.

116L with flush push button. Finger release to lift cover for paper loading on printer.

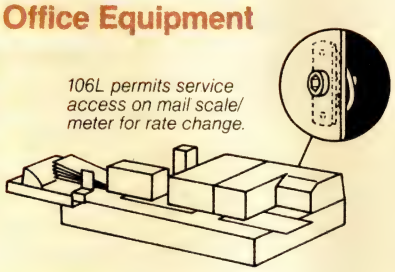


118L secures access door for roll feed on digital plotter.

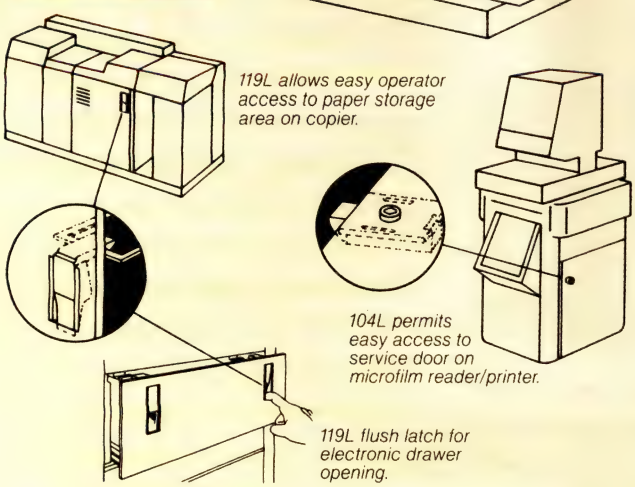
107L provides limited access and secure clamping for RFI shielding on CPU.



Office Equipment



106L permits service access on mail scale/ meter for rate change.



119L allows easy operator access to paper storage area on copier.

104L permits easy access to service door on microfilm reader/printer.

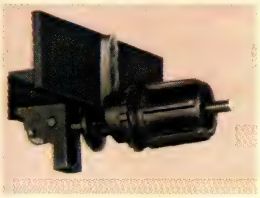
119L flush latch for electronic drawer opening.



Camloc III Tension Latches

34L Series. Miniature latch; available with secondary lock. **112L Series.** Small, yet high strength (600 lbs.). Self-compensating for variable loads. **47L Series.** Low profile, large take-up. Styling characteristics of similar plastic versions but is trouble free. **95/96L Series.** Attractive style. Available in two sizes; numerous materials/finishes. **51L Series.** Adjustable series; over 200 variations: secondary locks, right angle bases, extended drawhooks, etc. **30L Series.** Miniature latch. High strength to weight ratio.

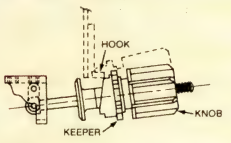
CIRCLE NO 222



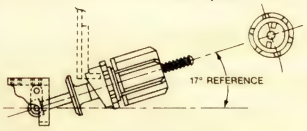
Tridair III Hold-Down Device

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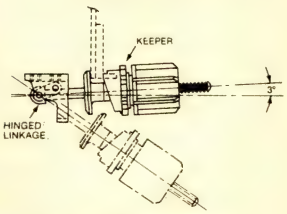
*ARINC specifications specify a clamping force of 100 to 125 lbs.



1. *Assembly lifts to clear NAS 622 hook. Keeper is rotated to captivate clamp assembly to the hook. Knob is rotated to seat the box in place.*



2. *Fully installed in locked position.*



3. *Shown here in the extraction mode. To release from hook, keeper is rotated and assembly falls free.*

CIRCLE NO 223

Equipment

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Camloc III Panel Latches

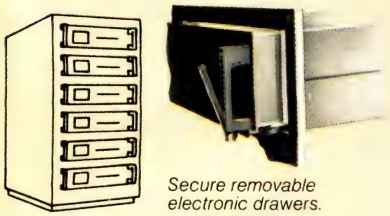
104L Series. Slams to close, 1/4-turn to open. No strike required. Available with 6mm hex for tool operation. **118L Series.** Open by turning 60° in either direction. Available with decorative knobs and 4mm hex recess. **107L Series.** Flush trigger latch. Ideal for gasketed applications. **106L Series.** Self adjusting pawl compensates for tolerances and gasket wear. Tool or hand actuator. **65L Series.** Manually adjustable where positive joint compression and high strength is needed to compress gaskets or suppress vibration. **119L Series.** Hand installed; requires only finger operation to open. **116L Series.** Push button to open; slam to close. Clean, unobtrusive design.

CIRCLE NO 224



Camloc III Chassis Latches

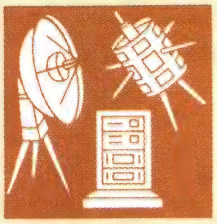
Provide mechanical advantage to engage and disengage drawer from pin connectors. Also function as carrying handles. Ideal for compressing RFI/EMI shields as well, or securing chassis equipment against high tension and shear loads.



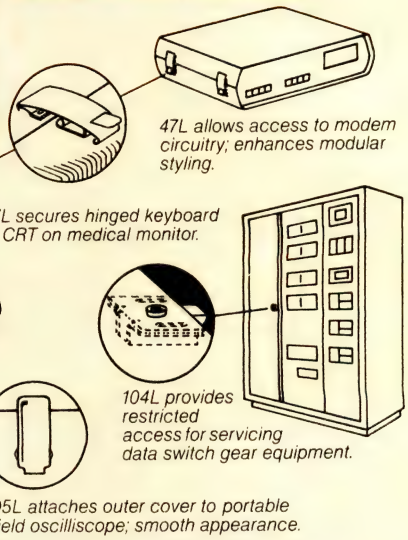
Secure removable electronic drawers.

CIRCLE NO 225

Typical Applications



Instrumentation and Telecommunications



47L allows access to modem circuitry; enhances modular styling.

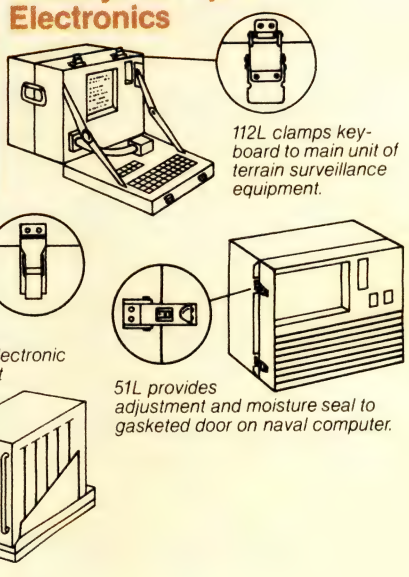
47L secures hinged keyboard to CRT on medical monitor.

104L provides restricted access for servicing data switch gear equipment.

95L attaches outer cover to portable field oscilliscope; smooth appearance.



Military/Aerospace Electronics



112L clamps keyboard to main unit of terrain surveillance equipment.

30L latches interconnect electronic countermeasure equipment modules. Low profile.

51L provides adjustment and moisture seal to gasketed door on naval computer.

Hold down devices secure avionic drawer equipment.

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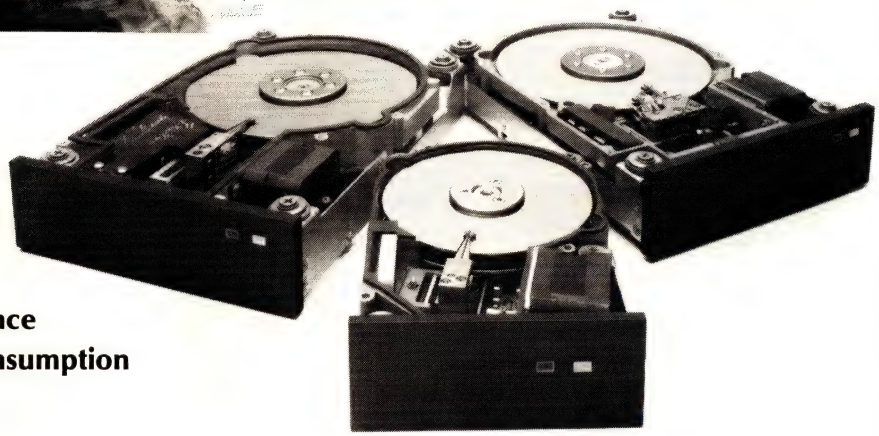
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Additional LSI and hybrid parts ease completion of LAN

Bringing up the completed LAN-node breadboard turns out to be surprisingly easy. Three volume-produced devices perform the difficult token-passing and line-interfacing tasks.

Robert H Cushman, *Special Features Editor*

An effective way of achieving a shared-RAM data link between two asynchronously coupled systems was described in the second article of EDN's networking-design series (**Ref 2**). That article highlighted the operation of an interface between SMC's 9026 LAN controller and a host μP. In this final installment, we'll describe the completion of our networking breadboard. We'll also describe the ultimate test of our system—integrating the breadboard into an existing network to see if it communicates with other nodes.

It turns out that in selecting ARCnet, we made an excellent choice of a LAN to breadboard. The ARCnet LAN is a good example of a mature, well-engineered system. Its history has been sufficiently long (it was introduced in the mid-1970s) to permit elimination of all the bugs. What's more, it's so well supported by LSI and hybrid devices that it wasn't too difficult to breadboard.

Fig 1 illustrates our complete breadboard system. The interface between our 65C02 host μP and the 9026 controller chip (boards 1, 2 and part of 3a) was completed during the preparation of this series' second article. We'll now describe the interface between the 9026 LAN controller on board 3a and the BNC network cable connector on board 4. There is also an extension to the system, board 3b; this extension carries the switches by which a user manually sets the ID (identification number or network address) of the node.

The parts go together nicely

Fig 2 diagrams the circuitry that comprises boards 3 and 4. You'll note that the LAN-cable interface side of the 9026 controller requires much less wiring and fewer glue parts than the interface to the host μP. In fact, the dedicated ARCnet devices are so well matched to the application and to each other that this portion of the breadboard project proceeded rather easily.

As with other LANs, the ARCnet protocol can be unusual and confusing, particularly when establishing and maintaining the token-passing scheme. Fortunately, the 9026's microcode automatically takes care of the necessary protocol. Indeed, we found that we really didn't have to understand it in great detail in order to bring the system up.

Similarly, the hardware-design problems are, for the most part, taken care of by the 9032 transceiver and the hybrid cable interface. About all that is left for the designer to do is see that the parts are properly connected and know enough about the operation of the system to make waveform checks and write the simple software for the basic operational tests.

What the parts do

Even though the 9032 eliminates much of the hardware you'll need, it's not a very complex device when compared with the 9026 controller. This transceiver is a gate array that replaces only six to eight TTL parts. It operates from the 20-MHz signal of the 0.1%-tolerance crystal oscillator, and it uses this signal as a clock for encoding and decoding the transmitted and received signals. The 9032 also divides the 20-MHz signal by 4 to produce the two 5-MHz clocks required by the 9026.

During transmission, the 9032 takes the TX pulses from the 9026 and converts them into the pair of P1 and P2 pulses that the LAN hybrid converts to the +10V, −10V "dipulse" that's transmitted over the cable.

On the receive side, the 9032 takes the RCVD positive pulses from the hybrid and converts them to

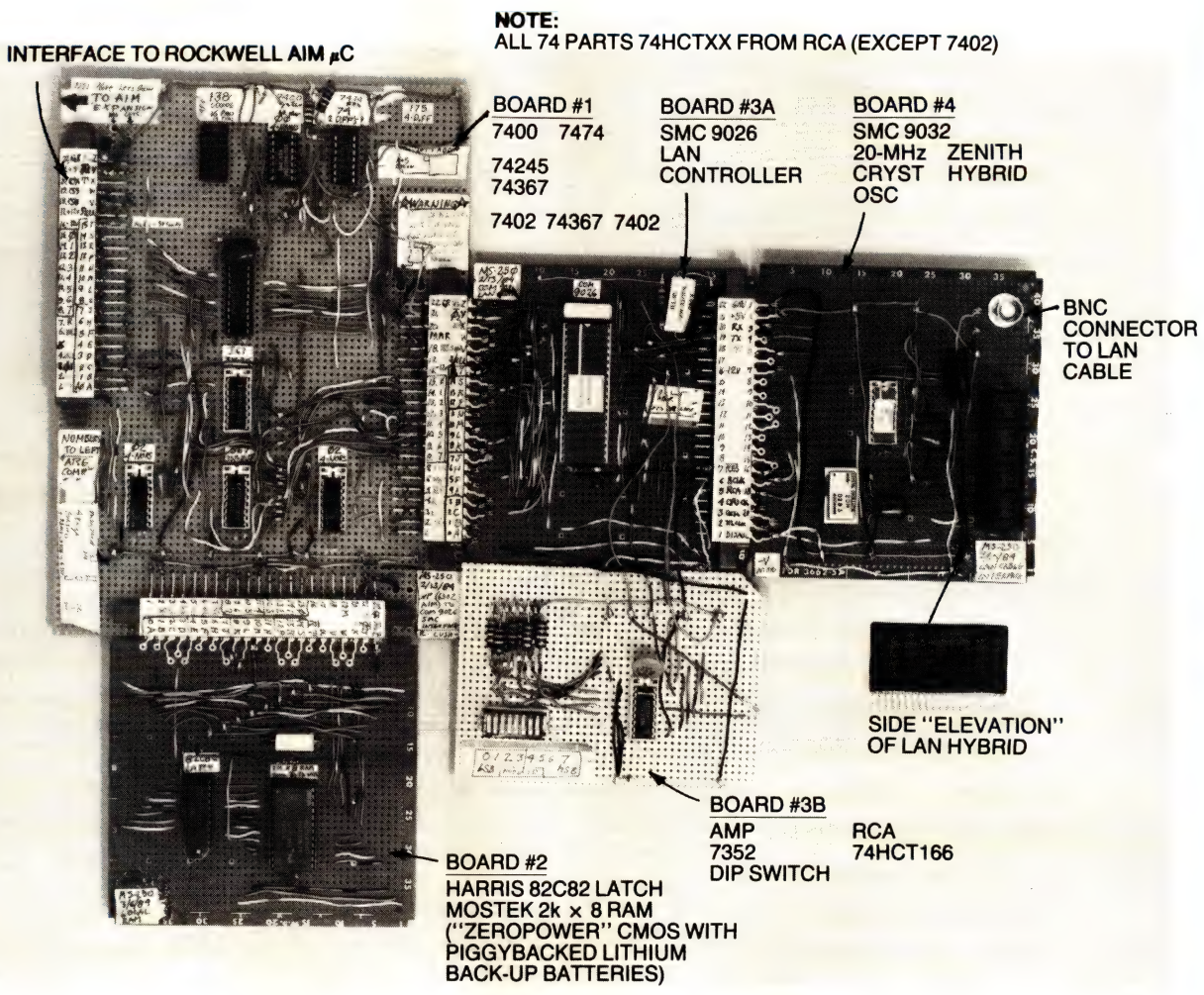


Fig 1—The breadboard designed for EDN's network *is composed of easily disconnected modules, which permit easy troubleshooting and modification. Based on the number and types of ICs, we estimate that it would cost $100 to make a similar breadboard, and that a product based on it would sell for approximately $300. As component prices come down, such a product could eventually sell for as little as $100. Note we used a Mostek Zeropower RAM. This wasn't necessary (an ordinary 2k × 8 RAM is adequate), but the built-in lithium backup battery gives us the luxury of saving test messages during breadboarding and trials.*

the NRZ signal that the 9026 expects to see. The DSYNC control from the 9026 stops the CA clock so that there is byte-by-byte synchronization of the data detection during reception.

The hybrid module is the most interesting part available for this interface. Its operation reveals some of the problems you might encounter when interfacing to a LAN cable that's perhaps one-third of a mile long (2000 ft). On the transmission side, both paths inside the 75453B line drivers (made by Texas Instruments and others) are paralleled to produce the fairly hefty push-pull dipulse.

In Datapoint's original design, this square pulse cycle was sent out directly to the cable, but FCC noise requirements forced the company to add the zero-insertion lowpass LC filter shown to round the wave shape into an approximate sine wave. A tiny 6-pin-DIP RF transformer couples both the transmit and receive signals to the 92Ω RG-62 coaxial cable. The transformer keeps each station on the network sufficiently isolated to ensure that, if one station should lose power, it won't interfere with system operation.

On the receive side, there is another LC filter and a 75108A line receiver. This filter is of particular importance to the success of ARCnet. It's a transcendental-type filter that's matched to the fundamental frequency

of the sine wave that the dipulse is approximating, and it sharply rejects all other frequencies. In fact, the need for sharp frequency rejection is precisely the reason why a dipulse is used: It's an easy signal to detect. Datapoint says that its system can continue functioning even when a noise signal that's larger by an order of magnitude is present.

At the current price of $9 a piece (dropping to $6 in quantity), most users will find, as we did, that these multisourced hybrids are quite convenient to use. Our particular design employs a unit from Zenith CRT & Components Operations (Glenview, IL), but the hybrids are also available from Centralab Inc (Milwaukee, WI), Micro-Technology Inc (Menomonee Falls, WI) and Kyocera America (San Diego, CA).

Before the final test of our breadboard—incorporating it within an actual LAN—we performed some local checks to ensure that it was functioning properly. In one check we looked at the contents of the 9026's status register (at memory-space location 9000 in our system). This register always read "F5," which agreed with the 9026's specification folder with respect to the status bits that should be set following a power-on-reset (POR).

The first two RAM locations (8000 and 8001 in our system) were also checked. After a POR, the first location was set to "DI." The DI, according to SMC, represents the proper result of the 9026's power-up initialization. It verifies the 9026's instruction code,

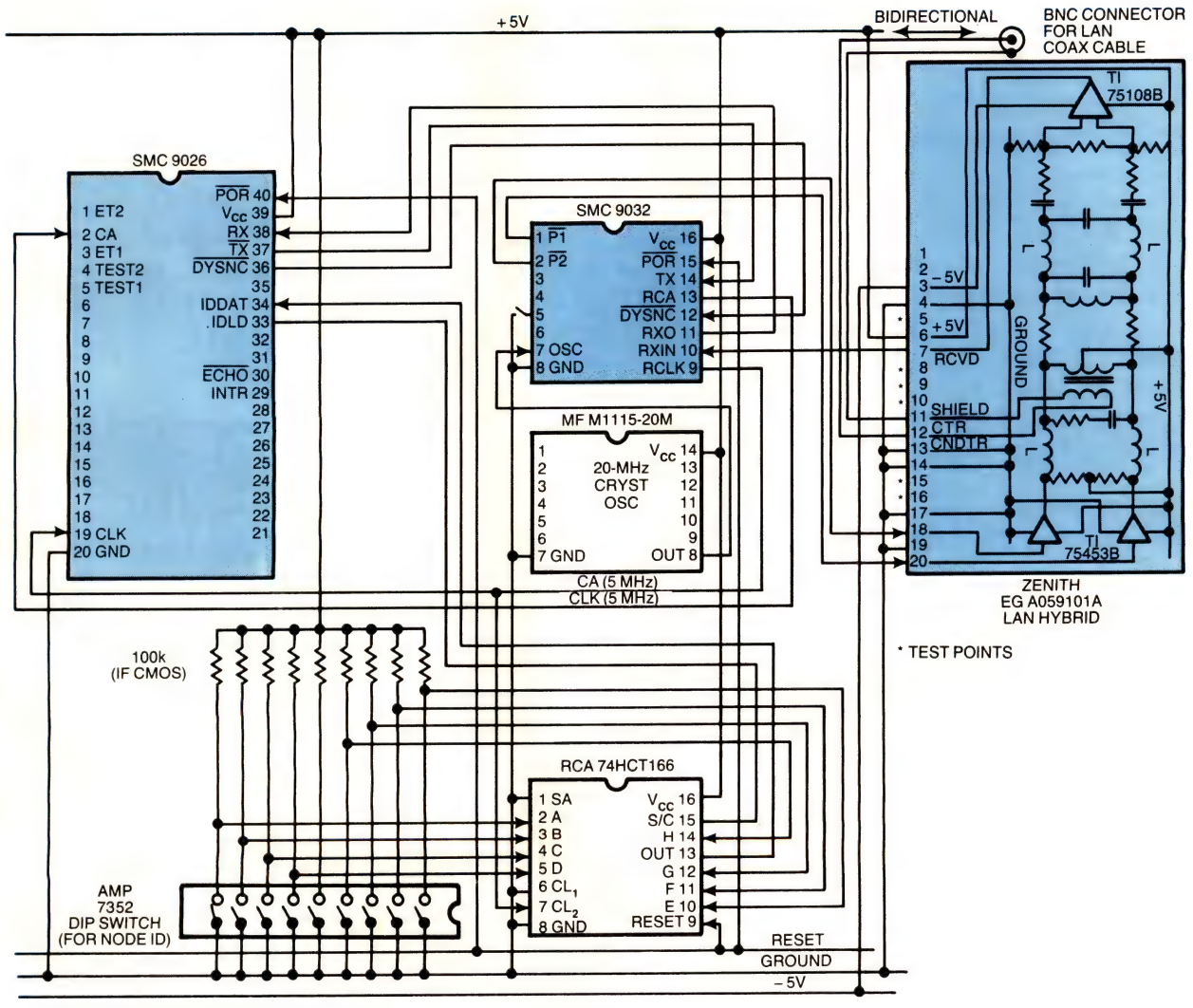


Fig 2—The interface between the 9026 LAN controller *and the LAN cable turns out to be quite simple. Most of the design problems are neatly solved by the 9026 LSI controller, the 9032 gate-array transceiver and the hybrid cable driver/receiver. These components go together with a minimum of additional glue parts.*

A hybrid LAN module eliminates design problems

instruction register, program counter, the command and decode, interrupt logic and the bus arbitration. The code is also an indication that 80% of the 9026 chip is functional, according to SMC.

The content of the second RAM location is what we had set into the ID switches. This code confirms that the 74166 shifter is being properly clocked to enter the ID serially, and that the working registers, the internal I/O bus and the buffers are all functioning.

Without actually connecting our breadboard to a working network, it was difficult to make sense out of the jumbled data pattern that the 9026 transmits. However, by carefully adjusting the scope trigger and settings, we found that we could begin to see details of the pattern. The pattern's periodicity was approximately 1 sec. John Murphy of Datapoint, one of the ARCnet's original developers, says that we were observing the 9026's activity as it tried in vain to make contact with other nodes.

During this operation, the 9026 waits 840 msec for activity on the cable, and then, not seeing any, it sends out a "reconfigure burst" consisting of eight marks repeated 765 times. Thanks to the delay feature on our 60-MHz scope (a Tektronix 2215), we could see the overall pattern and expand individual details at 5 nsec/cm to verify the timing between different signals.

The procedure is particularly useful for observing the alterations of the outgoing waveforms passing through the 9032 and the hybrid. We also found that we could follow incoming signal reception back through the hybrid and the 9032 right up to the RX pin on the 9026, because there would (of course) be reception of the transmitted dipulses. Our signals appeared to agree with the waveforms shown in the SMC manuals. (More-elaborate node self checks are outlined in Chapter 5 of **Ref 3** from Datapoint. The company uses the 9026's test pins, such as ECHO, and the TEST flag in the 9026's status register.)

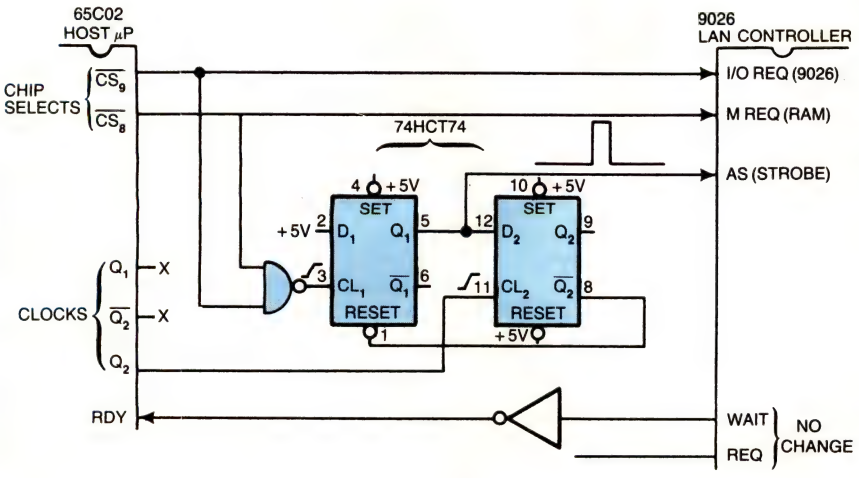
Getting the bugs out of the interface

There was one bug in our very simple interface between the host μP and the 9026 LAN controller. We found it would not work at all when we substituted the full-speed 5-MHz clock for the 3.5-MHz oscillator we had been using during early checkouts.

We returned to the 3.5-MHz oscillator and examined the waveforms. The delay feature of our Tektronix Model 2215 scope was invaluable here, because it permitted us to see 5-nsec/cm timebase details of the accesses while still providing a wider look at the long overall pattern of the software-driven test loop. (We programmed software loops to cause the host μP to address CS_8 or CS_9 continually.) The problem appeared to be that each time the 9026 tried to release the host at the end of the access cycle (by lowering WAIT), the continuous inputs from the μP clock to AS on our original design **(Ref 2)** made the 9026 think another access cycle was needed (both CS_8 and CS_9 were still Low).

Our solution was to ensure that only a single strobe for AS would occur each time the μP wanted to access the 9026 or shared RAM. We produced the desired single strobe by configuring a spare NAND gate and the two flip flops of a 7474 **(figure).**

Normally the flip flops would be in a reset condition, but whenever the CS_8 or CS_9 select lines indicated that an access should be made, the first flip flop would be set to start the AS strobe. Then the μP's 02 clock would set the second flip flop, which would in turn reset the first flip flop and end the AS strobe. With this additional circuitry, our interface, which is still fairly simple, worked at both 3.5 and 5 MHz.



A NAND gate and two flip flops *in a redesigned circuit provide a single, reliable AS strobe.*

For the acid test, we took our Rockwell AIM μC with the LAN breadboard to SMC's lab. The company has set up a network using its LAN boards in IBM Personal Computers. A 20-ft length of cable made the connection between one of the PCs and the BNC connector on our breadboard. It was a minimal 2-computer network, but it was adequate for the tests.

We performed two basic tests: receiving transmissions from the IBM PC and transmitting to it. The software we used in the AIM (**Fig 3**) is so simple that the AIM-to-PC transmit code was written on the spot during the tests, which lasted approximately 1½ hrs.

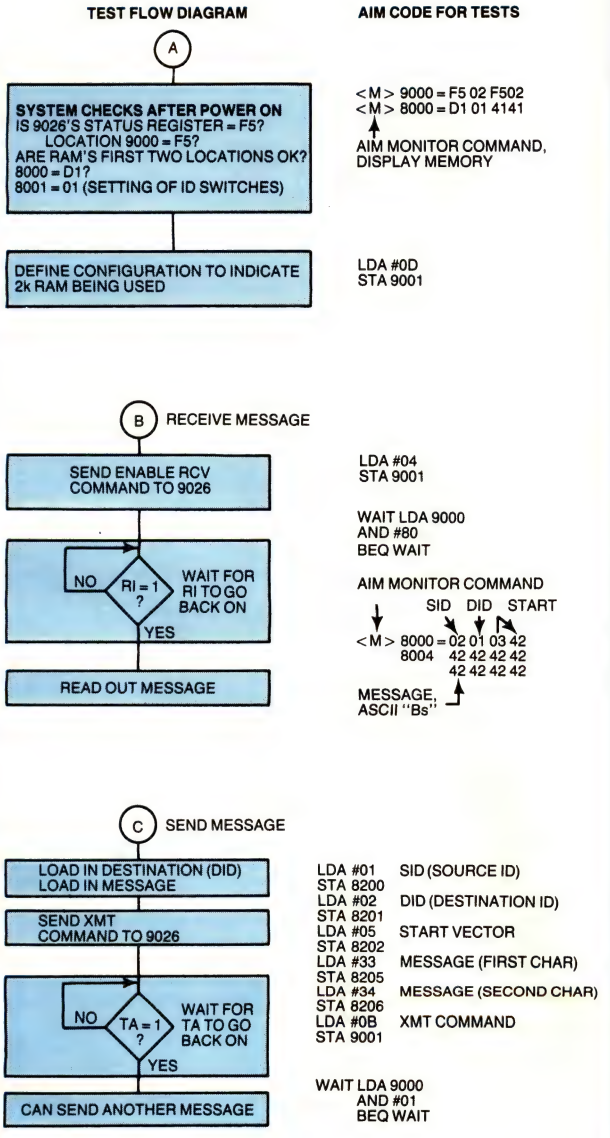


Fig 3—The software for testing our breadboard *on ARCnet turned out to be just a few routines.*

At the start of the test session we prepared our 9026 by sending it a Define Configuration command. To accomplish this task, we performed a Load Immediate of the command code (LDA #0D) followed by a store to the 9026's memory-mapped command location (STA 9001). The procedure informs the 9026 that a 2k (rather than a 1k) RAM is being used. Without this command, we could only receive and transmit to and from page zero.

For the receive test we sent an Enable Receive command (#04 to 9001), which directs the 9026 to receive any message on the cable addressed to its ID and store it in the RAM's page zero. This command resets the RI status bit in the 9026's status register (read from 9000) to Zero and provides a means for handshaking during reception. We then directed our AIM to enter a wait loop, reading the 9026's status register and monitoring when RI returned to One (indicating that a message had been received and was waiting in RAM).

When RI went to One, we had the AIM read out the correct contents of page zero of the RAM. The SID (source ID) at location 00 was 02 (the IBM's ID), and the destination ID was 01, the address we had manually entered into our breadboard's ID switches.

The third byte was 03, which means the message starts at location 03. At that location there was a string of ASCII 42s (letter B), which composed the test message from the PC.

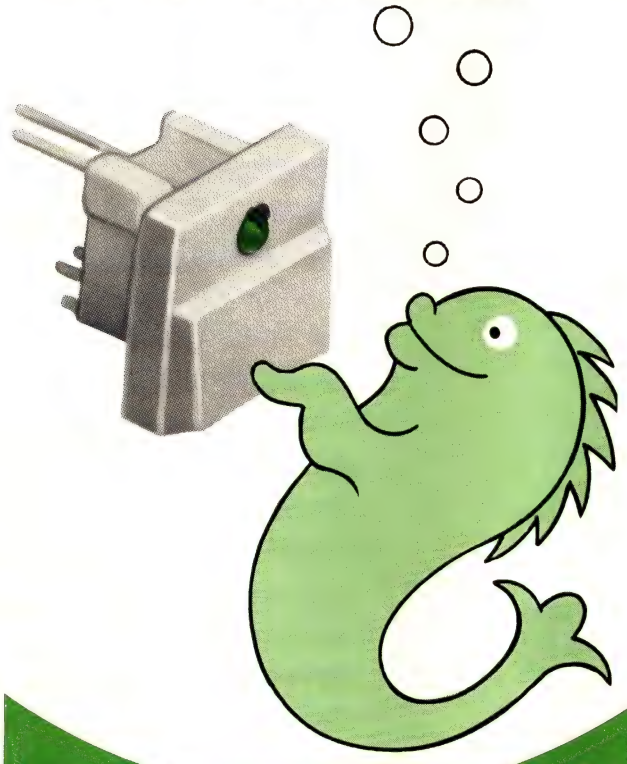
We had a bit more difficulty in transmitting from the AIM to the IBM PC, because we weren't aware that we should be starting our message at RAM location 8200 rather than 8100 (which would have been used if we had a 1k RAM). But as soon as we spotted the mistake and revised the code, our message, an ASCII 33 (number 3) followed by an ASCII 34 (number 4), appeared instantly on the PC's screen.

It's important to note that the stark simplicity of our test software might be quite misleading, in terms of actual trends taking place in LAN application software. With the large amounts of available low-level hardware and software (Open Systems Interconnection levels 1 and 2), systems-software suppliers are moving quickly to provide much higher and more complex levels to exploit the vast potential of LANs. For example, they are trying to write software that allows one user to lock out others with respect to modification of a remote file. Beyond this, there is even talk of software that would allow users to treat all the resources on a network as part of their personal computer's "virtual domain."

But even our modest tests dramatically illustrated

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how a LAN can enable totally different computers with totally different operating systems to talk to each other at high speeds. Our implementation—a single-board AIM with its 8-bit 65C02 host μP, and the relatively expensive IBM PC with its 16-bit (internal) 8088 μP—helps illustrate this point.

Future networking projects

With the successful completion of EDN's networking-design series, we anticipate more experimentation with software. For example, it makes more sense to make use of the 9026's interrupt signals rather than tie our AIM up in crude wait loops. We'd also like to incorporate some network self-checks, traffic logging, etc. In terms of hardware, breadboarding a version of the ARCnet active repeater hub to include a μP for continuous hub diagnostics also seems appropriate. This shouldn't be too difficult a task, because the hubs principally use multiple hybrid modules. With regard to applications, we believe that the way ARCnet automatically reconfigures itself when nodes are plugged in or dropped out of the network might have widespread appeal.

Although this article concludes EDN's networking-design series, we hope to update readers in the near future regarding progress we're making in software and hardware enhancements of our system. We also expect to report on unique applications we might encounter as our research continues. **EDN**

Acknowledgments

EDN wishes to thank the following people, who provided valuable assistance during this project: Brian Cayton, Gennaro DiGiuseppe and Vincent Rende of SMC (Hauppauge, NY); John Murphy and Joseph Parchesky of Datapoint Corp (San Antonio, TX); and Ron Thompson of Zenith (Glenview, IL).

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2. Cushman, R, "VLSI-based LAN-controller chip eases μP-to-network interface," *EDN,* May 3, 1984, pg 207.
3. "ARCnet Designer's Handbook," Publication 61610-01, 1983, Datapoint Corp, 9725 Datapoint Drive, San Antonio, TX 78284.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

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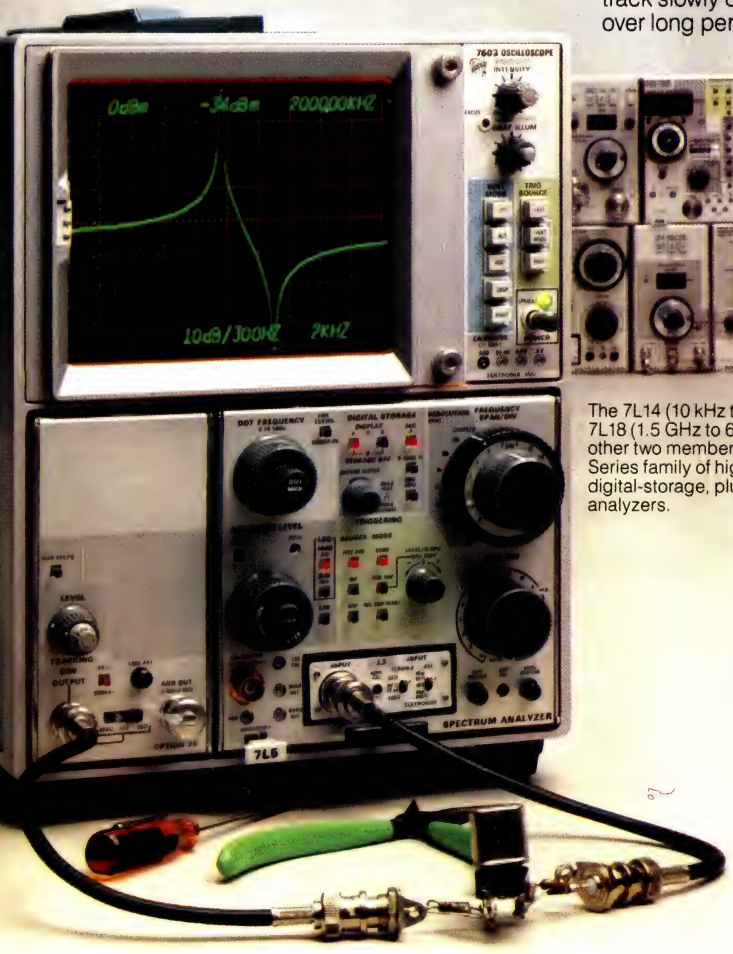
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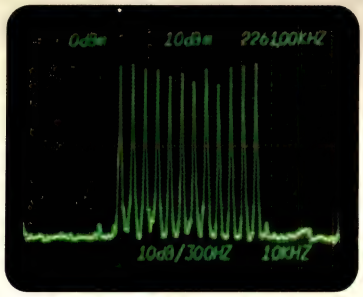
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Amplitude comparison of a 12 channel baseband system

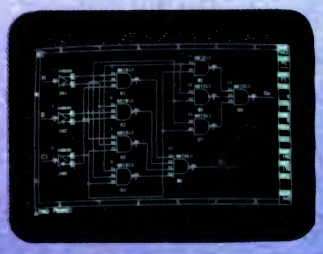
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NCC sessions to highlight software developments

The latest demands of software engineering, along with many current hardware concerns, are the focus of more than 90 meetings at the Las Vegas show.

Richard Comerford, *Senior Editor*

Next month at the 1984 National Computer Conference in Las Vegas, the technical program's balance tips toward software. Where last year's sessions were balanced evenly between hardware and software, this year all session topics (even the one on hardware and architecture) address software issues in a major way.

The show will run from Monday, July 9 through Thursday, July 12 at the Las Vegas Convention Center. The keynote address, to be delivered by John F Akers, president of IBM Corp, is scheduled for 9:30 to 11 AM. In addition to last year's nine topics is a new one, issuing from the software session, that's devoted to artificial intelligence. The 10 major topics, or tracks, comprise more than 90 sessions (see nearby **schedule**).

Also look for 18 developmental seminars, four half-day sessions and 14 full-day sessions. Again, those of most interest to designers—covering such topics as artificial intelligence, computer graphics, local networks and UNIX on microcomputers—are software oriented.

The preponderance of software topics reflects its growing importance in industry. Correspondingly, the software track outgrew the slots available over a 4-day period. Perhaps the best explanation for this growth comes from Winsor Brown of Volition Systems, who organized the software track.

Just a matter of programming?

Brown recalls that when the subject of topics for the software track first came up, software was dismissed as merely programming, ie, simply the writing of code. This casual dismissal triggered a sharp response. "Software engineering isn't just a matter of programming," Brown asserts. "It involves management, design, specification and testing. Coding is only a small portion."

The software sessions have since grown in breadth and number. There's even a session that regards software from a market-driven perspective ("Writing Microcomputer Software that Sells" on Thursday). In addition, two Monday sessions on software maintenance in the category of information-processing management are software-track spinoffs.

Software maintenance is a concept that EDP managers have been familiar with for years. It takes on new significance in the microcomputer world, however. The software-maintenance sessions will explore the subject from a microcomputer perspective. Participants will report on a new kind of engineering effort, called continuation engineering, that's already developing within some companies.

Continuation engineers try to tune products already in production to the latest market demands. Though this task might involve hardware changes, more often it means altering the software to provide extra features. Consequently, the Engineering Change Order mechanism for product control is evolving to include software.

New tools control software life

A related issue concerns the management of software engineering. EDP managers once developed their own tools for software maintenance. The proliferation of software, however, has now created a situation that demands general-purpose maintenance tools. Such tools provide the underlying theme in many of the software sessions. A good example of this theme and focus is a Tuesday session, "Software Engineering Management."

Leading off that session is Robert Loesh of the Jet Propulsion Laboratory in Pasadena, CA, who will look at the challenges presented by new system architec-

NCC '84 SCHEDULE

	MONDAY, JULY 9 AFTERNOON		TUESDAY, JULY 10			
TECHNICAL SESSIONS PROGRAM TRACKS	1:30 PM TO 2:50 PM	3:20 PM TO 4:40 PM	8:30 AM TO 9:50 AM	10:20 AM TO 11:40 AM	1:30 PM TO 2:50 PM	3:20 PM TO 4:40 PM
THE AUTOMATED OFFICE	STATE OF THE ART IN OFFICE AUTOMATION	ANALYZING MANAGERS'/ PROFESSIONALS' NEEDS FOR OFFICE AUTOMATION	MANAGEMENT WORK STATIONS AND INTEGRATED INFORMATION SYSTEMS	DESIGN AND FUNCTIONALITY IN OFFICE SYSTEMS	INTEGRATION ALTERNATIVES AND STRATEGIES	*VOICE TECHNOLOGY* IN THE OFFICE
HARDWARE AND ARCHITECTURE	DISTRIBUTED SYSTEMS	MULTI-PROCESSING SYSTEMS	32 BIT MICROPROCESSOR ARCHITECTURES	ATTACHED FLOATING POINT AND ARITHMETIC PROCESSORS	NEW MULTI-MICRO PROCESSOR ARCHITECTURES	VLSI SYSTEMS
SOFTWARE		COBOL 8X—THE NEW STANDARD	SOFTWARE ENGINEERING MANAGEMENT	MODULA-2 AND ITS APPLICATIONS	APPLICATIONS PROTOTYPING PRACTICES	EMERGING TRENDS IN INTEGRATED SOFTWARE
COMPUTER GRAPHICS AND ENTERTAINMENT	EVOLUTION OF COMPUTER GRAPHICS IN AN INFORMATION CENTER			BUSINESS GRAPHICS: THE EXPERTS PREDICT THE FUTURE		
PERSONAL COMPUTERS		PERSONAL COMPUTER INDUSTRY: THE EXPERTS FORECAST THE FUTURE	MULTIUSER AND NETWORKED PERSONAL COMPUTERS		NEXT GENERATION PC'S	FRONTIERS IN PERSONAL COMPUTING: THE USER INTERFACE
EDUCATIONAL AND SOCIETAL ISSUES	MEDIA MICRO MANIA		SMART CARDS—THE ULTIMATE CONSUMER COMPUTER	WORKING REMOTELY: WHERE WILL THE OFFICE OF THE FUTURE BE?	ENHANCING CREATIVITY IN EDUCATION	TELE-SOFTWARE DELIVERY
INFORMATION PROCESSING MANAGEMENT	SOFTWARE MAINTENANCE: NEW SYNERGY	SOFTWARE MAINTENANCE: THE FUTURE OF PRESENT SYSTEMS	BUSINESS PLANNING AND INFORMATION SYSTEMS	INFORMATION MANAGEMENT IN THE '80s: A MANAGERIAL PERSPECTIVE	SOFTWARE DEVELOPMENT PRODUCTIVITY STRATGIES	DISTRIBUTING INFORMATION—A MANAGEMENT PERSPECTIVE
DATA BASE MANAGEMENT	CURRENT STATUS OF THE RELATIONAL DATA BASE MODEL	SQL DATA BASE LANGUAGE				
ARTIFICIAL INTELLIGENCE	KNOWLEDGE BASED TRAINING SYSTEMS	AI TECHNIQUES FOR SIGNAL INTERPRETATION				
COMPUTER COMMUNICATIONS			MULTI-VENDOR NETWORKS— PART I	MULTI-VENDOR NETWORKS—PART II	VIDEOTEX	UPDATE ON LOCAL AREA NETWORKS
PROFESSIONAL DEVELOPMENT SEMINARS	1:00 PM TO 4:30 PM		9:00 AM TO 4:30 PM			
	MOTIVATING AND MANAGING COMPUTER PERSONNEL LETTING GO OF STRESS PEOPLE AND TECHNOLOGY: ISSUES AND RESPONSES		BREAKTHROUGHS IN STRATEGIC PLANNING AND EDP MANAGEMENT THE COMPUTER PROFESSIONAL AS EXPERT WITNESS EVALUATING AND USING DATA BASE MANAGEMENT SYSTEMS FOR MICROCOMPUTERS ARTIFICIAL INTELLIGENCE HOW TO SAVE TIME & MONEY BUYING A DESKTOP COMPUTER			

tures such as networking, distributed processing, multiple processors and fault tolerance. He's found, for example, that concurrent design principles don't exist in the multiprocessing environment. It thus becomes a management responsibility to develop them.

Because of the difficulty these architectural attributes can create, Loesh advises managers and designers that it's better to proceed with 1- and 2-processor architectures until you find a solid reason not to. If you find such a reason, you should develop the system's architecture piece by piece. Newer architectures require more time for development, he observes. The wise designer or manager will have to do more prototyping as a result, but there will be a fallback design in case of problems.

During the same session, Wolfgang Strigel of MacDonald Dettwiller & Associates Ltd will discuss his company's use of software-development tools, and he will present quantitative measurements of their effectiveness. As examples, he'll use both large (128,000 lines of code) and small (30,000 lines) projects as well as real-time applications. The most positive tools he found were walkthroughs, in which a software engineer's peer group reviews the full code asking hypothetical questions, and inspections, in which the group tries to determine what's missing in a program based on the members' general programming knowledge.

Strigel concludes that these tools produce results that conform to software-engineering principles. He found that you can apply even simple software-engineering techniques with positive benefits. He supports that statement by noting the high productivity achieved in the projects: 40 noncomment source lines were generated per person per day, vs the industry

WEDNESDAY JULY 11				THURSDAY JULY 12		
8:30 AM TO 9:50 AM	10:20 AM TO 11:40 AM	1:330 PM TO 2:50 PM	3:20 PM TO 4:40 PM	8:30 AM TO 9:50 AM	10: AM TO 11:40 PM	1:30 PM TO 2:50 PM
STRATEGIC SYSTEMS PLANNING: ART SCIENCE, OR NONSENSE?	SHARED NETWORK RESOURCES	MICRO-MAINFRAME CONNECTION	ELECTRONIC MAIL—CURRENT DEVELOPMENTS	OFFICE AUTOMATION EQUIPMENT SELECTION: Q & A SESSION	LARGE OFFICE AUTOMATION SYSTEMS	
TRENDS IN SUPERCOMPUTER SYSTEMS: DESIGN AND USE	THE FIFTH GENERATION REVISITED	—PIONEER DAY SESSION—LAWRENCE LIVERMORE LABORATORY—THE EARLY YEARS	–PIONEER DAY SESSION–THE OCTOPUS SYSTEM			SYSTEMS RELIABILITY
SOFTWARE ENGINEERING WORK STATIONS	UNIX STATE OF THE ART	SOFTWARE AUTOMATION —AN INTERNATIONAL PERSPECTIVE	A BATTLE ROYAL: STRUCTURED TOOLS & METHODS	WRITING MICROCOMPUTER SOFTWARE THAT SELLS	LARGE VS. SMALL PROGRAMMING LANGUAGES: PROS & CONS	MILITARY VS COMMERCIAL DOCUMENTATION
		NEW TECHNIQUES IN 3D AND ANIMATION	CASE STUDIES IN COMPUTER ANIMATION	EMERGING STANDARDS IN COMPUTER GRAPHICS	MICRO-GRAPHICS	
		DATA MANAGEMENT IN INTEGRATED OPERATOR ENVIRONMENTS	PORTABLE COMPUTERS AND THEIR SOFTWARE	TOWARDS A UNIVERSAL SOFTWARE STANDARD		
TELE/CONFERENCING: THE FUTURE OF BUSINESS MEETINGS		LEGAL ROADBLOCKS TO EXPLOITATION OF TECHNOLOGY	PROGRAMMER MALPRACTICE			AN OPERATIONAL APPROACH TO PENETRATING VERTICAL MARKETS
MULTI-USER MICROS VS. NETWORKED PCs	STRUCTURED METHODOLOGIES AND AUTOMATING THE SYSTEMS DEVELOPMENT PROCESS	NEW INFORMATION MANAGEMENT METHODOLOGIES	DECISION SUPPORT SYSTEMS AND DISTRIBUTED PROCESSING	INFORMATION SYSTEMS AND PRODUCTIVITY	PLANNING FOR AND SUPPORTING END USER BUSINESS COMPUTING	SOFTWARE TEST AND VALIDATION
	DATA BASE WORKSTATIONS	ENTITY RELATIONSHIP APPROACH TO DATA BASE DESIGN			FOURTH GENERATION LANGUAGES AND PERSONAL COMPUTERS	DATA BASE APPLICATIONS AND INTERFACES
EXPERT SYSTEMS IN THE COMPUTING INDUSTRY	TOOLS FOR COMMERCIAL AI SYSTEMS		SOFTWARE ENGINEERING TECHNIQUES	NATURAL LANGUAGE INTERFACES TO SOFTWARE SYSTEMS	INTELLIGENT AIDS TO DOCUMENT PREPARATION	THE FIFTH GENERATION: WHAT, WHY, AND SO WHAT?
COMPUTER INTEGRATED AUTOMATION	COMPUTER SYSTEMS AND DEVICES			AT&T DIVESTURE: THE AFTERMATH	THE WORLD OF INTEGRATED NETWORKS	
9:00 AM TO 4:30 PM				9:00 AM TO 4:30 PM		
SOFTWARE ENGINEERING WITH ADA INTRODUCTION TO COMPUTER GRAPHICS TRAINING TO SUPPORT ELECTRONIC TECHNOLOGIES: MANAGING THE CHANGE DATA ANALYSIS TECHNIQUES PROJECT PLANNING AND CONTROL WORKSHOP				SUPERCOMPUTERS: WHY ARE THEY NEEDED AND WHERE ARE THEY USEFUL LOCAL NETWORKS PUTTING UNIX TO WORK ON A MICRO STRUCTURED DESIGN AN INFORMATION SYSTEM PHILOSOPHY FOR THE 1980's		

average of 10 to 20 lines. He also notes that after integration, there was a rapid decrease of effort, suggesting that use of the tools helped eliminate bugs.

Strigel also found, however, that very few tools helped with problem solving. That lack and the nature of the desired tools are further explored in the session titled "Software Engineering Work Stations."

The soft half of workstations

A software-engineering workstation is the logical counterpart of the CAD hardware workstation. It differs from development stations, which usually enter the design cycle at the end of the software effort when code is being written, integrated and tested with the hardware. A software-engineering workstation, on the other hand, should help throughout the software life cycle, in design, analysis and maintenance.

Development systems, with their in-circuit emulators, are typically used in embedded system design. You might use a software-engineering workstation to develop application programs that would run on a full system when the in-circuit emulator would be extraneous. In the session, participants will attempt to formulate a more complete description of a software-engineering workstation while providing practical examples of what's already been done.

One example comes from Phil Grouse from the University of New South Wales, who will describe the workstation he designed, called Flowdata, which is based on the IBM Personal Computer. The system links the flow diagram, code and commentary together, so that if you make a change in one area, the other areas affected are apparent. Connecting these areas in such a manner helps control design. The workstation

is oriented toward tree-structured, modular software.

With this emphasis on software, you might expect more discussion than demonstration. Cooperation among a number of companies, however, has managed to produce a practical demonstration of software with hardware at multiple levels. When the exhibit hall opens on Monday, you'll be able to go to two booths and see network protocols in action. One booth is sponsored by the National Bureau of Standards and Boeing Computer Services, the other by General Motors.

The NBS/Boeing booth will contain equipment from nine manufacturers: Advanced Computer Communications (Santa Barbara, CA), Charles River Data Systems (Framingham, MA), Digital Equipment Corp (Maynard, MA), Hewlett-Packard Co's Colorado Networks Operation (Fort Collins, CO), Honeywell (Phoenix, AZ), Intel (Santa Clara, CA), International Computers Ltd (London, England) and NCR Corp (Dayton, OH). Software will link the hardware to create a multivendor CSMA/CD (carrier sense multiple access with collision detection) local-area network that conforms to the IEEE 802.2 protocol.

In the other booth, Allen-Bradley Systems Division (Highland Heights, OH), Concord Data Systems (Waltham, MA), Gould Inc's Programmable Controller Division (Andover, MA), IBM's Industrial Systems Division (Boca Raton, FL) and Motorola Inc (Phoenix, AZ) will provide equipment to implement a multivendor, broadband token-passing network that conforms to IEEE 802.4 and General Motor's Manufacturing Automation Protocol (MAP). The latter is a GM specification that selects existing or emerging standards for multivendor communications in manufacturing.

Both exhibits will demonstrate the ability of networks that link equipment from various vendors to function successfully as high as the transport layer, which is layer 4 of the 7-layer Open Systems Interconnection (OSI) Reference Model. The transport layer provides control of the information flow between sender and receiver.

At the show, you'll be able to verify that this layer really works by creating your own file at one manufacturer's station and accessing it at another's. Once you've seen the networks in action on Monday, you'll be able to get more specific information at the 2-part "Multivendor Networks" session on Tuesday. Part 1 will be chaired by Robert Blanc of NBS, Part II by Mike Kaminski of GM.

Hardware enthusiasts, don't despair

Although the sessions are heavily oriented toward software, there's plenty of hardware information to be gleaned from the track on hardware and architecture organized by Associate Professor Faye Briggs of Rice University. All nine sessions (six have contributed papers and three are panel discussions) should have something for hardware designers.

Even in this track, however, experts will contend with software issues. The first session, "Distributed Systems," will investigate operating systems and database design for distributed processing systems. Session chairman Ben Wah of Purdue University will discuss a new bus-arbitration scheme for which the university has filed a patent.

The scheme, developed for a local network of VLSI-based systems, is a protocol that recognizes two states: no access or access by one or more nodes. Its algorithm has the advantage of resolving access contention in an average time that's independent of the workload. The scheme compares favorably with such networks as Ethernet, in which contentions rise as the workload increases. An Ethernet-like system can suffer from lengthy contention-resolution times.

The session also covers the practical experience gained at Bell Laboratories in implementing DMERT, an operating system for the ESS #5 telecommunications switching system. S F Ho of the Naperville, IL facility will explain how the design group overcame the problem of designing the operating system so that, with the given hardware, they could detect a fault and reconfigure the system to overcome it.

The second session in the track, "Multiprocessing Systems," will provide some detailed hardware-architecture solutions. Armond Inselberg of Synapse Computer Corp (Milpitas, CA) will explain how that firm was able to use off-the-shelf parts to build a system based on multiple 68000 processors with their own cache memories. He'll provide details on how the cache convergence problems were overcome while ensuring that the cache remains transparent to the user.

One of the more useful session for hardware designers will be "32-bit Microprocessor Architectures." At this session, representatives of National Semiconductor, Zilog, Motorola, Bell Laboratories and Hewlett-Packard will present their 32-bit architectures side by side so that you can compare them.

In general, this year's NCC technical sessions should provide an interesting software counterpoint to the more than 650 predominantly hardware-oriented exhibits. Dividing your time between the technical sessions and workshops and the exhibit floor should provide a solid update on the state of the art in the computer industry. If you haven't already registered, call 800-NCC-1984. **EDN**

Article Interest Quotient (Circle One)
High 476 Medium 477 Low 478

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CIRCLE NO 73

PAC-139

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Digi-Data's Model 70 PC cartridge tape system lets you back-up your PC's Winchester drive without getting buried in floppies. One cartridge holds 16.5 Mbytes of data, more than you can put on 51 floppy disks! And you can back-up your 10 Mbyte PC XT® drive in less than 15 minutes of *unattended* operation. That is a small fraction of the time it would take with the PC's floppy, with you standing there changing disks.

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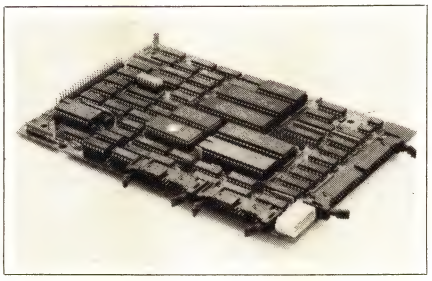
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Disk-controller and host-adapter boards suit use with multiuser μC systems

Model ACB-5580 controller incorporates an SMD interface as well as a full SASI/ANSI SCSI bus implementation that includes arbitration and disconnect/reconnect functions. To allow a host to run concurrent I/O tasks, this latter function connects a disk drive and I/O bus only when that drive is ready to receive or write data.

Suited to use with multiuser microcomputer systems such as those running Bell Labs's UNIX operating system, the board can support as many as seven host computers through the SCSI bus and as many



as four 8- or 14-in., 9.6M-bps SMD disk drives. The board manages multiple accesses to files, relieving the operating system of the task of managing shared disk resources. To increase data throughput, the controller implements noninterleaved operation, which allows information on one disk track to be accessed in one rotation.

Model ACB-5580 costs $980. Host adapters, which function as I/O processors between the SCSI and host buses and furnish 1.5M-byte/sec DMA, include the Multibus-compatible Model AHA-1530 ($460) and S-100-compatible Model AHA-1510 ($425). Production quantities will be available 3rd qtr.

Adaptec Inc, 580 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 946-8600.

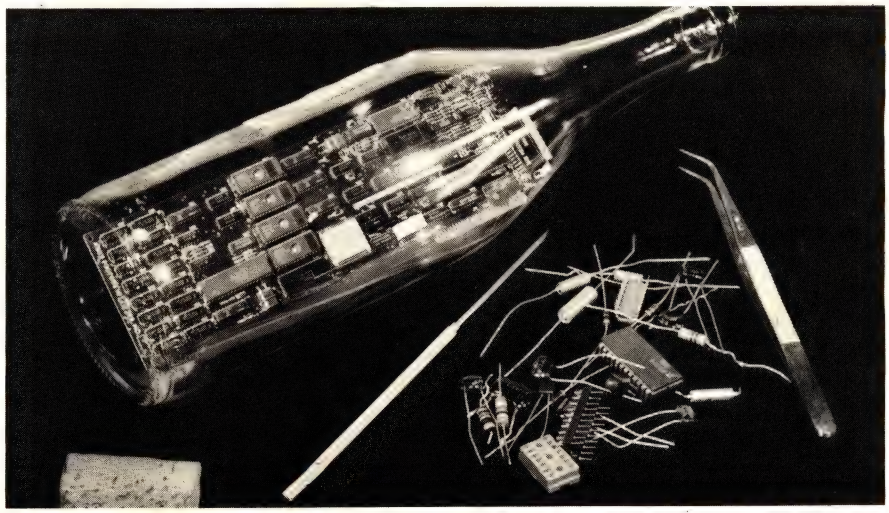
Circle No 685

IBM PC-compatible speech-input board recognizes 240 utterances

Compatible with IBM's PC and XT computers, this speaker-dependent speech-recognition board can recognize 240 isolated words or short phrases with 99% accuracy. Each utterance can be as long as 1.25 sec; minimum word length is 80 msec.

The plug-in board contains all the A/D-converter, signal-processing and I/O circuitry necessary to convert the spoken word to digital code; it incorporates an Intel 80186 16-bit μP, 128k bytes of dynamic RAM, and 32k bytes of EPROM (expandable to 64k bytes). It also includes its manufacturer's proprietary ASA-16 spectrum-analysis chip, which derives spectral patterns from input sound waves. Input bandwidth is 200 to 7000 Hz.

Supplied with the board, a menu-based utility program prompts operators with questions and instructions via the computer's display. In the board's keyboard mode, digi-



tized voice data appears to the computer as if it were entered via the keyboard; that mode permits the board to be used with any PC-compatible software. The PC mode accommodates users who write their own applications software and wish to incorporate speech input into it.

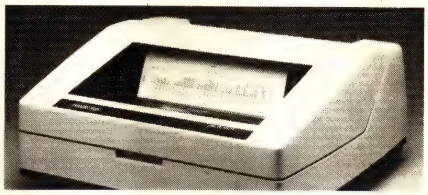
The board comes with a connecting cable, users' manual and a choice of head-mounting or desk microphone. Power requirements include 5V at 1A, +12V at 80 mA and −12V at 150 mA. Less than $2000.

Interstate Voice Products, 1849 W Sequoia Ave, Orange, CA 92668. Phone (714) 937-9010.

Circle No 680

Compact 80-lpm dot-matrix printer interfaces with desktop computers

Model MVP 150B dot-matrix line printer furnishes correspondence-quality output at 80 lpm; a compressed-print mode allows operation to 200 lpm. Such performance suits it for use as a shared resource for workstation clusters. Moreover, its Centronics-compatible interface permits it to work with a variety of desktop computers, suiting it for use as a system printer for μC-based local-area networks.



Under software control of a host computer, the MVP 150B can print a 132-column report on 8½×11-in. paper, eliminating the need for xerographic reduction. For graphics applications, it features 100×100-dot/in. resolution. Plotting speed ranges from 8.3 in./min in a high-resolution mode to 25 in./min in a high-speed mode. The unit's block-graphics character set allows users to generate custom business forms. It can provide shadowing and boldface printing.

Font-matrix dimensions range from 13×12 for lower-case characters in the word-processing mode to 7×5 for upper-case characters in the compressed-print mode. The printer's adjustable tractors feature 5-pin engagement and handle form widths from 3 to 16 in.

The 60-lb printer measures 10.5×24.6×20.7 in. Power requirements are 200W max at 120V (+10, −30%), 47 to 62 Hz. $3745.

Printronix, Box 19559, Irvine, CA 92713. Phone (714) 863-1900. TWX 910-595-2535.

Circle No 681

200-ips streaming-tape drives store 500M bytes per cartridge

Two streaming-tape drives in the MT-2000 family operate at 200 ips and can store 500M bytes of data on a book-size cartridge employing 1500 ft of ½-in.-wide magnetic recording tape. The drives can also work with 300M-byte cartridges using 1000 ft of tape.

The "full-wide" Model MT-2210 fits in a standard 19-in. rack; it's 8.75 in. high and 17.5 in. deep. The "half-wide" Model MT-2220 has an 8.5×10.2-in. panel footprint (making it form-factor compatible with Control Data Corp's Model 9175 FSD drive) and is 24 in. deep.



Both units operate at 200 or 50 ips in the streaming mode and at 50 ips in the start/stop mode. Data-transfer rate at 200 ips is 240k bytes/sec—allowing each drive to back up or restore 500M bytes in 36 min. The units use a 24-track, bit-serial serpentine format that yields a 9600-bpi recording density. Each model includes a 2-track read/write head assembly that's stepped 12 times to achieve the 24 tracks. This head-stepping procedure permits an average 30-sec access time to any record stored in the cartridge.

Data encoding and decoding takes place in the drive's integral formatter and is transparent to the controller. The formatter accepts byte-wide data from the controller and encodes it into bit-serial data during a write operation. During a read operation, the formatter sends the controller 9-bit-wide data—eight data bits plus a parity bit.

The MT-2210 and MT-2220 cost $5500 and $5750, respectively; a 500M-byte tape cartridge costs $140. Delivery begins 3rd qtr.

MegaTape Corp, Box 317, Duarte, CA 91010. Phone (213) 357-9921.

Circle No 682



MISSION ACCOMPLISHED.

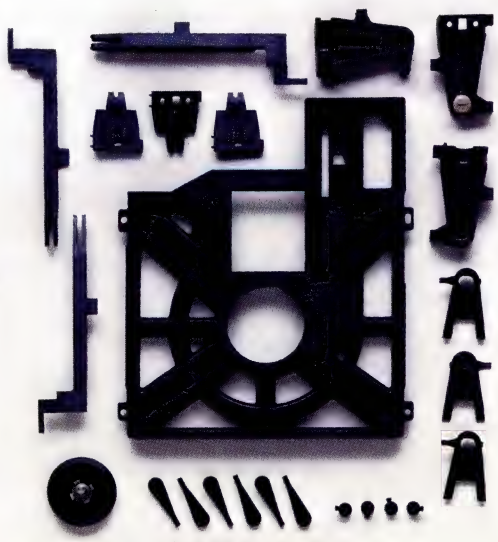
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CIRCLE NO 75

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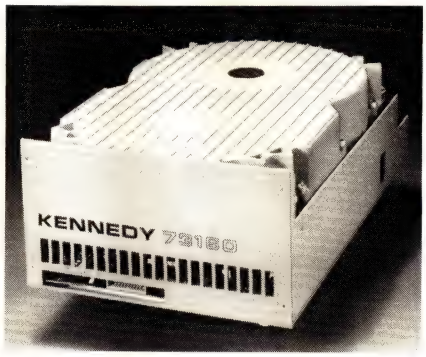
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165.9M-byte Winchester disk drive achieves 20-msec average access time

An 8-in. Winchester disk drive, Model 73160 employs composite heads and a rotary actuator to achieve a 40-msec max, 20-msec average access time; 1-track access time specs at 5 msec. Unformatted capacity equals 165.9M bytes. Average latency time is 8.33 msec at a 3600-rpm disk speed. The drive comes with an SMD, ANSI or PICO interface.



To achieve these access times, the drive's actuator system employs four samarium/cobalt magnets and a flat electromagnetic coil to minimize mass. The actuator arm is balanced to compensate for gravitational forces, allowing the drive to operate in any orientation without adjustment. The composite heads, which fly 14 to 17 μin. above the disk surface with a 9.5g loading, minimize fringing, permitting high track densities.

Each unit includes six platters that provide 10 data surfaces and a servo surface used to compensate for thermal expansion effects. The disks can store 9980 bpi on their inner tracks and feature 823 tracks per surface. A modified frequency-modulation technique achieves a 9.67-MHz data-transfer rate.

The drive operates from 40 to 122°F. Incorporating a brushless, direct-drive dc motor, the unit requires 5V at 1.5A and 24V at 4A peak running current, 5A starting current. The 25-lb drive measures 4.62 in. high, 8.55 in. wide, and 14.25 in. deep. $4695. Delivery, 90 days ARO.

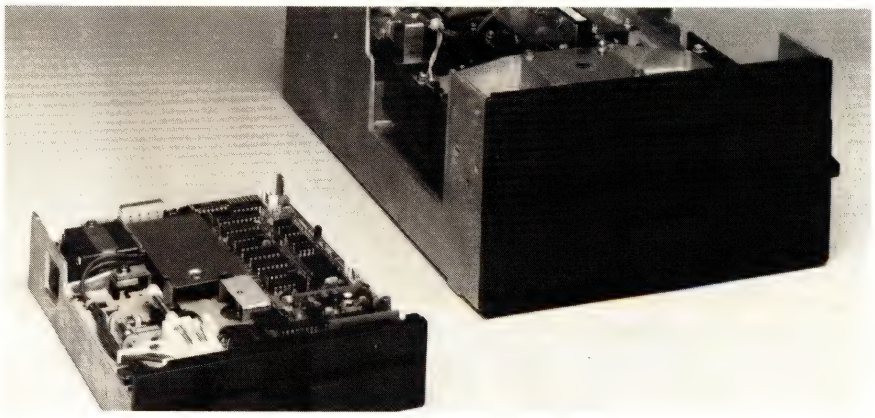
Kennedy Co, 1600 Shamrock Ave, Monrovia, CA 91016. Phone (818) 357-8831. TLX 4720116.

Circle No 683

Half-height 5¼-in. floppy-disk drive offers 1.6M-byte storage capacity

Model 475 double-sided 5¼-in. Minifloppy drive features a 1.6M-byte storage capacity, 500k-bps data-transfer rate and a 3-msec track-to-track access time. Furnishing 96-tpi performance, the drive can also read data written on 48-tpi 5¼-in. diskettes.

The drive can use a standardized 8-in.-disk recording format, giving users access to software written for 8-in. floppy disks. Formatted capacity is 1.2M bytes.



To achieve its storage capacity, the 1.63×5.75×8-in. Model 475 employs high-coercivity, 600-oersted media, which is easier to magnetize than the 300-oersted media used with most 5¼-in. floppy disks. To yield the 500k-bps transfer rate, the drive incorporates a brushless, direct-drive dc motor that revolves at 360 rpm, rather than the 300-rpm spec common to other drives.

The drive's pc board includes LSI circuitry and a 4-bit μP to handle read-channel, write-channel and motor-control operations. A stepper-motor/band-actuator system positions the read/write head. A vertical clamping mechanism centers the diskette on the drive hub to help minimize positioning errors.

Power consumption specs at 12.5W during operation and 3.6W during standby. MTBF specs at 10,000 power-on hrs. $200 (OEM qty). Volume deliveries are scheduled for 3rd qtr.

Shugart Corp, 475 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 737-4355.

Circle No 684

Continued on pg 180

As many as 320 Winchester drives can be tested every eight-hour shift using Wilson's new MDTS-1000 Multiple Drive Test Station.

With a continuous flow of 32 drives attached, the system can automatically certify up to eight drives* every 12 minutes. That's faster throughput than from any other digital test system on the market!

For All Volume Users

Designed for production floor testing, large-scale incoming inspection and burn-in applications, the MDTS-1000 accommodates all 5¼" drives with ST506 interface, up to 16 heads and 2048 cylinders. Future advanced interfaces such as ESDI, ST412HP, etc., can be added easily on site.

Composed of eight standard Wilson DTS-1000 Drive Test Stations linked through an RS-232 MUX to an MS-DOS based microcomputer, the MDTS-1000 uses the computer for centralized logging, test control, CRT display and data printout via a high-speed printer.

The standard Wilson test includes verification of basic drive functions, followed by media verification, read margin and drive voltage margin testing. Modified or custom tests can be added if desired.

The computer allows factory-action status reports, plus long-term trend, error and throughput analyses based on accumulated test data.

More Winchester Analyzers

Wilson offers a greater selection of Winchester drive analyzers than any other test equipment company.

MWX-1000 Winchester Drive Analyzer. The "heart" of all Wilson Winchester test systems, the MWX-1000 automatically tests a single drive at a time.

DTS-1000 Drive Test Station With four drives attached, the DTS-1000 fully tests up to five drives an hour.

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Now the fastest non-stop system for Winchester testing comes from

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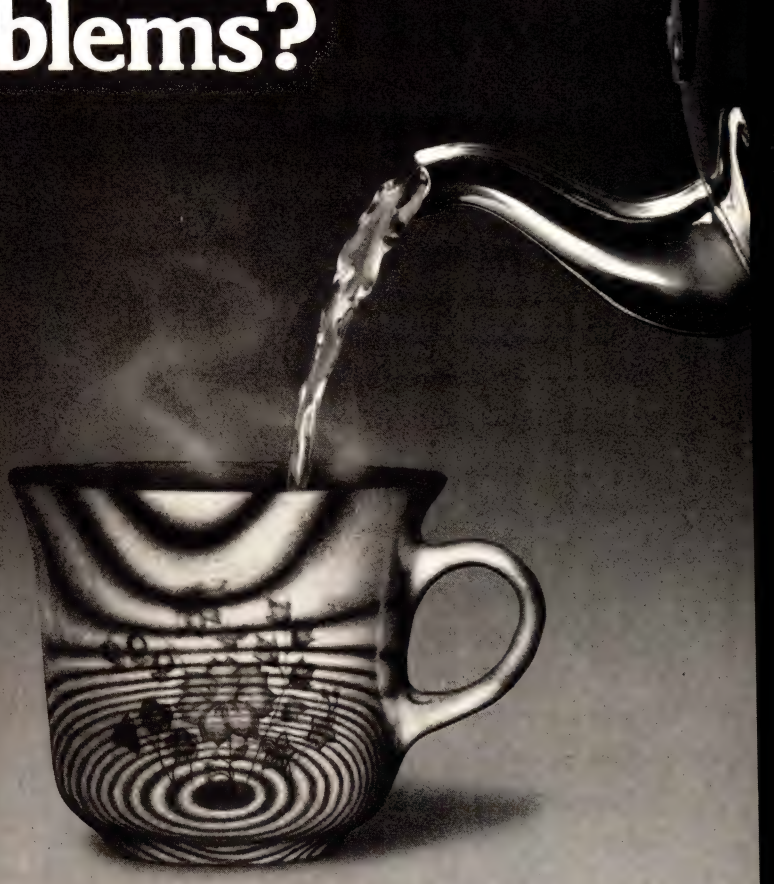
2237 N. BATAVIA STREET · ORANGE, CALIFORNIA 92665
TELEPHONE (714) 998-1980 · TELEX 181 598

*Using Standard Wilson Test on 10 mb Winchester drives.

CIRCLE NO 76

Thermal Problems?

New Camera shows deformations never seen before.



A unique solution

Powerful holographic interferometry is now a one-button operation with Newport's self-contained HC-1000 Holographic Camera. In seconds, anyone can produce an image of minute deformations and view them *as they evolve.*

Straightforward Interpretation

Each fringe in the holographic contour map represents a precise 12.4 microinch change in elevation. Using this simple guide, it is clear that the coffee cup is bulging. And anyone can use the HC-1000 after only about an hour of orientation. All-electronic, it requires no chemical processing.



The figures tugging and pulling on this 5¼ inch disk drive have been sketched in to help visualize the nature of the thermal deformations revealed by the holographic fringe pattern.

A Powerful Design/NDT/QC Tool.

Disk drive manufacturers use the HC-1000 to visualize thermal deformation of critical structural components and housings. Warping from the thermal transients can cause alignment and tracking errors–the HC-1000 pinpoints their causes.

Other engineers depend on the HC-1000 to study the turn-on/warm-up response of circuit boards, laser housings, and gyroscopes, and to observe the dimensional temperature sensitivity of small radio dish antennas at −120°C.

Free Offer.

Explore how holography can be applied to your work in a FREE introductory session in our consulting laboratory or take advantage of our low cost leasing program. We also have a free 208 page Laser/Optics catalog for anyone interested in general laser applications.

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CIRCLE NO 158

Discover HP's revolutionary answer to your measurement needs

Introducing an extremely versatile solution to your measurement needs: The HP 7090A Measurement Plotting System. By merging several technologies –waveform recording, digital plotting, analog recording, and automated measurement–the HP 7090A provides a powerful solution to a broad range of measurement problems. Imagine... significantly increasing your ability to measure and display low frequency phenomena and, at the same time, *substantially improving your real-time recording and digital plotting results. All in one* low-cost *system!*



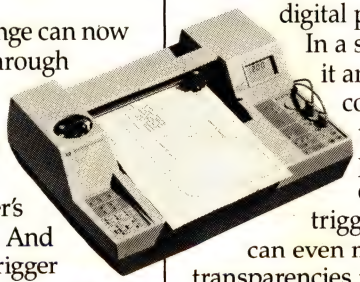
Hewlett-Packard's new 7090A– the single-instrument solution for low frequency measurement, analysis and documentation

Now you can capture low frequency (<3kHz) signals.

The HP 7090A precisely measures, stores and displays signals through simultaneous sampling on each of three channels, with 12-bit resolution, a bandwidth of dc to 3kHz (33.3k samples/s maximum) and a 1000 word memory per channel.

You get 6 trigger mode flexibility.

Virtually any signal change can now initiate signal capture through HP's six trigger modes. Even decaying repetitive signals, such as faults in a power line voltage or in a transducer's carrier, can be captured. And combined with our pretrigger capability, the HP 7090A Measurement Plotting System is your ideal system for turn-on/turn-off characterization, fault monitoring and mechanical motion analysis.



Plus, it's a system component.

All panel functions of the HP 7090A are programmable via the HP-IB interface. And data can be streamed at up to 500 points/s from either the internal 1K buffers, or in real time from the analog-to-digital converters. A menu driven software package is available for HP Series 200 computers, allowing you easy data manipulation, storage/retrieval, and system integration.

And the HP 7090A gives you much more...

The HP 7090A is also a high performance real-time X-Y recorder, digital plotter and DVM. In a stand-alone mode, it annotates setup conditions, date and time, selected data points from memory and even the trigger time. Plus, you can even make overhead transparencies for technical presentations!

The HP 7090A is your low-cost, one-stop system.

From its 3 analog inputs to its 6-pen writing system, the HP 7090A adds a totally new dimension to low-frequency measurement, analysis and display. And with a price tag of only $4400,* the HP 7090A is your complete measurement plotting system.

Send today for your free information package.

Clip out and mail the coupon below to receive–absolutely free– a complete information package, including our detailed brochure and specifications.

*Domestic U.S. price only

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Hewlett-Packard
16399 W. Bernardo Drive,
San Diego, CA 92127

Attn: Marketing Communications 11403 EM6

TAPE DRIVE



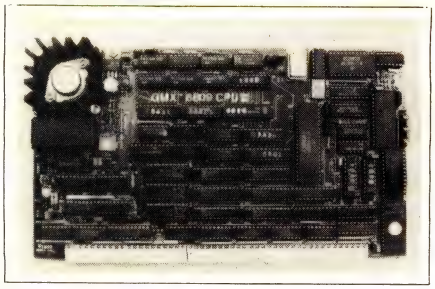
The GCR CacheTape family of group-code-recording (GCR) tape drives achieves 6250-bpi recording densities and employs their manufacturer's ½-in.-tape interface to facilitate compatibility with system software. Total storage capacity extends to 180M bytes.

Model M990 features a 128k-byte cache size and a 72k- to 395k-byte/sec average transfer rate. Model M991 sports a 256k-byte cache size and a 72k- to 790k-byte/sec average transfer rate. Maximum block size specs at 32k bytes for the M990 and 64k bytes for the M991. Both models incorporate 4-track error-correction schemes. Measuring 14 in. high, they suit use in office environments. Battery backup is optional. $6000 to $8000 (OEM qty).

Cipher Data Products Inc, Box 85170, San Diego, CA 92138. Phone (619) 578-9100.

Circle No 690

C SYSTEM



At the heart of its manufacturer's 15-user C development system, the Model GMX 6809 CPU III board (shown here) performs 1-byte/μsec DMA transfers from memory to memory or memory to I/O devices. The use of memory attributes and illegal-instruction trapping protect the system from program crashes. If one user's program crashes, only that user is affected; other users remain unaware of the problem. The board automatically arbitrates contention problems between on-board memory and external devices.

The system also comes with intelligent serial I/O boards that allow user terminals to run at 19.2k-baud rates. Other features include 1M byte of static CMOS RAM; a 72M-byte hard-disk drive; a 6M-byte, removable-pack hard-disk drive and a 96-tpi double-sided, double-density floppy-disk drive.

The compiler runs under OS-9, a multiuser, multitasking operating system similar to Bell Labs's UNIX. The system costs $18,868.09.

Gimix Inc, 1337 W 37th Pl, Chicago, IL 60609. Phone (312) 927-5510. TWX 910-221-4055.

Circle No 687

DOT-MATRIX PRINTER



A 24-pin printhead composed of 8-mil-diameter print wires allows Model P1340 to provide 80-column letter-quality output at 54 cps. A draft-quality mode operates at 144 cps (12 cpi) or 120 cps (10 cpi).

To maximize throughput, the P1340 prints in a single pass, even when producing bold-face type or underlining. It offers software-selectable fonts, pitches and line spacing as well as a 132-column, 78-cps condensed-print mode (16.7 cpi) and proportional spacing for use with word-processing packages supporting that function. The unit also includes a 180×180-dot/in., dot-addressable graphics mode.

The printer accommodates sheet stock or continuous forms from 5.4 to 10 in. wide. Line-spacing speed is 37 lps for a 6-lpi pitch. Friction and pin feed come standard, as does a Centronics-compatible parallel or RS-232C serial interface. The 22-lb. unit measures 11.6×5.9×16.5 in. $995. Delivery, 60 to 90 days ARO.

Toshiba America Inc, Information Systems Div, 2441 Michelle Dr, Tustin, CA 92680. Phone (714) 730-5000.

Circle No 686

E-MAIL TERMINAL



The Z80-μP-based Model MSR 744-8B terminal includes a 62-key keyboard that generates 128 ASCII characters. The battery-backed-up memory can store 8k characters. The printer includes a 256-character buffer and furnishes 30-cps performance. Fourteen character densities range from 5 to 20 cpi; a graphics mode provides 120-dot/in. horizontal, 60-dot/in. vertical resolution.

The Bell 103-compatible internal modem operates at 0 to 300 baud and allows the terminal to communicate with such networks as TWX, Telex, GTE Telenet, ITT Dialcom, MCI Mail, Tymshare Tymnet and Western Union Easylink. The modem features originate and auto-answer modes and permits keyboard and automatic-single-key di-

Now make secure electronic connections as easily as applying tape

Profits, time and labor can get lost in connecting a circuit board and an LCD or a membrane switch. That's why you get pressure to find faster, more economical ways to make a reliable connection.

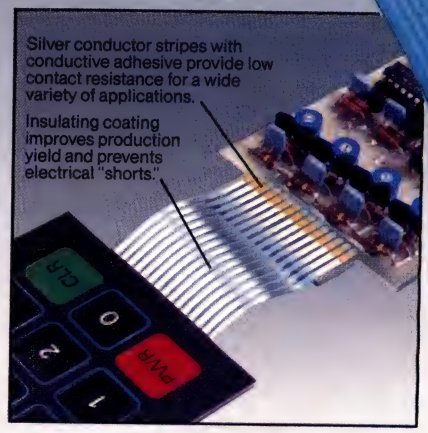
It'd be so easy if you could just tape it together. And even easier if you could automate the process.

Now you can.

Scotchlink Connector Tape is its own connector. Conductive silver stripes, each with a conductive adhesive coating, are regularly spaced on a polymer backing. It's a new technology based on two areas of proven 3M expertise: electrical PSA tapes and mass termination cable.

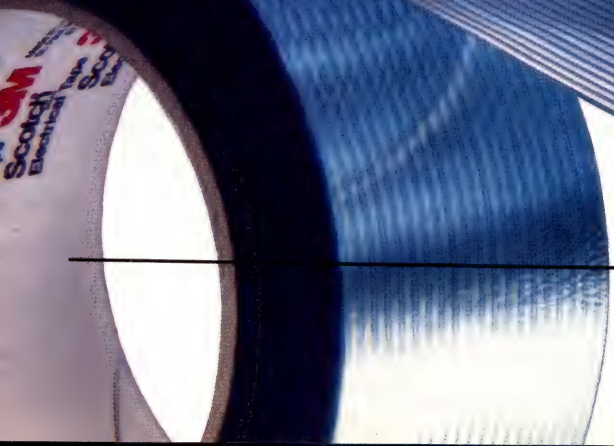
It will save you the labor and cost of clips; reduce assembly time and eliminate contact problems. And spare you the aging problems and mechanical clamping of elastomeric connectors.

In roll form, Scotchlink Tape is ready for automated assembly. Just cut to any length and heat bond in 5 seconds. You reduce inventories on various connector types and standard lengths. Have a contact that can withstand humidity and provide reliable connections even at elevated temperatures. And increase your design options with the tape's light weight and flexibility.



Free Sample is available with detailed literature. Contact Electro-Products Div./3M, 225-4N, St. Paul, MN 55144.

Scotchlink® Connector Tape for reliable, high-speed automated assembly



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CIRCLE NO 78

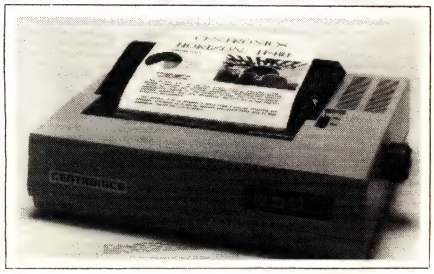
aling. It operates on an unconditioned voice-grade line; receive sensitivity is −40 dBm, and transmit power level equals −9 dBm.

The 12-lb unit measures 14×12×4.5 in. $1495.

Quint Systems, 3693 Commercial Ave, Northbrook, IL 60062. Phone (312) 498-5060.

Circle No 688

DOT-MATRIX PRINTER



Model H80 prints 27 cps in a near-letter-quality mode and 140 cps in a draft-quality mode. Able to produce pica and elite characters, the dot-matrix printer features overstrike, proportional-character and condensed- and expanded-print capability. It can produce half-size and superscripts and subscripts. It accepts fanfold and single-sheet paper from 5 to 10 in. wide and can print an 8-in.-wide line. It also accepts roll paper.

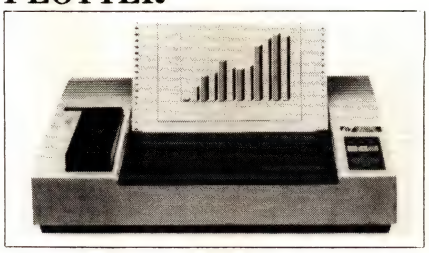
The 18-lb unit's dot-matrix pattern measures 11×9 in the draft-quality mode and 23×16 in the near-letter-quality mode. Horizontal pitch equals 5, 6, 7.5, 8.6, 10, 12 and 17.2 cpi. Other features include underlining and single-, double- and quadruple-density graphics capability, out-of-paper detection, a self-test mode and reverse paper feed.

The printer measures 15.75×12.6×4.3 in. It operates on 120V ac and consumes 120W. It comes standard with its manufacturer's parallel interface; an RS-232C port is optional. $699.

Centronics Data Computer Corp, 1 Wall St, Hudson, NH 03051. Phone (603) 883-0111.

Circle No 689

PLOTTER



Model 4731 Plotwriter is a 4-pen drum plotter capable of producing a 45-line, 104-cpl output at speeds to 7 cps. Selectable plotting areas measure 8½×11 in. or 11×17 in. Able to use ballpoint or fiber-tip pens, the plotter prints 0.11×0.06-in. alphanumeric and 0.11×0.07-in. Katakana and Greek characters. Character spacing equals 0.1 in.; line spacing is 0.16 in. The plotter accepts 12.6-in.×131-ft roll paper.

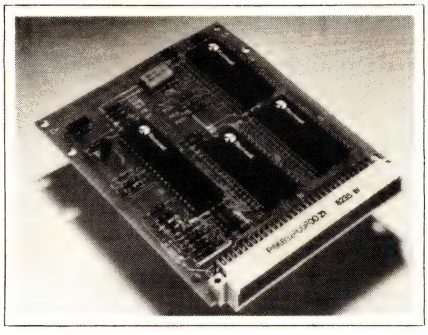
Resolution equals 0.004 in. Repeatability specs at 0.008 in. Pen replacement results in less than 0.012-in. errors. Plotting commands allow the unit to draw straight lines and circles as well as smooth curves through specified points.

The 28-lb, 21.6×11.8×5.8-in. plotter comes with an RS-232C, IEEE-488 or 8-bit-parallel interface. It consumes less than 90 VA. $2500.

Western Graphtec Inc, 12 Chrysler St, Irvine, CA 92714. Phone (800) 854-8385; in CA, (714) 770-6010.

Circle No 691

MODEMS



Available in CCITT V.29 and V.27 bis/ter configurations, Models R96DP and R48DP achieve transmission rates as high as 9600 and 4800 bps, respectively. Plug compatible with their manufacturer's line of 1200- to 9600-bps modems, they permit full-duplex operation over 4-wire dedicated unconditioned lines or half-duplex operation over the switched telephone network.

Other features include a −43- to 0-dBm dynamic range, automatic adaptive equalization, programmable tone generation and RS-232C compatibility, and local analog and remote (locally activated) analog and digital loopback capability. The modems can transfer data to and from a μP via the RS-232C interface or in parallel fashion. A control bit selects serial or parallel operation.

TTL and CMOS compatible, the modems consume 3W typ and measure 4×4.8 in. Model R96DP operates at 9600, 7200, 4800 and 2400 bps; Model R48DP, at 4800 and 2400 bps. The R96DP costs $500; the R48DP, $350 (OEM qty).

Rockwell International, Semiconductor Products Div, Box C, Newport Beach, CA 92660. Phone (714) 833-4700. TWX 910-591-1698.

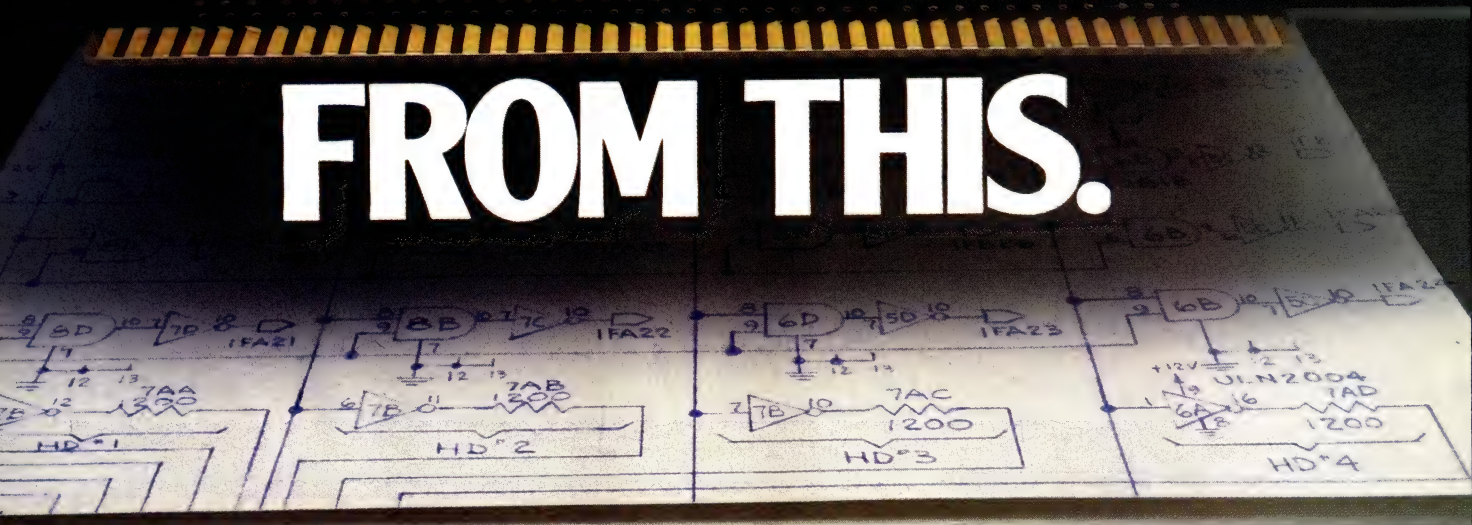
Circle No 692

CONNECTORS



For use with 0.05-in. flat ribbon cable, FT Series insulation-displacement connectors include ejector latches that ensure positive locking of the socket to the header as well as easy detachment. Available with or without strain relief, the headers feature a straight or right-angle design with solder tail. Polarized for correct socket-to-

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MULTIWIRE/WEST 3901 East La Palma Ave., Anaheim, California 92807 (714) 632-7770; MULTIWIRE/ADVANCED MANUFACTURING GROUP 10 Andrews Rd., Hicksville, NY 11801 (516) 938-2000
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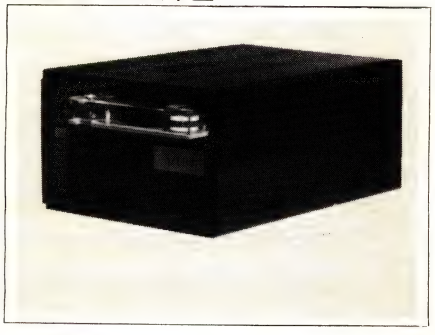
header assembly, the units come in 10-, 14-, 16-, 20-, 26-, 34-, 40-, 50-, 60- and 64-pin versions.

Manufactured with a glass-filled PBT/94V-0 material, the connectors have a 1A current rating and withstand 800V ac for 1 min. Insulation resistance specs at 1000 MΩ min at 500V dc, contact resistance is 30 mΩ max, and operating temperature range equals −25 to +85°C. A 26-position right-angle version with locking latches costs $3.71 (1000).

SMK Electronics, 1901 Nancita Circle, Placentia, CA 92670. Phone (714) 996-0960.

Circle No 693

TAPE DRIVE



A 60M-byte, 9-track, ¼-in. cartridge-tape system, the Cache Cartridge features a QIC 11/24 recording format and an SCSI interface to facilitate data transportability and easy connection to μCs.

A back-end multitasking system, the Cache Cartridge performs tape-to-disk and disk-to-tape data transfers without host intervention. Its 64k-byte cache allows 90k-byte/sec data transfers without requiring special streaming software.

All utilities are menu driven and include help functions. The utilities can perform selective file read/write operations, mirror-image streaming dumps and ASCII/EBCDIC code conversions and read foreign formats. $1995.

S/COM Inc, 352A University Ave, Westwood, MA 02090. Phone (617) 461-0200. TLX 924473.

Circle No 694

DATABASE SOFTWARE

BASIS is an interactive on-line information storage and retrieval system that can handle databases with more than 10M entries. It features term and phrase searching via inverted indices, full thesaurus capabilities and a full formatted screen module for editing and creating records. It permits variable-length data elements and records and allows entire sessions to be saved. In addition, it includes integrated computation capabilities.

The package runs on computers in Control Data Corp's 70, 170 and 6000 Series, DEC's 20, 30 and VAX Series, IBM's 370/155, 30XX and 43XX Series, Prime's X50 Series, Univac's 1100 Series and Wang's VS Series.

The package is written in 85% FORTRAN and 15% assembly code. Training is at either the customer's site or the supplier's office. First-year maintenance is included in the purchase price, which starts at $26,600.

Battelle Software Products Center, 505 King Ave, Columbus, OH 43201. Phone (614) 424-5524.

Circle No 696

DAISY-WHEEL PRINTER



Model 6300 daisy-wheel printer features automatic underscoring, centering and justification as well as proportional spacing and bold and shadow printing. It operates at 40 cps max and accepts Diablo 96-character daisy wheels and Hytype II multistrike ribbons. Users can choose a Centronics parallel or RS-232C serial interface.

The unit consumes 25W idling and 70W running. It comes with a 3k-byte buffer, expandable to 15k bytes. Noise specs at less than 60 dBa. MTBF is 3000 hrs under a 25% duty cycle; mean time to repair is 15 min.

The 31-lb unit measures 23.6×15.7×4.9 in. $1000 to $1200.

Juki Industries of America Inc, 299 Market St, Saddlebrook, NJ 07662. Phone (201) 368-3666. TLX 219022.

Circle No 695

KEYBOARD



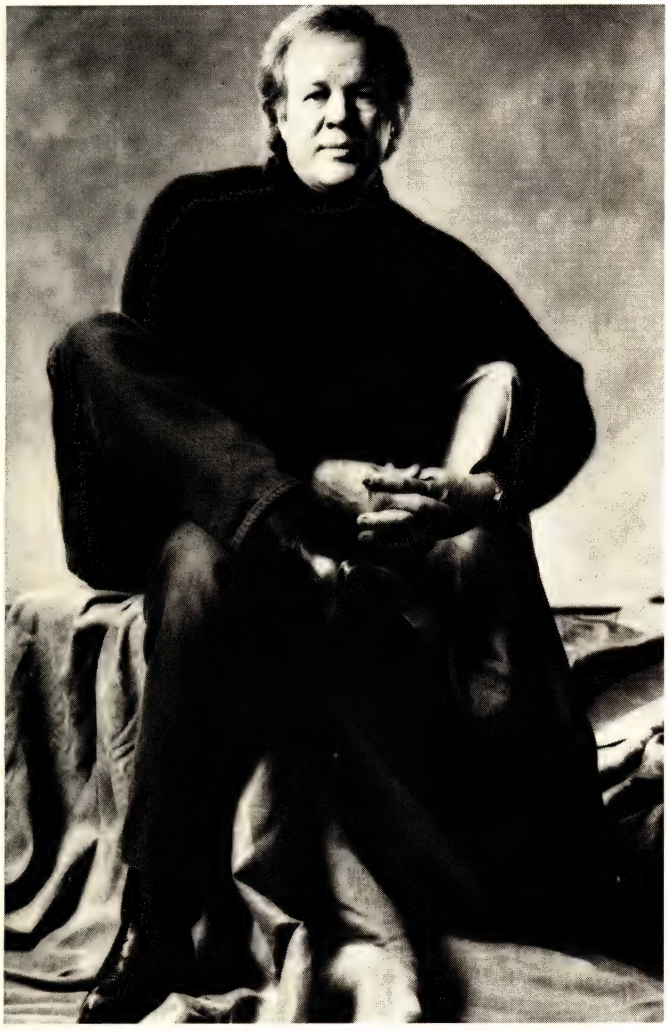
Each KB IV Series sculptured, low-profile keyboard, similar to the IBM PC's keyboard, features top-mounted and removable keycaps. A KB II model, similar to the IBM PCjr's keyboard, features keycaps that can't be removed that are captured by the keyboard's molded frame; keycaps on KB II keyboards don't include legends, which instead appear on easily changeable graphics overlays.

Keyboards in both series provide either linear or tactile feel. The linear version, with a 50M-cycle life, employs a conical metal spring that compresses during actuation. The tactile version has a 30M-cycle life and includes an elastomer layer that forms a dome-shaped spring between each keycap plunger and the keyboard circuit. In high volume, costs average $0.57/key position for fully encoded, serial-output keyboards and $0.37/key position for a non-encoded keyboard. Infrared wireless capability is optional. Delivery for custom designs is 4 to 6 mos ARO.

Cherry Electrical Products Corp, 3600 Sunset Ave, Waukegan, IL 60087. Phone (312) 578-3500.

Circle No 699

"IN 2001, WE REACHED THE STARS. NOW, WE CAN PRACTICALLY TOUCH THEM."



DOUGLAS TRUMBULL
Director. Creator of Oscar Winning Special Effects. Three-Time Oscar Nominee. Film Making Innovator.

The year was 1968.

But for the audience, the year was 2001. And they were not in a movie theater, they were in deep space — propelled by the stunning special effects of Douglas Trumbull.

The incredible realism of "2001. A Space Odyssey" opened new possibilities in film making — which Trumbull explored in "Silent Running," "Close Encounters," "Star Trek," "Blade Runner," and "Brainstorm."

But ultimately, it launched Trumbull on an odyssey that may completely revolutionize films.

"Films try to recreate or record reality. The more lifelike a film is, the more exciting it will be. Right now, I'm trying to create the most lifelike films ever."

Trumbull has developed a new way to shoot and project film that goes beyond 3-D. In "New Magic," his first effort, the images are so sharp and life-like the screen seems nonexistent.

"The difference is astonishing. Yet, all we did was utilize the full potential of the technology. It's that simple."

Trumbull is, perhaps, being too modest. At Hewlett-Packard, we know it takes exceptional skill and commitment to transform mere potential to full reality. That's what sets Hewlett-Packard apart, just as it sets Douglas Trumbull apart.

Like Trumbull, we've found that the superior results justify the effort. And the clear superiority of the HP-41CX Advanced Programmable Calculator is a perfect example.

Compare functionality. The HP-41CX offers 223 built-in functions. But that's just the beginning. You'll have over 2,500 different software programs to choose from.

Compare programmability. The HP-41CX gives you 2.2K bytes of main memory — again, just the beginning. It expands to 6.4K bytes. And the RPN logic of the HP-41CX gives you maximum use of memory through its ability to eliminate scores of extraneous keystrokes.

More functionality. Superior programmability. In short, the power to solve more kinds of technical problems more simply than any other calculator.

The HP-41CX.

Do you need a calculator this capable? That depends. Do you want to merely reach for the stars, or actually touch them?

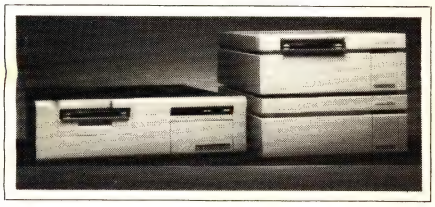


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DISK/TAPE DRIVE



Designed for use with DEC's Q Bus computers, including PDP-11/23, 11/73, Micro/PDP-11 and MicroVAX systems, these 5¼-in. Winchester and ¼-in. tape subsystems furnish 40M- to 140M-byte unformatted capacities. One tape cartridge can provide as much as 20M bytes of backup. A data-buffering scheme handles data transfers between the drive and the Q Bus.

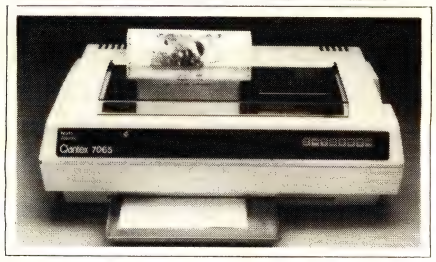
Compatible with DEC's digital storage architecture, the subsystems can run with existing operating systems without requiring software patches.

The drives come in rack-mounting and stackable, tabletop versions. Other features include software diagnostics, power-on confidence tests, on-board self-diagnostic routines and a front-panel digital readout. From $5695 for a 40M-byte Winchester model.

Data Systems Design Inc, 2241 Lundy Ave, San Jose, CA 95131. Phone (408) 946-5800.

Circle No 697

DOT-MATRIX PRINTER



Model 7065 operates at 300 cps in draft mode, 125 cps in near-letter-quality mode, and 65 cps in letter-quality mode. In its graphics mode, it provides resolution of 144×144 dots/in.^{2} and repetition rate of 1500 dots/sec per activated needle.

The unit can store three letter-quality fonts on line. Standard word-processing fonts include Trend and Courier; others are optional. Using escape-code sequences, a host computer can download parameters to the printer, allowing selection of eight character sets, a 1- to 256-line forms length, vertical and horizontal tabs and margins, and vertical pitch. Escape codes also allow users to select print density, proportional spacing and margin justification as well as underlining, automatic-repeat and boldprint features.

Controlled by a Z80 μP, the printer includes a 4.7k-byte input buffer as well as Centronics-compatible parallel and RS-232C serial interfaces. The serial-channel baud rate ranges from 110 to 19,200 bps.

Qantex Div, North Atlantic Industries Inc, 60 Plant Ave, Hauppauge, NY 11788. Phone (800) 645-5292; in NY, (516) 582-6060.

Circle No 698

DATA CABLE



The 8162 Series multipair data cables combine low capacitance (12.5 pF/ft) with a foil and 65%-coverage braid shield and chrome/PVC jacket to allow extended-distance data transmission in RS-232C and RS-422 applications. Shielding on each pair minimizes crosstalk.

The cables employ #24 AWG stranded conductors. Versions are available with 2, 3, 4, 5, 6, 7, 8, 10, 15, 18 and 25 pairs. Representative prices include $464.70 for 1000 ft of 2-pair cable and $3094.50 for 1000 ft of a 25-pair cable.

Belden, 2000 S Batavia Ave, Geneva, IL 60134. Phone (312) 232-8900.

Circle No 700

PORTABLE PC



Compatible with the IBM PC, the Z-160 PC features a detached keyboard, four open expansion slots and 128k bytes of dynamic RAM, upgradable to 640k bytes. The unit's single or dual top-loading disk drive accepts 5¼-in. IBM-format double-sided, double-density diskettes.

The 80-character×25-line, 9-in. amber-phosphor video display comes standard. Color monitors can connect to the unit via a 9-pin RGB output. In color applications, the Z-160 PC comes with a choice of eight background and 16 foreground colors and 320×200-point color-graphics resolution; each graphics point can be one of four colors selectable from one of two color palettes. B/W graphics resolution is 640×200 points.

The keyboard provides 10 function, 17 keypad and 57 alphanumeric keys. An audible click accompanies each keystroke. The unit includes an RS-232C serial and Centronics-compatible parallel interface. It weighs 33 lbs and measures 19.5×8.38×19.13 in. $2799 and $3199 for single- and dual-disk-drive versions, respectively.

Zenith Data Systems, 1000 Milwaukee Ave, Glenview, IL 60025. Phone (312) 391-8744.

Circle No 701



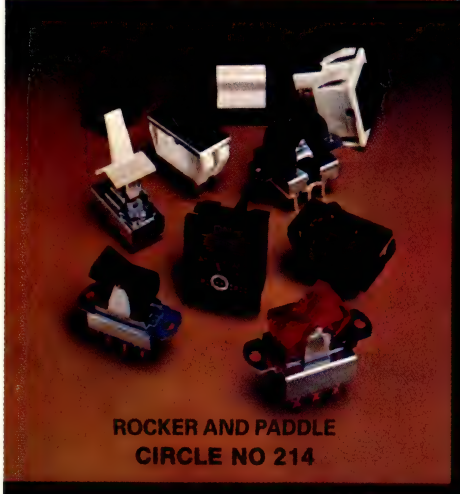
ROTARY
CIRCLE NO 211



SLIDE
CIRCLE NO 212

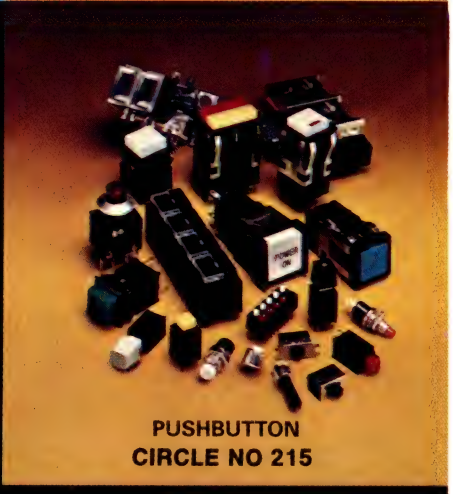


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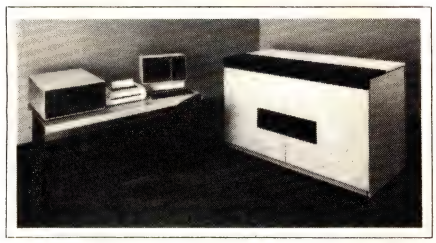
For more product information, catalog or sample, contact your local ITW Switches representative, distributor or ITW Switches, An Illinois Tool Works Company, 6615 West Irving Park Road, Chicago, IL 60634. Phone: (312) 282-4040. TWX: 910/221-0275. Telex 433-0130.

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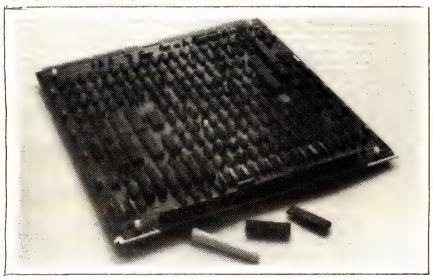
Models 5310 and 5320 computer-output-microfilm systems provide automatic microfiche production from magnetic tapes formatted by a host computer. Model 5310 uses a photographic-chemistry process, while Model 5320 uses heat as the developing agent.

Each unit includes an 8086-μP-based single-board computer that allows it to communicate with the manufacturer's personal computer over an RS-232C cable. The personal computer can thus store on disk job-specific information like page size, lens size and operator prompts. The systems can also use a self-loading tabletop tape drive for data input. A typical configuration costs $67,000.

NCR Micrographic Systems Div, 520 Logue Ave, Mt View, CA 94943. Phone (415) 965-3700.

Circle No 702

CONTROLLERS



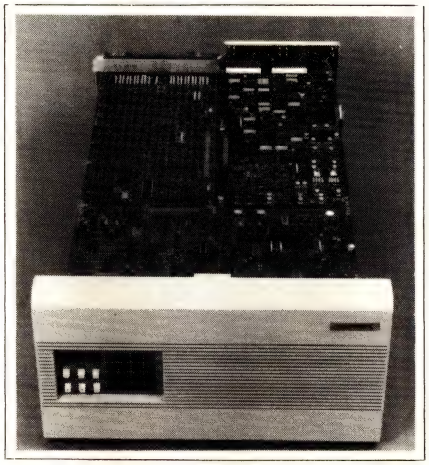
Model ZDF-1 controls disk and tape drives while occupying only a single slot in Data General's Nova/Eclipse Series minicomputers, employing a dedicated μP for each function. In addition, the controller employs EEPROMs to eliminate the need for on-board DIP switches and to allow board configuration from an operator's console.

Similarly employing EEPROMs, the Model BMX-1 single-board disk-drive controller supports as many as four SMD disk drives on Data General computer systems. Both boards are plug compatible with Data General's FCC-compliant chassis. Model ZDF-1 costs $4195; Model BMX-1 costs $4995.

Custom Systems Inc, Zetaco Div, 6850 Shady Oak Rd, Eden Prairie, MN 55344. Phone (612) 941-9480.

Circle No 703

HARD-DISK DRIVE



The Centaurus family of 14-in. Winchester disk drives provides 330M-, 660M- and 825M-bytes unformatted storage capacities in rack-mounting configurations. All three models employ a linear voice-coil actuator in a closed-loop servo system to achieve average access times of less than 25 msec.

Other features include a direct-drive spindle motor, built-in tester, universal ac-input power supply, automatic spindle/carriage locks, and an SMD interface with dual-port capability. The disks can store 40,320 bytes/track; the drives achieve a 1.859M-byte/sec data-transfer rate while maintaining the SMD interface protocol.

The drives employ conventional ferrite heads and oxide media. Field upgrades, requiring exchange of the head/disk assembly, take less than 30 min. The units consume 350W after spin-up. MTBF equals 12,000 hrs. An 825M-byte model costs $8250. Shipments begin in Sept.

Ampex Corp, 401 Broadway, Redwood City, CA 94063. Phone (408) 725-2017.

Circle No 704

UPS



Offering 10 min of backup operation at full load, Model 1350 (shown here with its manufacturer's line of 215- to 750-VA line regulators/conditioners) can drive a 350 VA load. Recharge time specs at 8 hrs max.

The unit accepts a 120V ac (+10, −15%) input at 4A max and delivers a 120V ac output (+5, −15% at full load and +22, −15% at no load). Power-line to UPS transfer takes place at a 102V (typ) input level; transfer back to the line occurs at a 108V (typ) input level. Transfer time specs at 12 msec. The 32-lb unit measures 6×10.75×12.625 in. $750.

Dymarc Industries Inc, 21 Governor's Ct, Baltimore, MD 21207. Phone (800) 638-9098; in MD, (301) 298-9626.

Circle No 707

TERMINAL

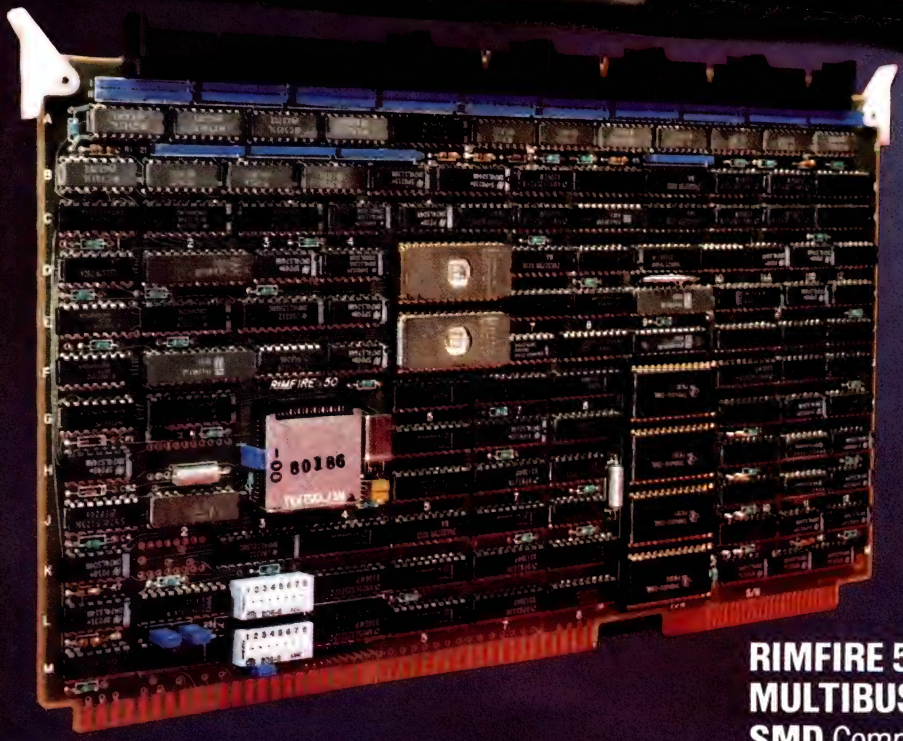
The Freedom 110 low-end smart video terminal has a tilt-and-swivel display, detached 94-key DIN-standard keyboard with numeric pad, and a nonglare display.

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CIRCLE NO 82

NCC '84

or status-line set-up modes, 15 thin-line graphics characters, nine cursor-control keys, eight editing keys, screen time-out, a bidirectional buffered auxiliary port, eight foreign character sets, and built-in self test. The 7×9-dot characters are displayed in a 9×12 matrix.

The terminal also provides block, conversation, monitor and local communication modes. It emulates the Televideo 910, ADDS Regent 25, Lear-Siegler ADM 3A/5 and the Hazeltine 1420. $595. An optional amber-phosphor screen adds $25.

Liberty Electronics, 625 3rd St, San Francisco, CA 94107. Phone (415) 543-7000. TLX 470439.

Circle No 708

CAD SOFTWARE



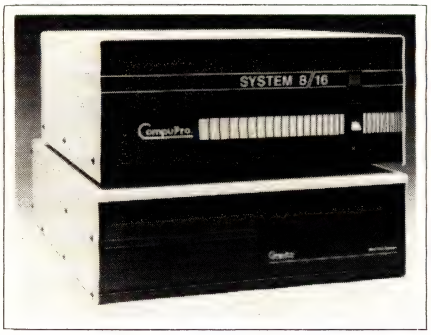
A pc-board-artwork editor for the IBM Personal Computer, smART-WORK allows interactive control over the placement and routing process. The program permits quick correction and revision of artwork, increasing design productivity.

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Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (317) 742-8428.

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Software supplied with the system includes Bell Labs's UNIX version 4.2 operating system as well as the C and FORTRAN languages. $19,995. Available 3rd qtr.

Compupro, 3506 Breakwater Ct, Hayward, CA 94545. Phone (415) 786-0909.

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Nova Electric Manufacturing Co, 263 Hillside Ave, Nutley, NJ 07110. Phone (201) 661-3434.

Circle No 709

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If you design with linear integrated circuits or if you are planning to use gate arrays, semicustom, or custom integrated circuits, you will find these proceedings invaluable.

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Unique new circuits covered include monolithic active filters, fast and accurate sample/hold amplifiers, switching regulators, CMOS linear devices, analog multiplexers, FET-input operational amplifiers, drivers, interface circuits, and more.

Each talk in the proceedings was prepared to help engineers learn about the features and applications of new devices. The authors are applications engineers and are familiar with the problems commonly encountered in designing with integrated circuits. Each paper deals with application considerations and many include actual design examples.

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Topics presented include ways to go custom, how to get started, advantages of cell library systems, choosing parameters for a custom circuit, personalizing gate arrays, the role of computer aided design, testing gate arrays, linear custom products, and customer owned tooling.

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MOSFETs, Schottky diodes vie for low-voltage-supply designs

Lower R_{DS} renders power MOSFETs competitive with Schottky diodes for low-voltage, high-current power supplies. However, to take full advantage of power-MOSFET performance, carefully consider circuit implementation.

Richard Blanchard *and* **Rudy Severns,**
Siliconix Inc

Designers of low-voltage, high-current power supplies face a perennial problem: How do you overcome the efficiency loss imposed by the offset voltage inherent in Schottky and pn junction diodes? MOSFET-based synchronous rectifiers can provide a solution to the problem, serving as practical alternatives to Schottky rectifiers, particularly for outputs below 5V. (To understand how you optimize MOSFET devices for power applications, see **box,** "Power MOSFETs: the inside story.")

To exploit the opportunity provided by the MOSFET, however, designers must answer several questions. What's the basis for choosing between a MOSFET and a Schottky diode in a given application? What extra drive circuitry is needed when you use a synchronous rectifier in place of a line-commutated diode? What are the performance limits? How do you use the device in a circuit to take advantage of its characteristics?

Efficiency dictates rectifier choice

When choosing between rectifier types, efficiency provides the most important selection criterion. In low-voltage power supplies, losses in the rectifiers dominate overall efficiency (η). The relationship between efficiency and the rectifier forward drop V_R can be expressed as

$$\eta = \frac{1 - \beta}{1 + \frac{V_r}{V_O}},$$

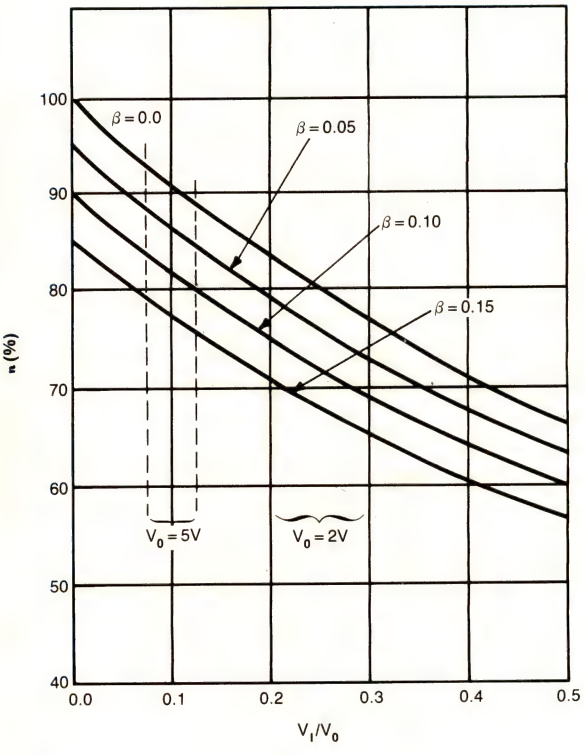


Fig 1—The rectifier's forward drop V_R *is a major factor in determining power-supply efficiency at low output voltages. For outputs of 2 and 5V, there's a marked difference in efficiency as V_R changes from 0.4 to 0.6V.*

Schottky diode's offset voltage imposes efficiency penalty

where β equals the percentage of power dissipated within the power supply, and V_O equals the nominal output voltage. When you look at a graphic presentation of this equation (**Fig 1**), it's clear that with a low output voltage, the rectifier's forward drop is a major factor in overall efficiency regardless of other circuit losses. That doesn't mean, however, that losses in addition to forward drop are insignificant.

Reverse leakage current, for example, is the most prominent of these additional losses in a Schottky diode. It can be substantial at junction temperatures of 100 to 150°C, the normal operating range for the device. The Schottky diode's high capacitance also creates problems. Losses related to capacitance charging and discharging are relatively small. However, large current spikes can develop in high-frequency inverters

Power MOSFETs: the inside story

In a typical device-introduction cycle, manufacturers of power MOSFETs first provide transistor selections that perform across a broad voltage range, and then they optimize devices for certain applications, for example, low-voltage rectification. There are many designs for power MOSFETs presently in use. Unfortunately, most of these structures were originally optimized for service over a 100 to 400V operating range. As a result, they do not reflect the practical limits attainable for On resistance when it comes to low-voltage applications. In fact, tests show that considerable improvement remains to be achieved below 100V.

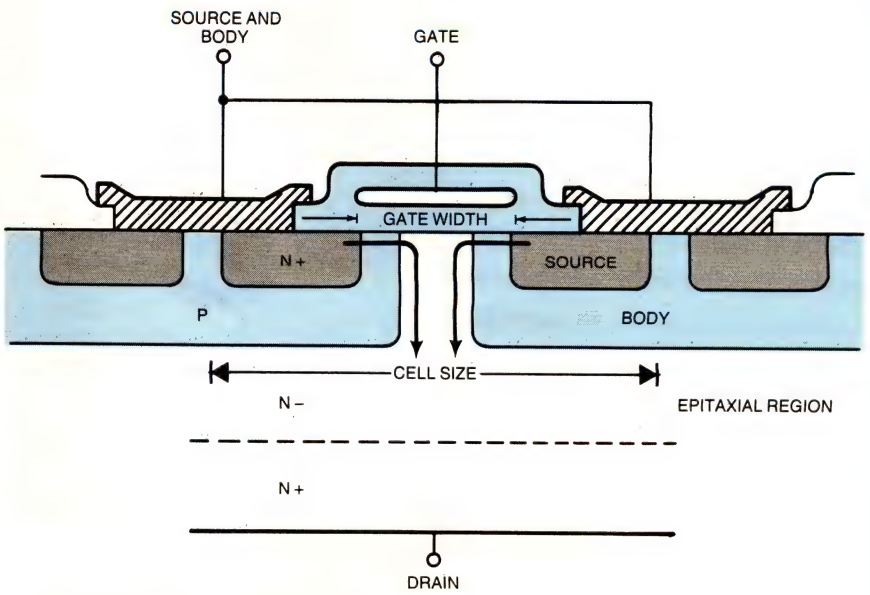
A look at the cross section of a contemporary MOS transistor (**figure**) illustrates how manufacturers minimize a device's On resistance. First, they employ the thinnest and lowest-resistivity epitaxial layer that's consistent with the required breakdown voltage. Second, they must optimize gate width. If it's too wide, surface utilization is poor; if it's too narrow, the JFET formed by body regions results in an unwanted increase in total resistance. The surface geometry also must be optimized to squeeze maximum performance from the devices. Increased chip area will also reduce resistance, but in practice, this usually involves paralleling several dies.

Layout efficiency varies with the surface geometry. There is a wide variety of layouts: linear geometry, square on square grid, circle on square grid, hexagon on square grid, square on hexagonal grid, circle on hexagonal grid and hexagon on hexagonal grid. Though the areas of these geometries vary to just a small degree, the square-on-hex layout is more efficient than the rest. Keep in mind optimal design depends on breakdown voltage and drain current (for high-current devices).

Low-voltage, high-current devices using some of these optimizing techniques are beginning to appear (**table**). While the devices listed are practical synchronous rectifiers, they are by no means fully optimized. Significant improvement (by a factor of 2 or more) should be possible.

SYNCHRONOUS RECTIFIER PARAMETERS

DEVICE	PACKAGE	ON RESISTANCE	BREAKDOWN	CURRENT
SILICONIX VNC003A	TO-3	0.035Ω	60V	60A
MOTOROLA POWER MODULE	EPOXY MODULE	0.018Ω	50V	100A



To minimize On resistance, *MOS-transistor manufacturers employ the thinnest and lowest-resistivity epitaxial layer possible that's consistent with the breakdown-voltage rating.*

(greater than 100 kHz) where the primary switches' transition times measure 20 nsec or less. These spikes can increase dissipation and peak-power stress in the primary switches.

Reverse-leakage current is insignificant in a MOSFET, and capacitance can be as much as an order of magnitude lower than that of a Schottky diode. This lower capacitance is particularly significant for high-speed conversion. Given the MOSFET's short transition-time capability, a synchronous rectifier's operating frequency can approach 1 MHz in switch-mode converters. Even higher operating frequencies are possible in resonant converters.

To put the efficiency question in perspective, look at the power-loss equations for the Schottky diode and the MOSFET. For the diode,

$$P_S = I^2_{L(rms)}\, R_B + I_L V_{OS} + P_I,$$

where: I_L = average output current
$I^2_{L(rms)}$ = RMS diode current
R_B = diode bulk resistance
V_{OS} = diode offset voltage
P_I = losses due to leakage.

For the MOSFET,

$$P_M = I^2_{L(rms)}\, R_{DS(ON)}.$$

By evaluating the difference between these two equations, you can determine which device is superior in a particular application. In terms of power saved by using a MOSFET, this operation yields the equation

$$P_{SAVED} = I^2_{L(rms)}\,(R_B - R_{DS}) + I_L V_{OS} + P_L.$$

Using typical values for R_B, V_{OS} and a range of values for R_{DS}, you can graph this equation (**Fig 2**) to simplify the task of selecting the most efficient device. If P_{SAVED} is positive, the MOSFET has the edge. When P_{SAVED} is negative, the Schottky diode is the superior device for the application.

It's important to realize that though the graph in **Fig 2** is a useful tool, it does not take all efficiency factors into account. For example, as the rectifier's efficiency changes the rms currents in the transformer's windings, the primary switches and the filter capacitors also change. Because most of these losses are proportional

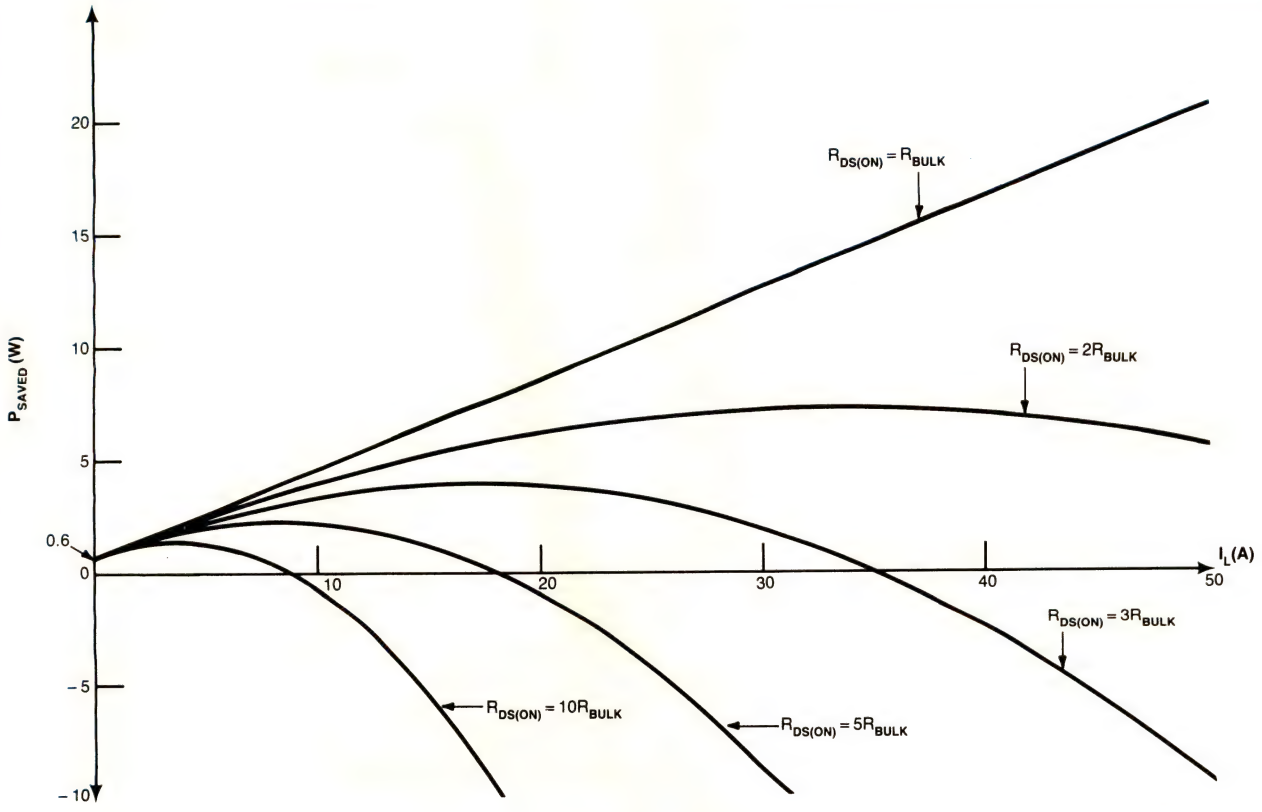


Fig 2—To simplify the choice between a power MOSFET *and a Schottky diode for any given application, simply look at the polarity of the power-saved parameter. Positive values favor the power MOSFET, while negative levels dictate the use of Schottky devices.*

to I^2_{rms}, as the rectifier's efficiency improves, the value for β (the percentage of power dissipated within the power supply) also improves significantly.

The curves in **Fig 2**'s graph also do not include the temperature effect on R_{DS}, R_D, V_{OS} and P_I. R_{DS}, R_B and P_I all increase with temperature, while V_{OS} increases as T_J decreases. At lower junction temperatures, therefore, P_{SAVED} increasingly favors the MOSFET. It's important to consider this behavior when comparing devices.

There are several other factors to appraise when using power MOSFETs for synchronous rectification. You must not exceed maximum gate-to-source voltage limits as called out on the manufacturer's data sheet. This sounds like a straightforward task, but the dynamic behavior of switching circuits such as those found in switch-mode power supplies often results in unexpected transients. Careful design and analysis will help you avoid problems caused by unexpected voltage excursions.

Not your typical operating scheme

If you decide to employ a power MOSFET, you can't simply drop it into your circuit in place of a Schottky diode. This is because the performance of a power MOSFET operating as a synchronous rectifier differs significantly from that in either linear or switching applications. For one thing, a power MOSFET conducts current equally well in both directions. Therefore, a power MOSFET's gating must be properly timed to achieve rectification (hence the term "synchronous rectifier"), and its operating point must be selected to avoid intrinsic-diode turn-on. Such a condition can alter circuit performance, because the device's reverse-recovery characteristics allow current to flow for some time after the voltage reverses.

The presence of minority carriers resulting from intrinsic-diode conduction can have other effects on circuit performance. Carriers present in the body-drain junction region reduce the dV/dt limit of a power MOSFET.

You also have to address current-related problems. Power MOSFETs do not maintain their resistor-like characteristics as the current increases. First, an increase in current forces more carriers through the channel region, causing a transverse voltage drop. The channel region then narrows, and current flowing through the device reaches saturation, resulting in increased On resistance. Device heating arising from increased current also increases channel resistance.

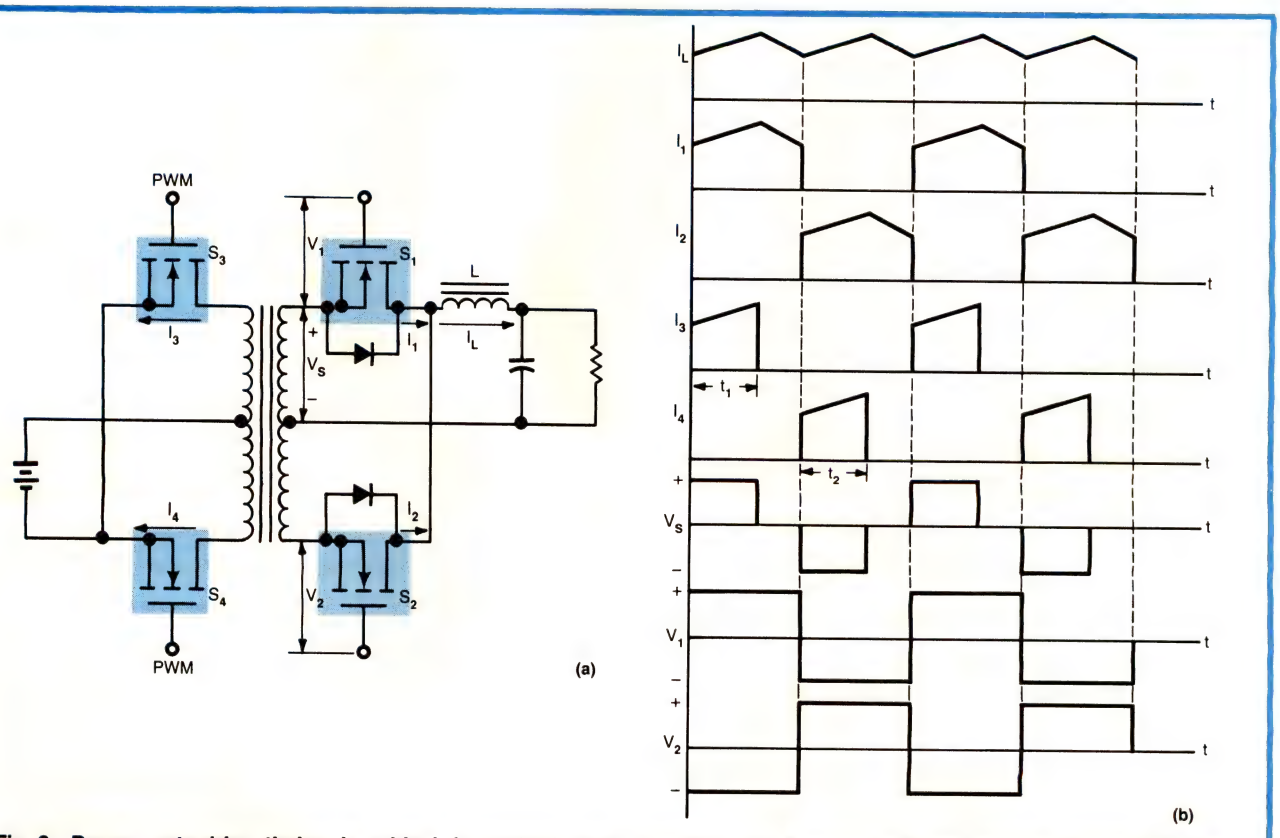


Fig 3—Proper gate-drive timing is critical *for optimal circuit operation, but it varies with the converter design. For the quasi-square-wave converter* ***(a)****, proper timing for* I_1 *and* I_2 *conduction* ***(b)*** *occurs with a 50% duty-cycle drive in phase with* V_S.

With these operational considerations in mind, you're ready to address some of the details of designing power MOSFETs into synchronous-rectifier-based supplies.

Correct timing is all important

Gate-drive timing is critical to proper circuit operation. Unfortunately, proper timing considerations vary with the type of converter circuit used. The popular quasi-square-wave converter circuit (**Fig 3a**) provides a good example.

As the voltage and current waveforms illustrate (**b**), the proper timing for I_1 and I_2 conduction occurs with a 50% duty-cycle drive, which is in phase with V_S. However, when you configure the converter using a regular diode in place of the MOSFET, the current waveforms change completely (**Fig 4**). Notice that during the intervals when both S_3 and S_4 are Off, I_L divides more or less equally between the two rectifiers.

From a loss point of view, this change in waveform isn't significant in a diode. However, to reduce power losses in power-MOSFET-based synchronous rectifiers, you must change the driving scheme (**Fig 5**) to generate similar current waveforms (without t_{rr} spikes). This drive-timing scheme improves efficiency, because conduction losses in a power MOSFET are proportional to the rms current. The extended conduction interval thus provides a waveform having a lower rms for the same average current than in the quasi-square-wave design.

Now examine what happens when gate timing varies from the ideal. There are two possibilities worth analyzing: conduction intervals that are too short and conduction intervals that are too long. If S_1's conduction interval terminates early, I_1 must continue to flow (the switch is in series with an inductor), and it will do so through the integral diode within the MOSFET. This current flow is not catastrophic, but it will increase overall losses because of the diode's higher forward-voltage drop. It will also introduce reverse-recovery current spikes, and it can aggravate the dV/dt problem.

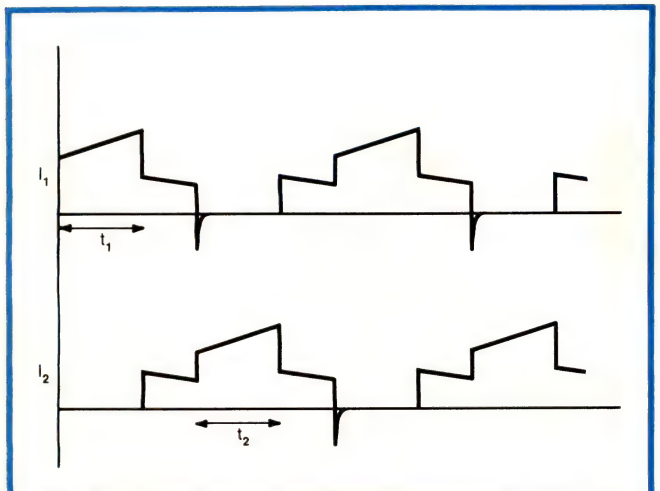


Fig 4—Current waveforms change completely *when you configure the quasi-square-wave converter with a regular diode in place of a power MOSFET.*

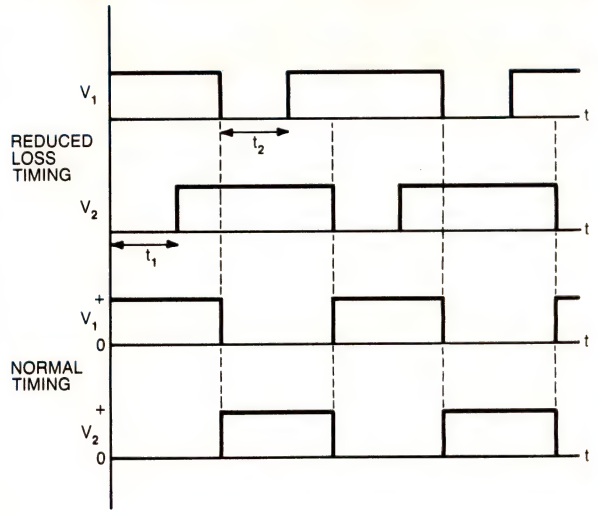


Fig 5—To generate current waveforms *that are free of t_{rr} spikes, you must reduce power losses in power-MOSFET-based synchronous rectifiers.*

If the conduction interval is too long, there's a possibility that S_1, S_2 and either S_3 or S_4 will be On simultaneously. As a result, the secondary will be short circuited for some period of time, and the primary switches will see a large current spike. This is clearly an undesirable situation. Fortunately, MOSFETs are easy to drive, and they switch rapidly, so you can avoid these problems with careful drive-circuit design.

For other converter circuits, the consequences of mistiming could be quite different. For example, in the buck converter (**Fig 6**), there's no advantage to extending the conduction interval beyond 50%, as there was in the quasi-square-wave converter. On the other hand, if the conduction interval does become too long, the current-limiting action of the input inductor won't impress current spikes on the primary switch. This performance is definitely an improvement over that of the quasi-square-wave circuit. The buck-derived converter also handles a conduction interval that's too short by allowing the integral diode to conduct.

The boost converter circuit (**Fig 7**) is even more tolerant of long conduction intervals. Though a 50% duty cycle is favored for drive-circuit simplicity, the circuit will accommodate duty cycles well beyond 50%, because the primary inductor will again limit switch-current transients. With this converter circuit, in fact, you can use synchronous rectifiers for output control if their conduction duty cycles are greater than 50%.

To realize such performance, you simply vary the conduction duty cycles of S_1 and S_2 so that both switches are On simultaneously for part of the switching sequence. You can thus achieve regulation without having to couple a control signal back to the primary circuit—a significant design simplification. Clearly, gate-drive timing requirements and the degree of tolerance to mistiming depend on which converter circuit you use.

Design drive circuit with care

The most basic method of providing gate drive uses an auxiliary winding on the transformer's secondary (**Fig 8**). The scheme's simplicity is definitely a positive factor, but it does have some disadvantages. To illustrate, consider what happens when you use an auxiliary winding with the quasi-square-wave converter circuit.

When the driving transistors are both Off (a condition that occurs twice each switching cycle), $V_1=0$, so there's no gate drive to synchronous rectifier S_1. While I_1 continues to flow, it now goes through S_1's integral diode and increases the power losses.

This isn't the only problem you'll run into using auxiliary-winding drives in the quasi-square-wave family of converter circuits. You could destroy the synchronous rectifier, because the voltages of the transformer's gate-driving winding are directly proportional to input-voltage levels. If the gate-drive voltage equals 12V when the input voltage is low, it will rise to 24V when the input voltage is doubled—not an uncommon requirement. Most MOSFETs spec a ±20V limit for gate

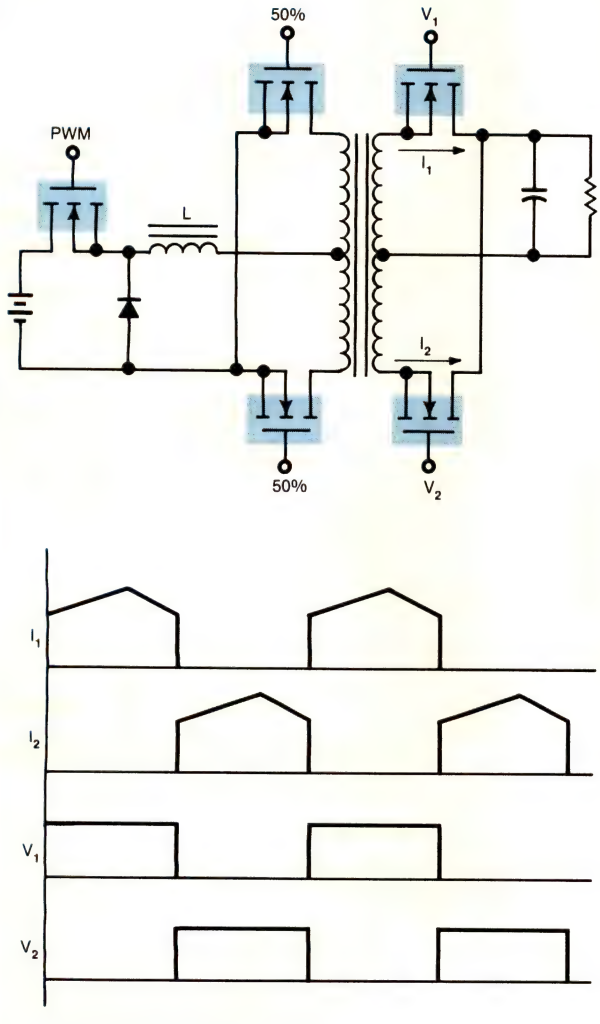


Fig 6—There's no advantage to extending *the conduction interval beyond 50% in the buck-derived converter circuit.*

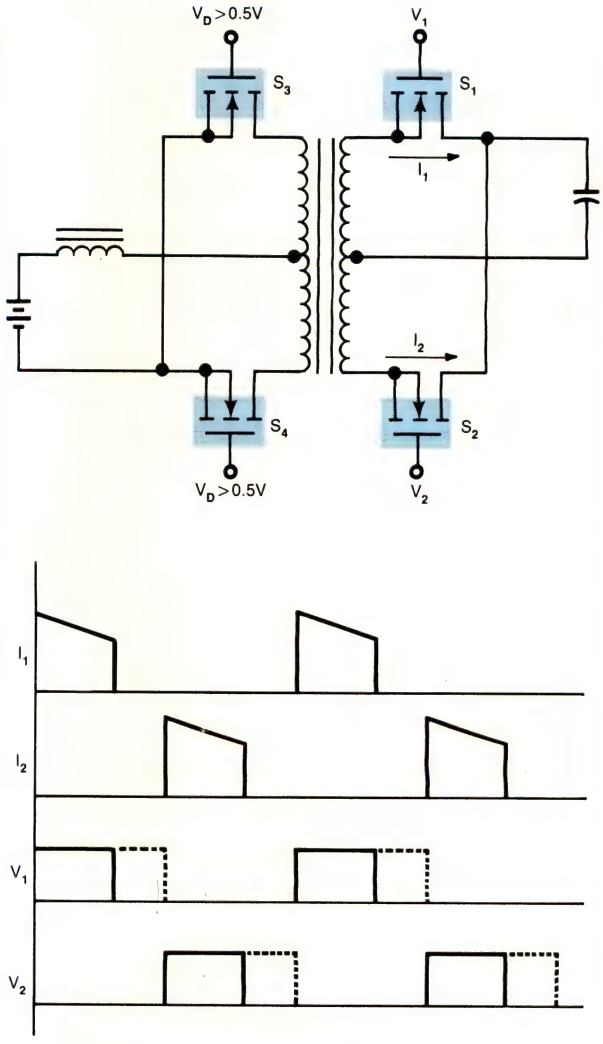


Fig 7—When it comes to tolerating long conduction intervals, *the boost-derived converter proves to be the most flexible.*

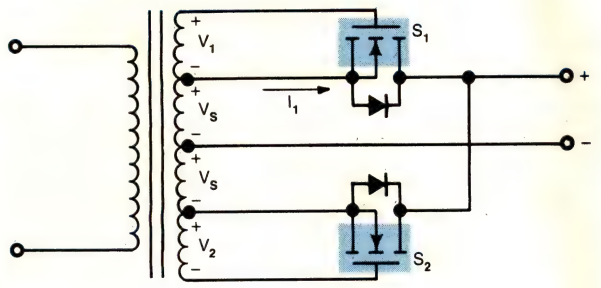


Fig 8—The most basic gate-driving scheme *employs an auxiliary winding on the transformer's secondary.*

voltage; exceed this level and you'll destroy the device. You can, of course, adjust the winding so that the gate drive is below 20V for a high line condition. This could, however, produce insufficient gate drive at low line levels and thereby increase conduction losses.

The winding voltage's dependence on input voltage also increases the peak voltage levels seen by the rectifiers. For a 5V output, for example, the rectifier commonly sees a peak voltage (not including noise or transients) of 20 to 25V. For a relatively high rectifier-voltage rating (in proportion to nominal output voltage), this requirement means that the R_{DS} of the MOSFET must be higher for a given device's current-carrying capacity.

You can easily overcome all of these problems with a different converter circuit. Both the buck- and boost-derived current-fed converters have correct timing and a relatively constant gate voltage when used with an auxiliary winding. In addition, the rectifier only sees a reverse voltage equal to twice the output (10V in a 5V supply), regardless of the input voltage.

Gates require protection

Drive-circuit design involves more than the choice of a converter. Even the best-designed converter has some noise, ringing and transients appearing across the transformer's windings. In converters employing an auxiliary-winding drive, these transients couple directly into the gate, where they could cause timing problems or even destroy the gate. You can avoid such problems by providing some form of gate protection **(Fig 9).** You must locate protective components close to the switching devices to minimize series inductance. The protection scheme should also have a response time in the nanosecond range. Not all transient suppressors and zeners have this response capability.

Note also that the source connection for the gate-drive in **Fig 9** is brought out separately. This technique reduces pick-up problems that might develop as a result of high current in the source lead. You can provide additional protection by bringing the drive winding to the FET via a twisted pair.

The circuit also employs damping resistors across the gates. Without such precautions, winding and drive-circuit leakage inductance can resonate with gate capacitance to generate a ringing voltage on the gate. This ringing could damage the gate or cause spurious switching. Although you can use either series or shunt resistances for damping, the series option has the disadvantage of reducing the switching speed. For ringing frequencies greater than 1 MHz, you can use a ferrite bead for damping. This technique also minimizes parasitic oscillation.

Other drive circuits are possible

Of course, the auxiliary-winding scheme is not the only drive technique available. You can, for example, use a separate drive source derived from the primary-switch circuit **(Fig 10).** An independent gate drive does offer several advantages.

For one thing, switching speeds are typically faster. It's much easier to provide gate protection, and precise gate drive is easily achieved. You can also optimize V_{GS} at a predetermined value and eliminate the negative part of the drive to reduce drive power and gate stress. In some circuits **(Fig 7),** it's even possible for the rectifiers to perform control functions.

Unfortunately, you must pay a price for such performance. Increased circuit complexity is an obvious disadvantage. The increase in complexity, however, is not monumental, so the option is worth examining.

Addressing triggering, thermal problems

Whatever drive scheme you use, make sure the device's integral diode is not allowed to conduct. The absence of conduction reduces loss and eliminates the

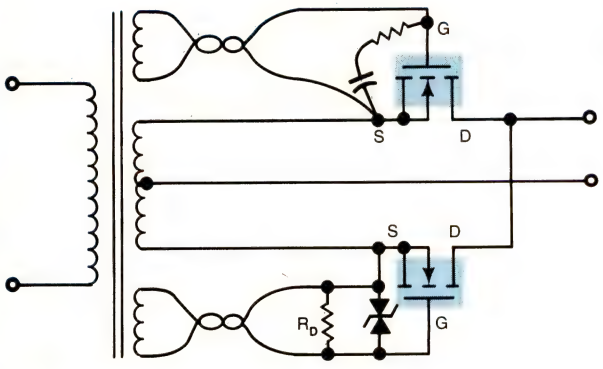


Fig 9—Some form of gate protection *is required to avoid noise-related problems when the converter employs an auxiliary-winding gate drive.*

Gate-drive mistiming tolerance depends on converter circuit used

diode's reverse-recovery current spikes. More important, it helps preserve static dV/dt characteristics.

As long as there's no reverse diode current, most MOSFETs stay Off with an applied dV/dt of 50 to 100V/nsec. It's quite unlikely that a low-voltage power supply will even approach this limit. However, when diode current is present, the dV/dt capability could fall to a value as low as 0.5V/nsec, a rate that's possible even in low-voltage supplies. Triggering a synchronous rectifier on during reverse-voltage conditions effectively short-circuits the transformer's secondary and could result in damage.

There are also temperature aspects to consider. R_{DS} is a positive function of junction temperature T_J, and when a current source (the inductor) controls I_D, positive thermal feedback develops. As the FET becomes hotter, R_{DS} increases. This in turn increases power dissipation, which increases the junction temperature even further. For this reason, it's extremely important to observe good thermal-design practices. In fact, efficiency relies heavily on good thermal design.

There is hope for a solution to the problem. Cryogenically cooled equipment is becoming relatively common, and the low temperatures associated with such equipment provide a unique opportunity to reduce conduction losses drastically. A power MOSFET will work just fine at liquid-nitrogen (−196°C) and liquid-helium (−265°C) temperatures. At a −196°C junction temperature, R_{DS} measures only 20 to 25% of its value at T_J=125°C. As an added bonus, heat transfer is much better because of silicon's higher thermal conductivity at these temperatures. Switching properties are not affected significantly, so you should use cryogenic cooling if it's available.

There's one final thermal consideration—I_D reduction. Conduction loss in a MOSFET is defined by the expression

$$P_C=(I_{D(rms)})^2(R_{DS}).$$

Because R_{DS} is a function of T_J, and T_J is a function of $I_{D(rms)}$, R_{DS} is also a function of I_D. In essence, P_C is proportional to $I_D\alpha$, where $\alpha>2$.

High efficiency requires that $I_{D(rms)}$ be as small as possible, and there are practical ways to accomplish this. You can, for example, make the averaging inductor larger, which changes the shape of the current waveforms (**Fig 11**). While both of these typical switching waveforms have identical average currents, rms current decreases as inductance increases. When you raise the ratio of the two values to the 2.5 power, the power-loss difference measures almost 40%. Clearly, the averaging inductor's value is critical.

Circuit design also has an effect on the rms current.

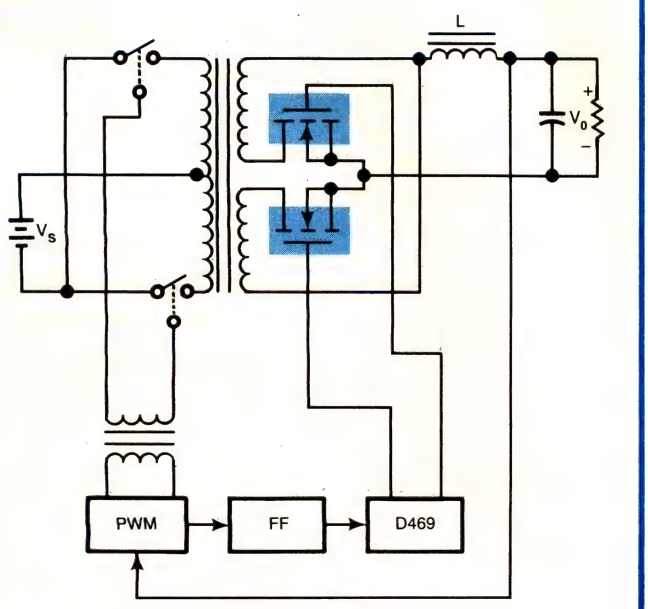


Fig 10—Faster switching speed is a key advantage *of an independent gate-driving scheme. It also simplifies the task of providing gate protection.*

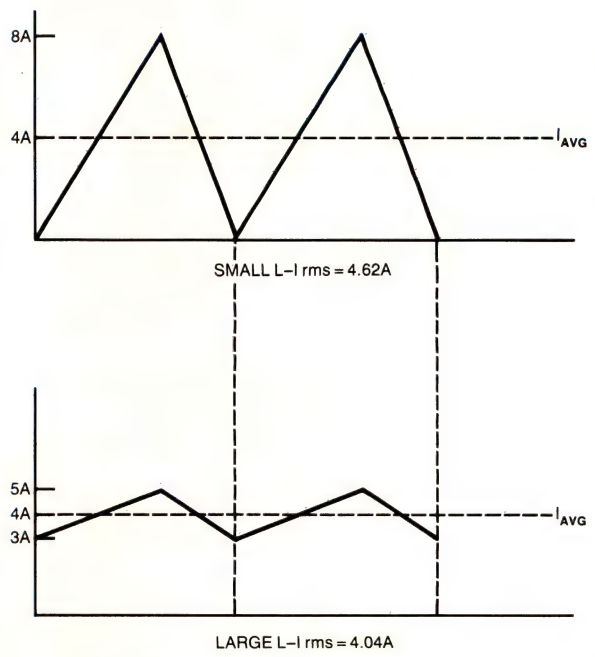
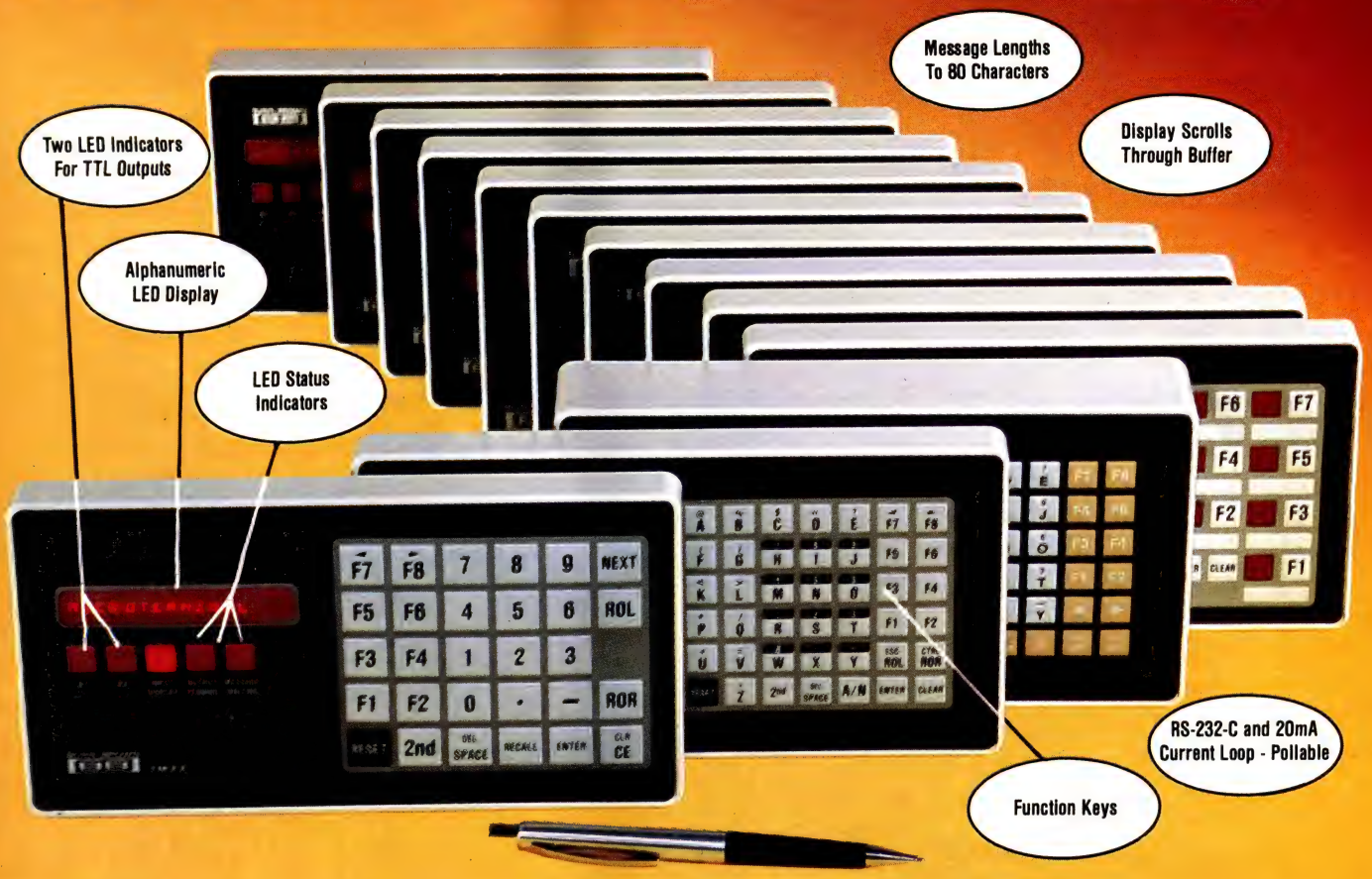


Fig 11—By using a large inductance *to reduce rms current, you can improve converter efficiency.*

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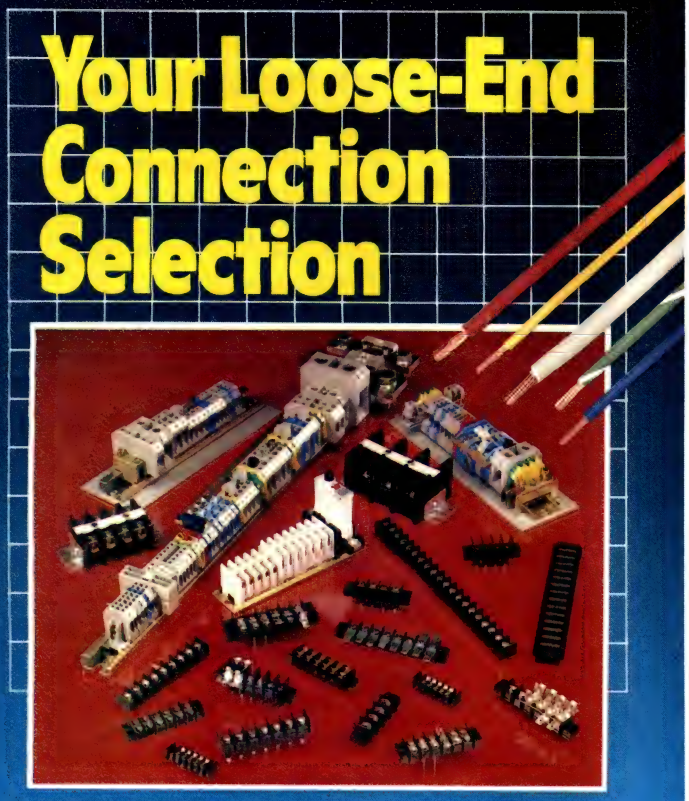
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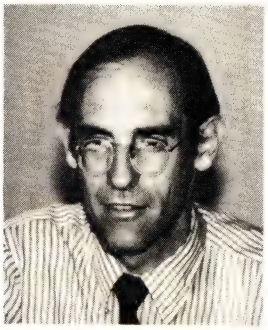
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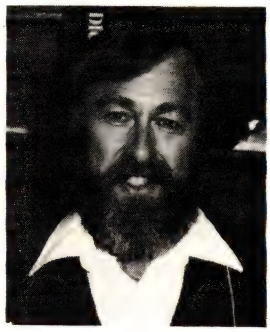
Simplest gate-drive scheme uses auxiliary transformer winding

For the same output current, for example, the circuits in **Figs 3** and **6** have a lower rms rectifier current than the circuit shown in **Fig 7.** This occurs because of the pulsating nature of the output current in any boost-derived converter. **EDN**

Authors' biographies



Richard Blanchard is director of engineering at Siliconix Inc (Santa Clara, CA) where he coordinates the development of new devices, circuits and processes. Holder of two patents and a member of IEEE and ECS, he's earned BSEE and MSEE degrees from MIT and a PhD degree in engineering from Stanford University. In his spare time, Richard enjoys woodworking, hiking and bicycling.



Rudy Severns is a senior staff engineer involved with product applications at Siliconix Inc. He holds a BSEE degree from UCLA and lists ocean sailing as his main leisure-time activity.

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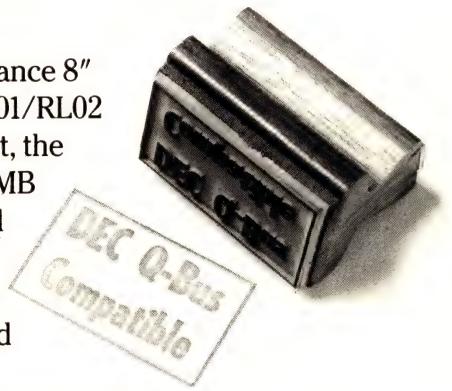
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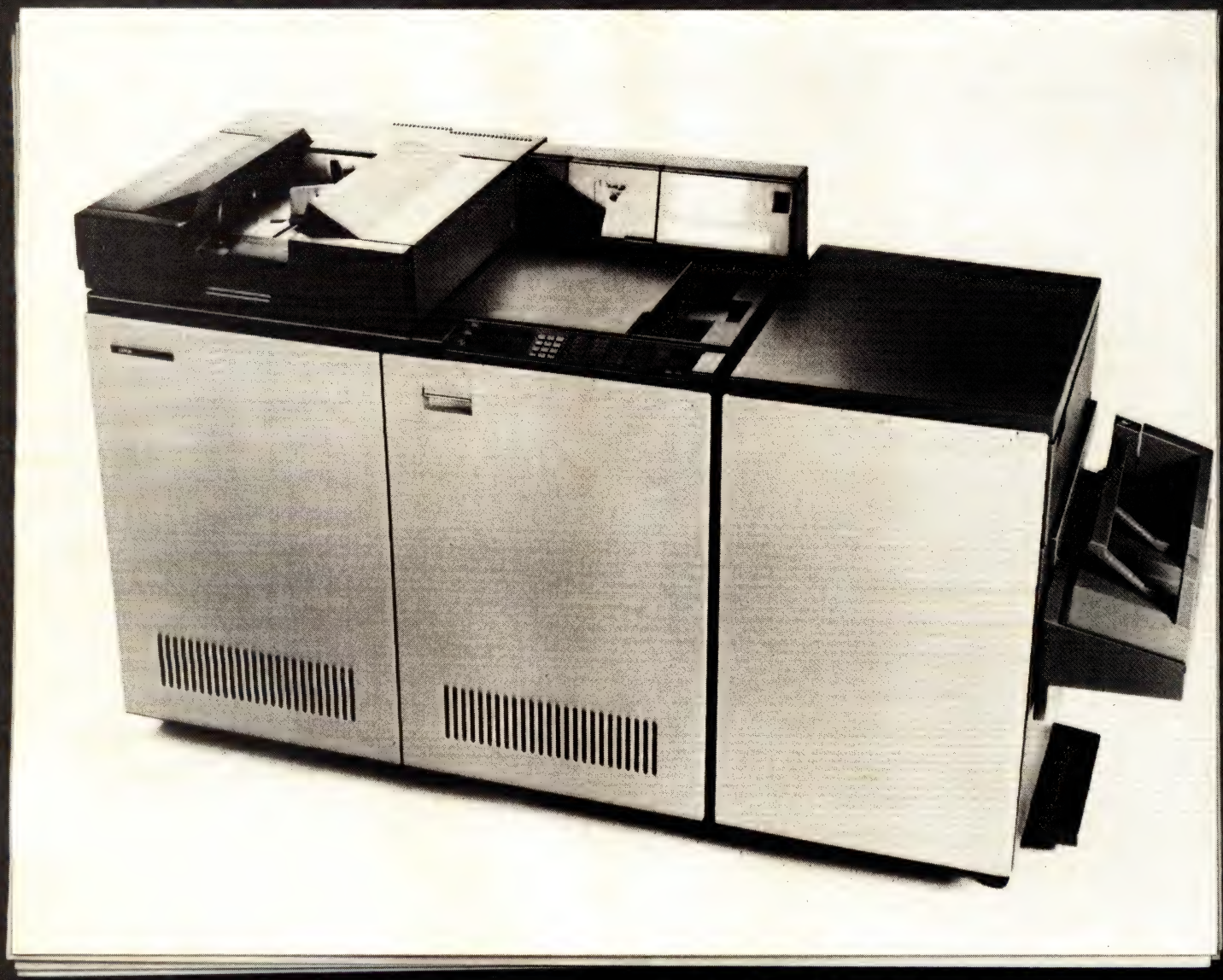
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CIRCLE NO 86

This Xerox machine was made possible



The 1075 Marathon Copier (at the left) represented a whole new level of technology for Xerox: a copier that could think for itself, analyze input, make decisions and turn out copies like those above.

Just as remarkable is the machine that helped plan, manage and expedite it: the Xerox Star 8010 professional workstation (at the right).

"Star was worth it for the graphics alone," said one Xerox engineer. "With it, we could sketch out the parts we needed, change the dimensions and locations electronically, print out hard copies for our suppliers and store everything in the memory. In no time at all, we had a family tree of components."

For a Chief Engineer, "forms and more forms" was his primary use for Star. "It's hooked up to an Ethernet, so it's a breeze to get tooling authorizations, for example, through the electronic mail."

"We also use it to document problems in design iterations, in testing—we can incorporate changes so much faster and easier."

XEROX

by this Xerox machine.



Another engineer regularly used Star for its 3270 and TTY emulation capabilities—"for highlighting infant mortality and installation problems. We would take data generated by the field and use the TTY to pull it back into the network."

An engineer at the Xerox plant in Webster, N.Y., feels Star has given him a kind of extra edge over the competition. "We've been able to use a lot of Xerox innovations like the mouse, icons, windows, property sheets and combined text and graphics for some time now. I can't tell you how easy it's made all the administrative details."

A Xerox Project leader summed it up: "Star gives us more control over what we do. Actually, I think it's one of the most useful tools we've ever used in an engineering environment."

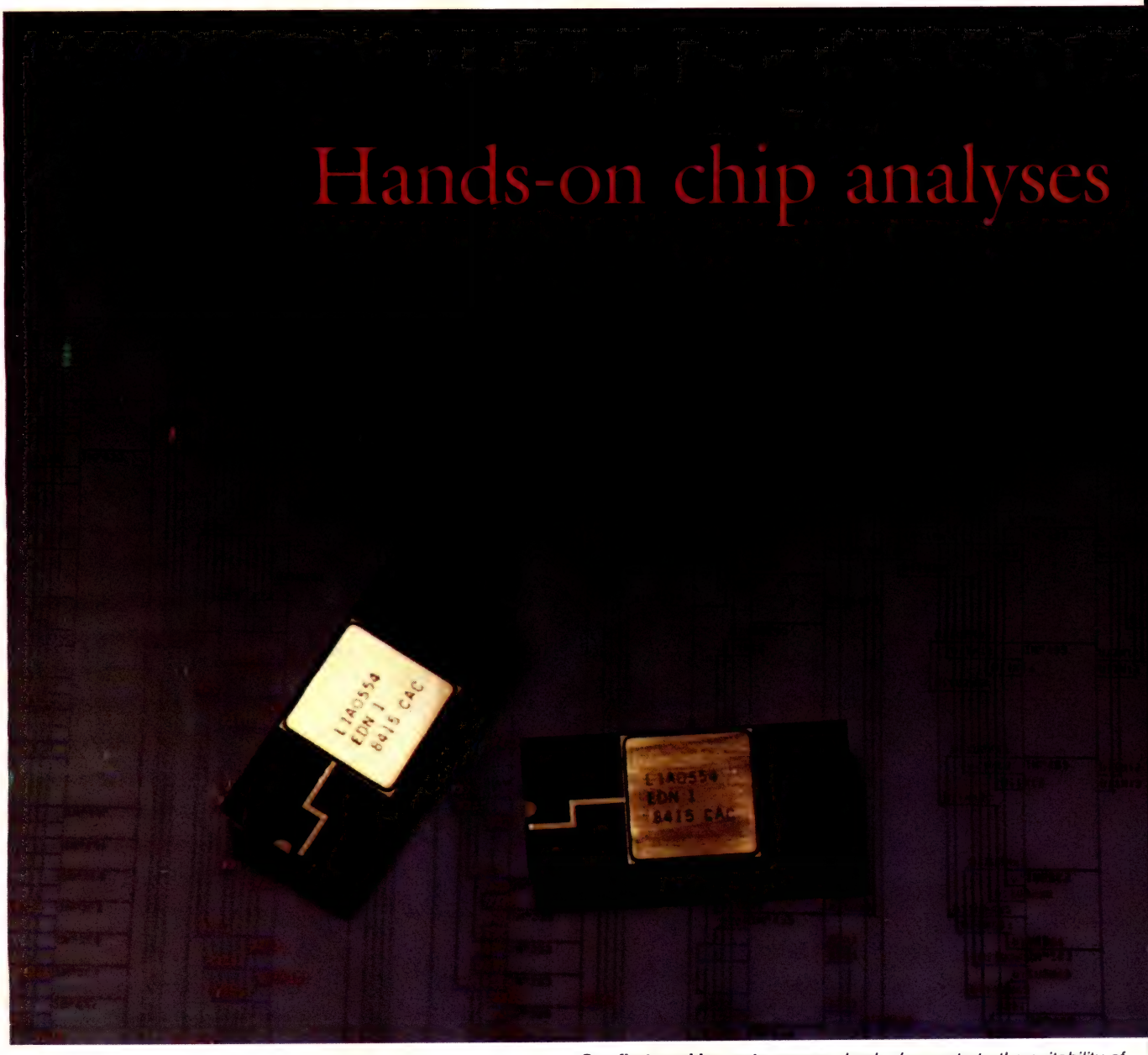
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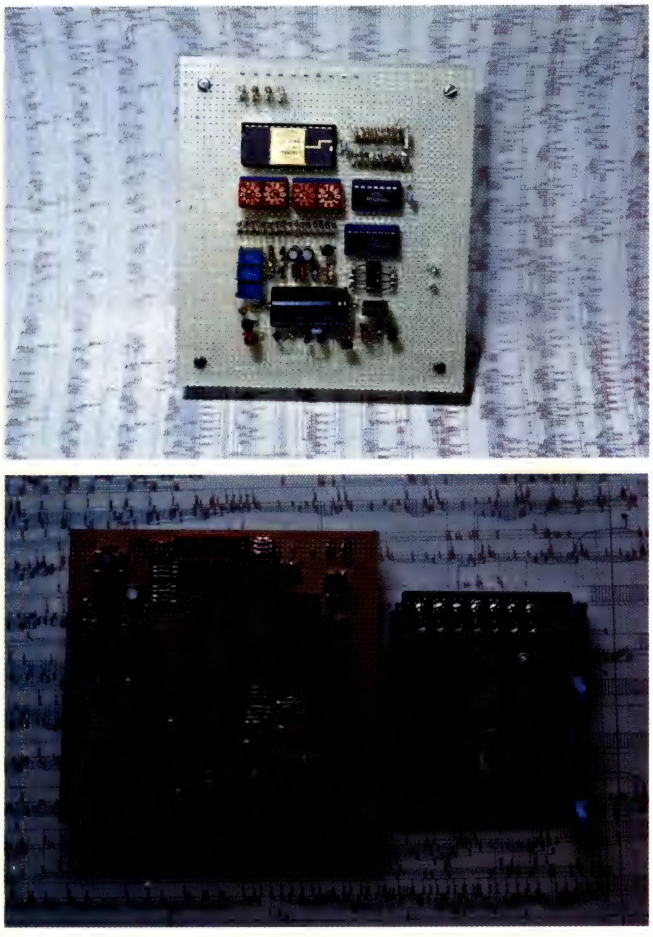
Hands-on chip analyses



Our first working gate arrays *clearly demonstrate the suitability of semicustom-IC technology to our sample system. Analysis of the chips' performance and economy proves that even trade-press editors can design ICs with significant advantages over standard components.*

determine project success

In a blazing triumph of editors over technology, EDN's first semicustom ICs actually work. Performance and cost analyses prove that gate arrays easily satisfy our design objectives.



A prototype of our semicustom-IC-based system (top) *occupies only one-fourth the space of our standard-IC-based system* ***(bottom).*** *In addition, it provides added functionality and costs roughly $60 less to construct. Note that our system's semicustom-IC-based version incorporates only three ICs.*

Andy Rappaport, *Special Projects Editor*

After nearly nine months of planning, intermittent design work, writing and waiting, we have finally received our first gate arrays. These gate arrays not only meet our initial design specifications, but their performance and economy clearly demonstrate the benefits that well-conceived semicustom-IC use can bring to electronic systems. Indeed, chip tests and system-cost analyses indicate that our first gate array meets our design goals with resounding success.

Our first gate arrays were shipped to us by LSI Logic. Of the three chip vendors involved in this design series, LSI Logic was the first to receive design data sufficiently detailed to allow chip production. In addition, of the three series participants, LSI Logic currently employs the most mature automated tools for design transmission, layout and test design. Therefore, the firm was able to meet its promise to deliver prototypes eight weeks following our approval of layout results. With the other two vendors, American Microsystems Inc and International Microelectronic Products, we used new and largely untested design transmission and conversion software. Therefore, debugging and experimentation time has extended the delivery times of chips from those two vendors.

Most important, the chips we're expecting from IMP are based on standard-cell technology—technology that currently results in added layout and fabrication time compared to gate arrays. IMP promises prototype delivery within 12 to 14 weeks of design receipt and thus adds four to six weeks to average gate-array delivery times. We're especially anxious to analyze the

performance and cost benefits of our standard-cell-based chips in light of the ICs' extended prototyping cycles.

The moment of truth

Upon completing our prototype gate arrays, LSI Logic sent us 25 tested parts. That firm's production-floor tests using patterns based on our simulation runs confirmed that these 25 arrays performed the functions we requested. Our goal in analyzing the devices centered on determining whether the functions we asked for accurately reflected our actual system requirements. To gauge such correspondence, we tested our chips in the working environment they would encounter in actual use.

The arrays' 8-week prototyping cycle gave us plenty of time to construct a wire-wrapped prototype board representative of our sample application's complete system. In addition to the gate array and a few passive and discrete components, our system now includes only a CD4011 quad CMOS NAND gate used for clock generation and an XR2206 function generator that performs our system's analog functions. Thus, prototype construction was a simple and rapid task.

The most time-consuming aspect of our prototype-development efforts involved the construction of a programmer used to exercise roughly half of our chip's function. We developed the specifications for this programmer as we designed and simulated our semicustom chip, but had given no thought to its construction until submitting our semicustom-IC designs for layout and fabrication. Compared to our 3-chip semicustom-IC-based system, our 15-chip programmer represented a sizable design and prototyping challenge, especially in light of our lack of CAE tools for that system-development step. Indeed, were our programming circuit destined for production of more than a few units, we'd consider designing a second semicustom chip to reduce complexity and enhance portability.

By using our waiting time to construct a prototype system, we prepared ourselves to test our gate arrays immediately upon receiving them. Our first tests uncovered a few errors in our prototype board's wiring—a few pull-up resistors instead of pull-downs, for example—but, on the whole, our gate arrays behaved predictably. We noticed that our chip's first gate-array version wakes up in an active test state, but soon settles into a predictable quiescent condition. Initial conditions are hard to predict through simulation and depend somewhat on logic-cell and -macro design. We'll be curious to observe how the other two versions of our design begin their operation. In any event, our chip's short self-initialization cycle entails no adverse system-performance consequences.

Exhaustive in-circuit chip tests yielded remarkable results. In all ways, our gate arrays behaved consistently and predictably. All major chip functions worked exactly as desired. Our only disappointment stems from a single unintentionally inverted input line. We should have caught and corrected this misplaced inversion during design and simulation steps, but it somehow managed to escape our scrupulous investigations. As a result of this line's active-Low rather than active-High operation, we were forced to borrow an inverter from our circuit's clock oscillator in order to restore normal system function. Were our system destined for production, we'd have corrected our design database immediately to ensure proper operation of production circuits.

According to most semicustom-IC application engineers, our unintentional signal inversion is typical of the types of errors discovered in prototype arrays. Our simulations, like those of most designers, centered on verifying the performance of large, complex internal chip functions; it dealt only briefly with I/O functions. The misplaced inverter, therefore, easily escaped our observation.

Simulations of I/O behavior are further complicated by a lack of tools aimed at integrating chip simulations into overall system analyses. The improperly inverted signal in our design is fed by a diode decoder wired to two of our chip's output pins. During chip simulations, we used software to assign values to this input signal, but we didn't set up a system simulation designed to analyze the operation of our external decoder. To do so, we could have used our chip as an element in a larger system simulation, a simulation that would have uncovered our design error immediately. Such simulations are now possible—although time consuming—using most CAE workstations, but impossible using most semicustom-IC vendors' proprietary design systems. In our next chip-design project, we'll anticipate these simulation difficulties by using a functional simulator to quickly establish specifications for I/O-signal polarity and external-circuit operation.

No way to use production vectors

Our in-system tests verified the operation of our design but couldn't check our chips as exhaustively as did our production-test programs. Our production vectors, executed using ATE, result in comprehensive chip tests in far less than 1 sec. By contrast, similarly exhaustive tests using our prototyping board and programmer take more than 1 hr, including both chip-operation and manual test-setup time. As a result, we relied heavily on LSI Logic's tests of our chips to ensure overall chip consistency. We used our tests primarily to verify the correctness of our basic design, to check the operation of all chip functions, and to

characterize such chip parameters as I/O capability and power dissipation.

In our design, the most interesting chip parameters are those relating to power dissipation. Our circuit's 32.768-kHz master clock results in no critical system-speed parameters, and none of our system's input signals involve timing characteristics sufficiently complex to demand detailed examination of our chip's I/O speed. In addition, none of our circuit's I/O characteristics stress our gate array's input or output capabilities. Most of our system's interface signals operate at CMOS current levels and involve no significant threshold sensitivity. The most critical interface signal requires our chip to sink 0.5 mA during active cycles, a current level well within the 3.2-mA capability of the output buffers selected for our LSI Logic gate arrays.

Power dissipation, however, is critical in our design. Because it must be capable of operating from standby-battery power for extended periods of time, our system must consume only minimal power. Therefore, we made extensive power-supply comparisons between our gate-array-based system and our original standard-component prototype.

Our standard-component system consumes nearly 1W during quiescent periods and dissipates slightly more than 1W during active cycles. Most of the design's current requirements stem from our use of LM555 and LM556 timer chips to control long-interval system timing. Together, our circuit's timers draw 50 mA at 12V, resulting in power requirements of nearly 600 mW. We could have designed our system for minimal current drain by replacing the bipolar timing circuits with CMOS counters, but that scheme would have significantly increased our system's IC count. Instead, in our standard-component system, we minimized standby power dissipation by using an elaborate power-switching system that kept only real-time clock circuits alive during low-battery intervals.

Our semicustom-chip-based system, on the other hand, draws only 13 mA at 12V, most of which is required by our XR2206 oscillator. The gate array itself requires 665 μA during quiescent periods and 1.6 mA during active cycles. Almost all of this chip current is required by I/O drivers; our calculation indicates that the chip's core, which includes 1200 active gates, dissipates less than 80 μW. These calculations are based on a specified consumption of 20 μW/MHz per active gate, a clock frequency of approximately 0.03 MHz and assumptions that, on average, only 10% of all gates toggle during each clock cycle.

Thanks largely to our semicustom chip's CMOS operation and our 3-chip system's elimination of several power-hungry signal decoders and multiplexers, our gate-array-based circuit requires less than 20% as much power as our original system. Therefore, without elaborate power-switching schemes, the new system extends standby-battery capability five times.

Although significant in our application, the power savings offered by our semicustom chip pale in comparison to the cost saving it provides. Our initial design

Softening our views

Receiving our first working gate arrays has altered our previously clinical view of semicustom ICs. Until now in this design series, we consciously avoided becoming overwhelmed by the gee-whiz aspects of IC design. Semicustom-ICs have been touted by vendors and the media as panaceas—solutions to problems ranging from escalating system complexity to US industry's problems competing in world technology markets. To us, however, semicustom ICs were primarily an addition to engineers' toolboxes. In our evaluations of the IC-design process, we focused almost exclusively on the extent to which semicustom ICs deliver on their promises, not on intellectual and emotional appeal.

Those views changed when our first tests began to indicate that our design work over the past nine months has actually led to the production of ICs meeting our functional and performance specifications. As our gate arrays began to show signs of life, our coldly rational analyses became colored by a feeling of design freedom. As seasoned system designers long held captive by the tyranny of standard-IC vendors, we now fully appreciate the power of do-it-yourself chip design.

Indeed, as we continued to probe our gate array, we thought little about the suitability of our first chip to its intended application. Instead, we thought back on past designs that could have benefited from semicustom-IC technology and, more important, ahead to all of the systems that we can now build practically and economically. Our enthusiasm was only heightened by the cost and development-time analyses summarized throughout this article.

Thus, having successfully harnessed the potential of semicustom silicon, we feel that our efforts have been educational in several respects. Not only have we learned how to use semicustom-IC and CAE technologies, but we have learned why to use them as well.

CMOS gate arrays reduce power needs by 20%

STANDARD COMPONENT VERSION		
COMPONENT	**IC COST**	**INSERTED COST**
12 x CD40XX	$ 6.00	$30.00
2 x LM556	0.50	5.00
LM555	0.25	2.25
ICM72023	4.00	6.00
XR2206	3.00	5.00
TOTAL	**$13.75**	**$48.25**

SEMICUSTOM-IC VERSION		
COMPONENT	**IC COST**	**INSERTED COST**
GATE ARRAY	$13.20	$15.20
XR2206	3.00	5.00
CD4011	0.50	2.50
TOTAL	**$16.70**	**$22.70**

Fig 1—Based on digital-IC purchase costs alone, *our gate array provides no bargain. But when receiving, stocking and assembly costs are factored in, the gate array saves more than $25.*

objective called for the trimming of 60% from the cost of producing our system's digital circuitry. Analyses of the costs associated with both standard-component and semicustom-chip implementations of our design indicate that we have nearly met this goal and, as a result, have slashed 47% from the production costs of our system's analog/digital main circuit board.

Fig 1 illustrates the comparative costs for our system's active digital circuitry. We computed these costs based on a production run of 10,000 pieces, a volume typical of the yearly production of systems now incorporating gate arrays. According to LSI Logic, our gate arrays, packaged in 28-pin plastic DIPs, would cost $13.20 in 10,000 piece lots. The firm claims that this price would drop to $11.85 in 1985, as it ascended the learning curve, but we elected to base all of our comparisons on the higher 1984 price.

Based on IC-purchase prices alone, our gate array costs slightly more than the sum of all of the digital ICs required to build our system using standard components. However, cost comparisons based only on purchase price are misleading. Most investigations into the true costs of system production yield added costs—costs associated with receipt, test, stocking and insertion—averaging $2 per IC. Adding these costs to our IC-price analyses suggests that our gate array actually reduces our system's digital-IC costs by $25.55, or 53%.

CLASS	STANDARD COMPONENTS				SEMICUSTOM IC			
	QUANT	**NAME**	**INSERTED COST**	**TOTAL COST**	**QUANT**	**NAME**	**INSERTED COST**	**TOTAL COST**
ACTIVE COMPONENTS	12	4000 SERIES CMOS ICs	$2.50		1	GATE ARRAY	$15.20	
					1	XR2206	5.00	
	2	LM556 ICs	2.50		1	CD4011	2.50	
	1	LM555 IC	2.25		4	2N2222 XISTOR	0.75	
	1	ICM7223 IC	6.00		1	LM7812	1.50	
	1	XR2206	5.00					
	5	2N2222 XISTOR	0.75					
	1	LM7812	1.50					
				53.50				27.20
PASSIVE COMPONENTS	41	1N914 DIODES	0.25		21	1N914 DIODES	0.25	
	1	LED	0.50		1	LED	0.50	
	50	1/4-WATT RES	0.25		24	1/4 WATT RES	0.25	
	21	CERAMIC CAP	0.25		5	CERAMIC CAP	0.25	
	5	ELECTROLYTIC	0.35		3	ELECTROLYTIC	0.40	
	4	BCD SWITCHES	2.50		4	BCD SWITCHES	2.50	
	1	CRYSTAL	1.50		1	CRYSTAL	1.50	
	3	TRIMMERS	1.00		3	TRIMMERS	1.00	
	2	20-PIN CONN	1.25		1	8-PIN CONN	0.75	
				47.25				29.45
PACKAGING	1	50-IN² PC BOARD	12.50	12.50	1	13-IN² PC BOARD	3.25	3.25
TOTAL				**113.25**				**59.90**

Fig 2—Passive-component and pc-board costs *are also reduced through semicustom-IC use. Passive-component prices in this estimated system-cost analysis include assembly expenses of $0.20 to $1.*

This cost reduction doesn't quite meet our 60% goal, but it's significant.

In addition, our semicustom IC reduces the number of passive and discrete components our system requires (**Fig 2**). Not only does it eliminate diodes and resistors used for signal decoding and interface functions, but it also eliminates two connectors by communicating serially with an external programmer. Building serial communications into the standard-component version of our system would have added several ICs; as a result, a lowest cost standard-IC implementation employs two 20-pin connectors that accommodate programming signals. Semicustom-chip economy allowed us to build serial communications into our gate-array and standard-cell-based chips, thus reducing the system's programming-pin count to eight and eliminating two costly connectors. Factoring in all of these costs, including overhead costs of $0.20 to $1 per passive component, yields additional cost savings of $18.55.

Moreover, our semicustom-IC-based system requires a pc-board area of only 13 $in.^2$ compared with 50 $in.^2$ for our standard-component system. Assuming pc-board costs of $0.25/$in.^2$, then our semicustom-chip saves an additional $9.25. Therefore, gate-array use results in an overall savings of $53.35, or 47%, on the assembled cost of our system's main circuit board. Through careful design and efficient production, we might have reduced the cost of our standard-component-based system, but we doubt that these efforts could come close to matching the cost reductions for our first gate array.

Analyzing system savings

Of course, in our case, a circuit board is not a complete product. Although we saved 47% on our circuit board's cost by employing semicustom logic, we can't hope to realize that level of cost reduction for our entire system. But the overall system cost savings we can expect through gate-array use are significant.

Fig 3a illustrates an overall cost analysis for our sample system. In addition to its main circuit board, our system employs an RF transmitter ($35 in volume), a plug-in 12V transformer ($5) and a sealed, rechargeable 12V battery ($7.50). These costs remain constant regardless of the method we use to construct our main circuit board. Our package costs, however, are reduced through semicustom-IC use. We estimate that the small circuit board required by our semicustom-based system could lead to package-cost savings of $5, further adding to the economy of our semicustom-IC based system. Adding $15 for assembly and test expenses results in an overall cost of $190.75 for a standard-component-based system vs $132.40 for a system employing our gate array. Total savings, therefore, equal $58.35, or 31%.

Our 31% cost savings are sufficiently high to allow us to recoup our development expenses fairly quickly. According to LSI Logic, the development of our gate array would have involved charges of $17,000 for vendor-supplied engineering time, $10,000 for tooling and $4500 for the computer time we used for simulation and testability analysis. Because our prototypes were produced using production-ready tooling, LSI Logic claims that we would incur no additional charges upon committing to full-scale chip production. Total engineering and tooling costs for our design, therefore, equal $31,500.

By saving more than $55 on the cost of each of our systems, we could recoup our direct development expenses after producing only 540 units. Interestingly, we could recoup both chip-development expenses and the cost of the CAE tools we used for chip design after only a few months of production.

Assuming that we spent $100,000 to acquire an engineering workstation with design-entry, simulation, timing-analysis, mass-storage and hard-copy capabilities, and assuming a production rate of 10,000 units per year, we would reach our break-even point of approximately 2250 units after less than three months of production. It appears, therefore, that CAE tools used to design semicustom ICs can pay for themselves through successful implementation of only a single chip. As **Fig 3b** demonstrates, over a production run of

COSTS	STANDARD COMPONENTS	SEMICUSTOM IC
PC BOARD	$113.25	$ 59.90
RF CIRCUITRY	35.00	35.00
PACKAGE	15.00	10.00
TRANSFORMER	5.00	5.00
BATTERY	7.50	7.50
ASSEMBLY/TEST	15.00	15.00
TOTAL COST	190.75	132.40
NET SAVINGS	—	58.35

QUANTITY NEEDED TO JUSTIFY $31,500 DEVELOPMENT COST	540 UNITS
QUANTITY NEEDED TO REPAY $31,500 DEVELOPMENT PLUS $100,000 CAE COST	2254 UNITS

(a)

COST FOR 10,000	**$1,907,500**	**$1,324,000**
IC DEVELOPMENT COST	**—**	**31,500**
TOTAL COST FOR RUN	**1,907,500**	**1,355,500**
NET SAVINGS FOR RUN		**552,000 (29%)**

(b)

Fig 3—An overall system-cost analysis (a) *demonstrates that our gate array reduces our system's cost by more than $58. This saving is sufficiently large to allow us to recoup development expenses after producing only 540 units and to pay for CAE tools after building fewer than 2500 units. A production-run analysis* ***(b)*** *shows that after a 10,000-piece run, our gate array saves us more than $550,000.*

DESIGN STEP	STANDARD COMPONENTS	SEMICUSTOM IC
LOGIC DESIGN	1 WEEK	2 WEEKS
SIMULATION	—	2 WEEKS
TEST ANALYSIS	—	1 WEEK
LIBRARY CONVERSION	—	1 WEEK
RESIMULATION	—	1 WEEK
PROTOTYPING	2 WEEKS	8 WEEKS
DEBUGGING	3 WEEKS	1 WEEK
TOTAL	6 WEEKS	16 WEEKS

Fig 4—Ten weeks were added to our development schedule *by our decision to use a gate array in our system. But the cost savings resulting from semicustom-IC use more than compensate for development delays.*

10,000 systems our semicustom chip yields a total cost savings of more than $550,000, excluding the amortization of our CAE tools, or $450,000 after paying the costs of CAE.

What hidden costs does our semicustom chip involve? Primarily, it entails increased development time. **Fig 4** shows estimated development schedules for two versions of our relatively simple system. Because we had to design our own real-time clock for the semicustom-based system (as opposed to using an off-the-shelf CMOS LSI component), development of our chip's basic logic design took one week longer than the design of an equivalent standard-component-based system.

In addition, we spent approximately two weeks simulating our design and debugging its logic—time we probably wouldn't have invested in a standard-component-based system. But we recouped this simulation time through shortened debugging cycles. Actual debugging of our wire-wrapped prototype board took less than one day. The remaining time allotted to debugging our semicustom-chip-based system was spent testing and characterizing our gate array. In contrast, we estimate that debugging an equivalent system built from standard ICs would take approximately two weeks. In our case, therefore, simulation cost us one week.

Test design also delayed our project by one week. In the design of most standard-component-based systems, test design usually doesn't commence until after logic-design, -prototyping and -debugging cycles. In our case, however, as with all semicustom-chip design projects, test design was tied tightly to design and simulation. The result of up-front testing, however, is that we'll need to spend little time developing routines to test our entire system. The vast majority of our system is tested by our gate-array or standard-cell vendor through production testing of our semicustom chip. Therefore, we consider our week of test development to be time well spent.

The most significant scheduling costs associated with our LSI Logic gate array result from design transmission and prototyping. We spent approximately one week formatting and checking our design using LSI Logic's design tools; we received prototypes approximately eight weeks after we'd turned over our design. This prototyping time compares to approximately one week for a standard-component system and therefore results in a net delay of eight weeks. Some gate-array vendors promise to shrink prototyping times, but eight weeks is about average for cycles without significant rush charges.

In all, development of our gate-array-based circuit added 10 weeks to the development of our system. In light of the cost reductions it affords, however, we believe the array to be worth the wait.

What happens next

Analyses of our first gate arrays not only prove the suitability of semicustom chips to our sample application, but they also prove our ability to master the gate-array design process. We're glad, though, that the chips we've received so far have come to us pretested. Had we received untested chips, or were our prototype-characterization objectives centered on repeating and observing production tests, we would have had considerable difficulty. We don't possess an ATE system similar to those used by IC vendors, and rapidly applying and observing test patterns is beyond the capabilities of our fairly simple logic-analysis equipment. Therefore, the extent to which we could exhaustively analyze our 25 prototypes is severely limited.

In the next and final installment of this chip-design series, we'll report on the characteristics of our remaining two chip versions and discuss measures and test-systems needed to characterize untested semicustom ICs without the aid of million-dollar ATE setups. **EDN**

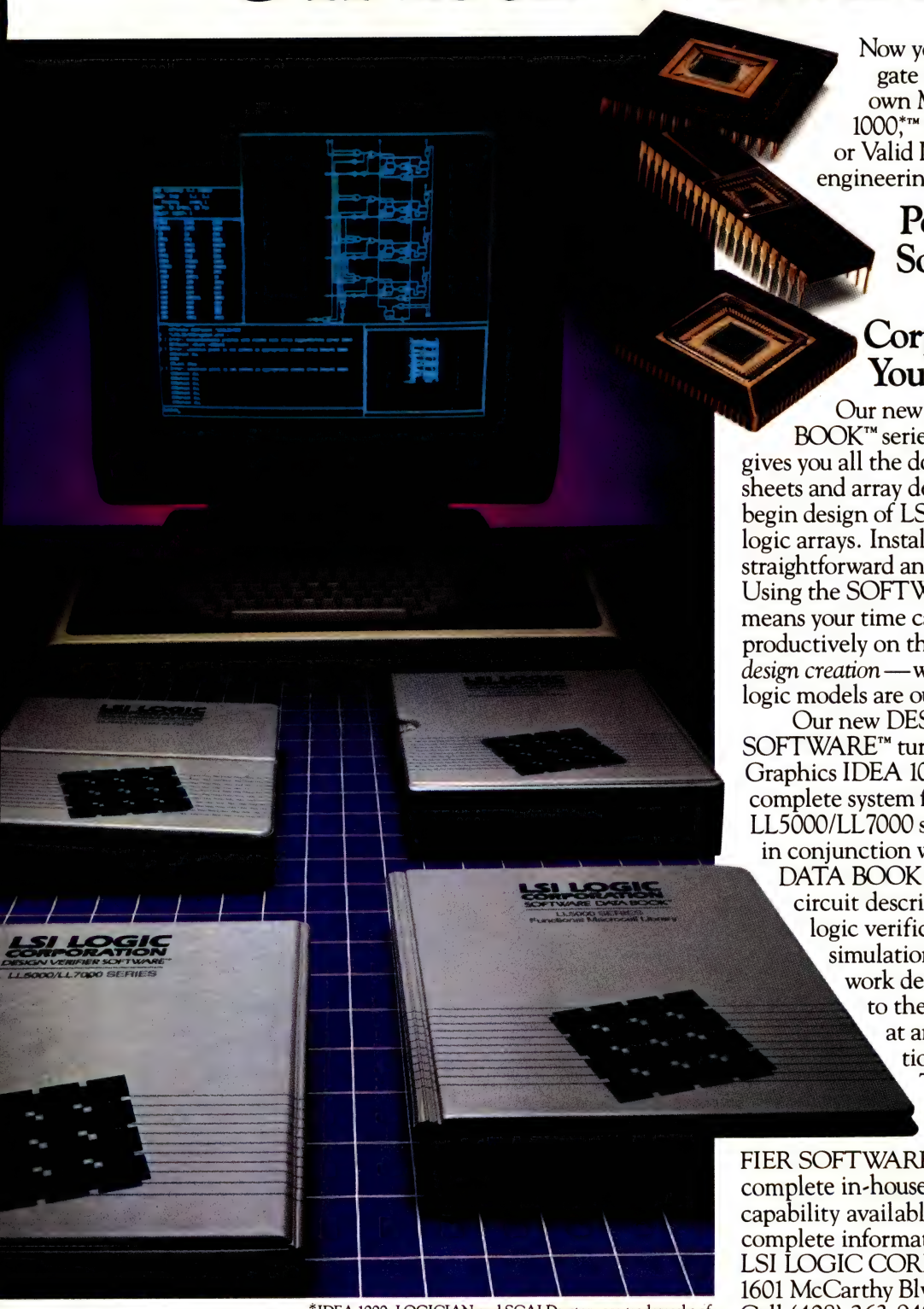
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GaAs logic characteristics result in integration problems

The high speeds of gallium-arsenide logic devices create a new set of design constraints and challenges that occur from circuit conception and board layout through testing.

Jeff Haight, *GigaBit Logic*

In the first two articles in this series (**Refs 1** and **2**), you learned about various gallium-arsenide technologies, their applications potential and the implications and variables in high-speed design. This final article discusses actual design considerations, the interface to other logic families and the tradeoffs associated with the resulting architecture.

In the late '60s and early '70s, TTL emerged as the standard logic family. As technology improved and new logic types such as AS, ALS and more recently high-speed CMOS became available, they remained compatible with TTL. For very-high-performance designs, ECL has maintained its supremacy, and its new families are compatible with older ones. Gallium-arsenide circuits interface with little difficulty to both TTL and ECL.

Many GaAs designs appear in systems that previously used ECL. Furthermore, GaAs performance might motivate retrofits such as speeding front ends and critical paths. This allows you to increase system clock

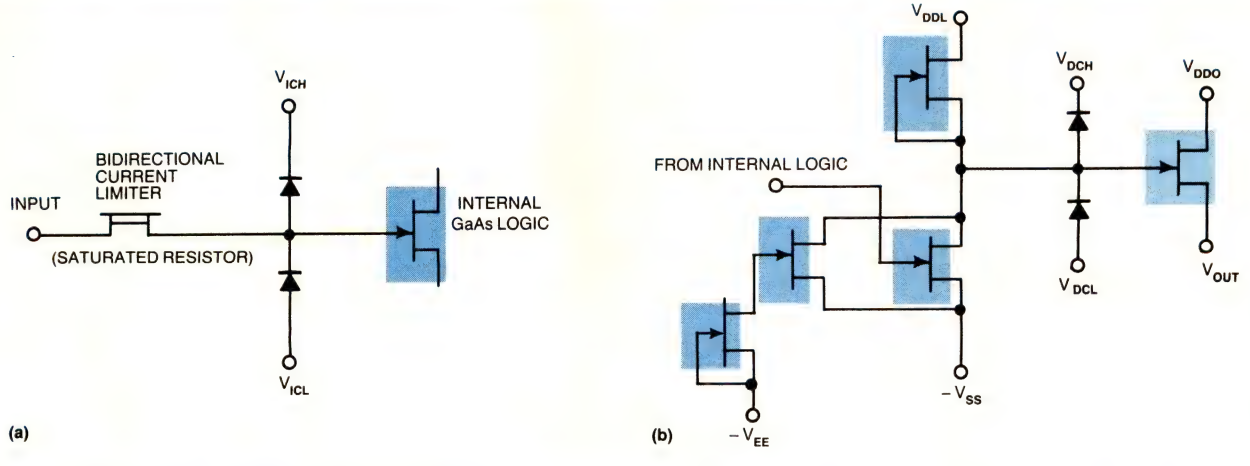


Fig 1—GaAs logic input and output circuits *play a large role in device interfacing. Clamping voltages V_{DCH} and V_{DCL} can enhance performance, and their values depend on the values of R_{LOAD} and V_{TT} in the* **table.**

rates with minimal impact on multilayer pc artwork, final test, logistics and other system aspects.

Although most GaAs digital ICs have ECL-compatible input and output voltage levels, differences do exist. Current GaAs production technology, specifically depletion-mode MESFETs, requires two supply voltages. For ECL compatibility, they require $V_{SS}=-3.5V$ with $-5.2V$ V_{EE} for the supply. Because internal current sources power internal logic, V_{EE} can vary widely without greatly impacting performance. V_{SS}, however, acts as a logic-switching threshold for this internal logic, so you must control it carefully to maintain noise immunity.

It's easier to understand the interface characteristics and performance of GaAs ICs if you examine a block of input and output circuitry (**Fig 1**). In front-end designs, device inputs often resemble sine waves rather than the desired digital square waves. Furthermore, peak-to-peak values can substantially exceed normal ECL values because of standing waves. Even valid ECL levels can have slower than optimal rise times.

To extract maximum switching speeds in GaAs logic, you can use input clamps to reduce effective rise times and optimize levels. This reduces stored charges and minimizes the required internal voltage swing without sacrificing noise immunity. For this purpose, use V_{ICH} (voltage input clamp high) and V_{ICL} (voltage input clamp low). In a typical ECL system where $V_{EE}=-5.2V$, these clamps have a nominal value of $-1.3V$. But these clamp voltages are optional, and GaAs performance exceeds ECL's even without clamps; the performance improvement they bring depends on the input waveform's condition. If you don't need maximum performance, you can connect V_{ICH} to V_{DDL} and tie V_{ICL} to V_{SS} and still protect the device from static discharge without affecting input waveforms.

GaAs logic often uses a saturated resistor in its input structure. This resistor, a GaAs FET connected in series, limits input current to 15 mA. (Actual input impedance is a function of frequency. At dc, it's approximately 5 kΩ, falling to roughly 600Ω at 1 GHz, where gate capacitance begins to dominate.) Following the resistor are clamping diodes that switch at roughly 1 THz (1000 GHz). Because the diodes have a very low On resistance, an electrostatic discharge (ESD) on the input results in a much lower field across the subsequent gate than for MOS devices. This effect reduces susceptibility to punchthrough, the most common cause of static-induced failures. The safety procedures for handling and installing MOS devices are also recommended for GaAs, but actual susceptibility of installed devices to ESD damage is minimal.

The output circuitry of GaAs devices must take the input requirements of other logic families into account. In ECL, for instance, performance deteriorates if inputs are overdriven. Most ECL gates require that input voltages don't exceed approximately $-0.5V$ to guarantee that their input transistors aren't driven into saturation. For this reason GaAs devices often provide V_{DCH} and V_{DCL} pins (output driver clamp high and low, respectively) to limit output voltage swings.

Remember that in this discussion the driven gate's input voltage swings are a primary concern, so if lines are lossy, you can compensate by increasing output swings somewhat. On the other hand, if ringing becomes excessive at the subsequent input, reducing output swings might help. Again you have the option of using V_{DCH} and V_{DCL} for maximum performance. Their optimal value, as shown in the nearby **table,** depends on the terminating voltage (V_{TT}) as well as the line's characteristic impedance and terminating resistor value.

V_{DCL}

TERMINATION VOLTAGE (V_{TT})	LOAD RESISTOR (R_{LOAD}, Ω) 25	37.5	50	75	100
−2.0	−1.53V	−1.62V	−1.67V	−1.73V	−1.76V
−3.5	NR	−0.88V	−1.03V	−1.21V	−1.31V
−5.2	NR	NR	NR	−0.88V	−1.03V

V_{DCH}

TERMINATION VOLTAGE (V_{TT})	LOAD RESISTOR (R_{LOAD}, Ω) 25	37.5	50	75	100
−2.0	−1.45V	−1.66V	−1.78V	−1.93V	−2.02V
−3.5	NR	−1.19V	−1.38V	−1.60V	−1.73V
−5.2	NR	NR	NR	−1.32V	−1.49V

NOTES: 1. PIN V_{DCHS} PROVIDES A −1.8V SUPPLY AND CAN BE CONNECTED TO PIN V_{DCH} WHEN 50Ω, −2V TERMINATION IS USED.

2. NR = NOT RECOMMENDED. CURRENTS THROUGHOUT THE TERMINATION RESISTOR USING THIS CONFIGURATION EXCEED THE RATINGS OF THE OUTPUT DRIVER.

With some degradation in maximum performance, you can connect V_{DCL} to V_{SS} and tie V_{DCH} to 0V to eliminate two additional voltages. Note, too, that you don't need these output clamps when you feed GaAs outputs to GaAs inputs. As with most ECL parts, GaAs devices provide separate V_{DD} pins for internal logic V_{DDL} and output drivers (V_{DDO}). This separation reduces coupling between internal logic and noise generated on the outputs during switching.

This coupling raises another minor point. Outputs from your board and its internal logic will almost always dc couple these outputs to subsequent inputs. However, 50Ω test-equipment inputs almost always have their shields connected to ground (**Fig 2**). Thus, for easy interfacing to test equipment, reference V_{TT} to ground. Doing so might require shifting V_{ee} and other voltages to make V_{TT} equal to the external ground. The **table** of V_{DCH} and V_{DCL} vs V_{TT} is referenced to V_{EE} of −5.2V.

Track both temperature and voltage

Another requirement in high-performance ECL systems is temperature tracking. Unlike TTL families, ECL's optimal input voltage levels and resultant voltage output levels shift as a function of temperature and vary among different ECL families. Unmodified GaAs devices suffer less input and output voltage shifts than ECL, so thermal gradients on a board or in a system don't reduce noise immunity in GaAs as much as in ECL systems.

To optimize noise immunity on a board with mixed logic families, all circuits must track both input and output voltage levels. For instance, if a temperature rise of 30°C raises V_{OL} 0.1V, you'd like V_{OH} to increase by the same amount. Ideally, V_{IL} and V_{IH} will increase by the same amount. Many GaAs devices provide a V_{TRIM} pin that can match GaAs temperature/voltage shifts with any ECL family when you add the circuit in **Fig 3**, which consists of a GaAs inverter, an ECL inverter and an op amp. Inverter voltages shift as a function of temperature and logic input and output levels. The appropriately scaled V_{TRIM} forces the GaAs logic to accurately track the ECL maintaining maximum noise immunity.

Another design consideration arises when you want to drive TTL with high-speed GaAs gates. For instance, a multistage counter might accept gigahertz frequencies and deliver output frequencies low enough for TTL or even CMOS. In this way you could construct high-speed frequency counters without sacrificing the low power, low parts count and cost advantages of available CMOS parts.

This interface problem isn't difficult to solve. In fact, you can use SSI gates as level shifters (for example, ECL to TTL) and create a design that operates faster than available silicon devices (**Fig 4**). Because the voltage swing is greater for TTL and CMOS, these circuits tolerate more ringing than does GaAs. If the lines are long and noise is a problem, reduce line impedance to construct a more correctly terminated line.

Another challenge that surfaces with the advent of GaAs logic is testing to determine actual device per-

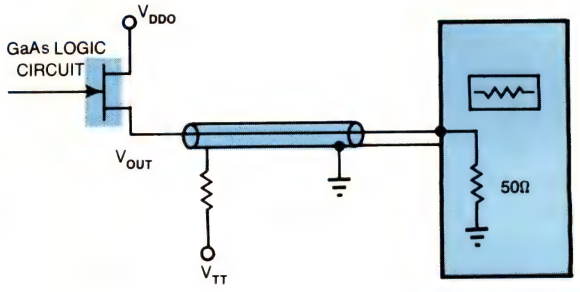


Fig 2—When interfacing GaAs logic to 50Ω test equipment *reference V_{TT} to ground; this might require shifting V_{EE} and other voltages to make V_{TT} equal to the external ground.*

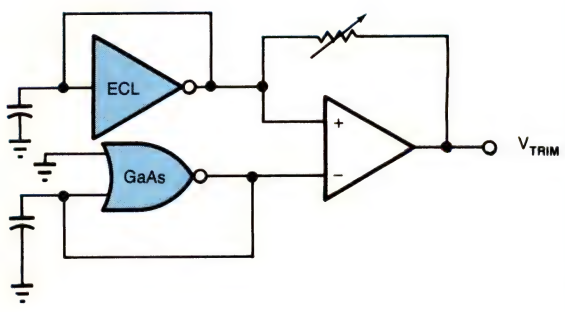


Fig 3—This temperature-tracking circuit *connects to the V_{TRIM} pin of GaAs logic devices so you can match their temperature/voltage shift with ECL families.*

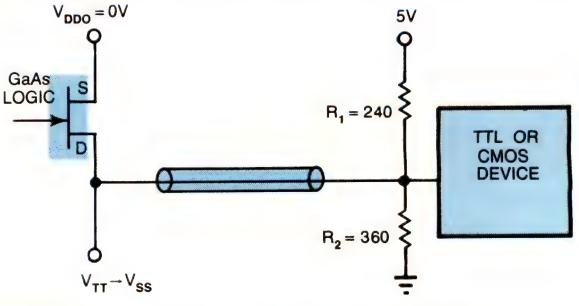


Fig 4—You can drive TTL and CMOS devices with GaAs logic *with this interface, which you can apply with either CMOS or TTL.*

formance. Although some of the following points might seem of peripheral or academic interest to circuit designers, you'll see how they help in understanding the requirements and tradeoffs in the design process.

The initial level of integration in GaAs logic devices may be modest, but their phenomenal speeds and rise times make some ac testing a nontrivial task (for functional and dc tests, vendors can use the equipment they have for silicon circuits). You can avoid significantly degrading device performance and still use inexpensive packaging. Furthermore, many designers will place these die in high-performance hybrids. All these conditions require extensive testing at the wafer level.

First, you can quickly eliminate some parts by measuring device parameters and testing for performance using wafer-ring oscillators. However, you must still perform full functional and extensive parametric testing on the remaining die. As noted, some ac tests require ingenuity and creativity. Standard test probes don't have the transmission-line properties required for performance at several gigahertz (eg, at 4 GHz, excessive stub lengths are actually very short), and the resolution of timing signals is 1 nsec in most available test units. The fastest oscilloscopes have bandwidths of less than 2 GHz, and even at that frequency, outputs are attenuated several decibels.

For obvious reasons, test-equipment makers are anxious to keep current with GaAs developments so they can develop the necessary test units. Meanwhile, you need a great deal of creativity to accurately characterize available GaAs logic devices. For instance, you can do some analysis in the frequency domain where signal generation and accurate spectral analysis at gigahertz frequencies are routine. Furthermore, gating high-frequency signals with slower gates provides one means of assessing delays (**Fig 5**). With such techniques, you need to know exact transmission times, so you need lines with equal lengths or lengths with differences you can exactly determine.

Such factors will affect your design decisions. For instance, this series earlier analyzed different pc-board materials (**Ref 2**). Most nonmilitary designs use stan-

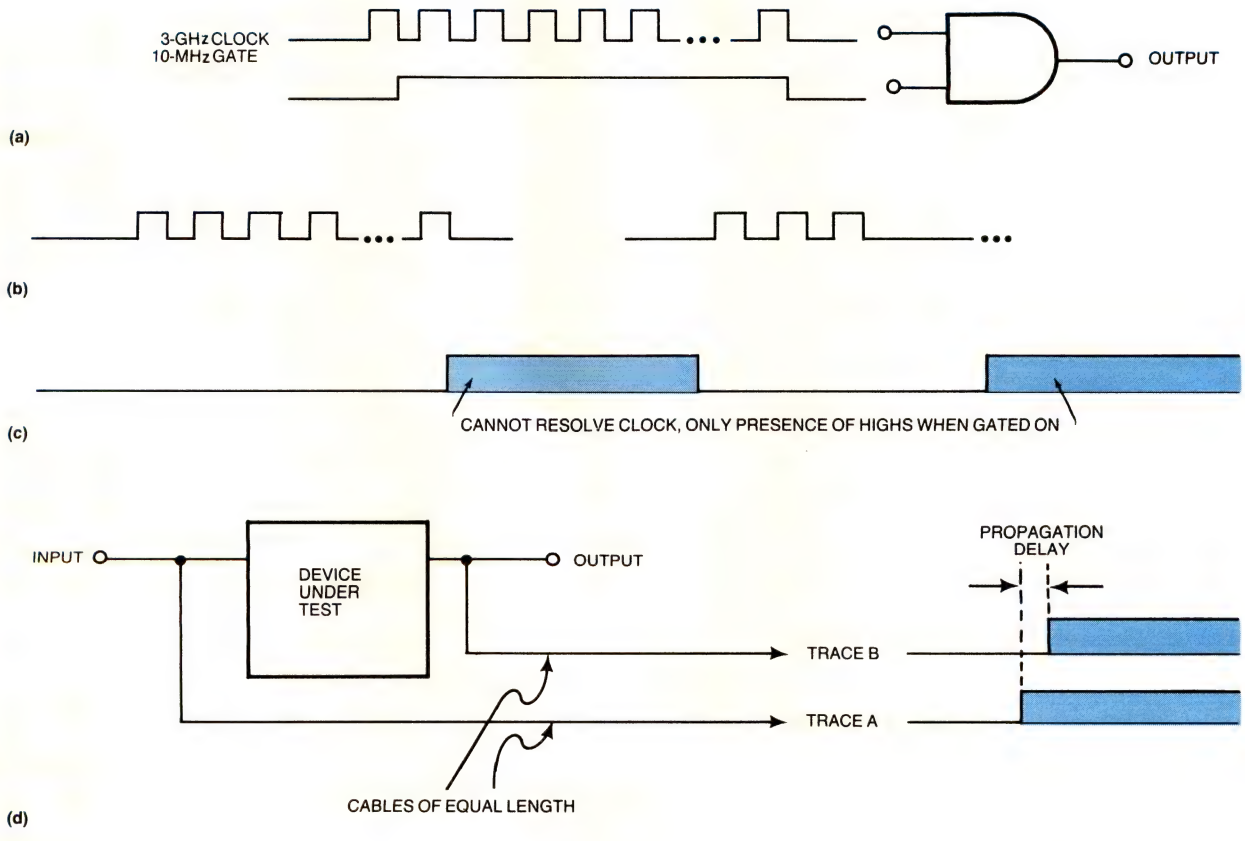


Fig 5—One way to assess high-speed delays *is by gating high-frequency signals with much slower gates* ***(a).*** *Compare the actual output* ***(b)*** *to what you would see on an oscilloscope* ***(c).*** *In* ***(d)*** *you can see a test setup that allows you to determine delays when you know the exact lengths of test leads.*

dard glass epoxy materials such as FR4. Does this fact mean that a small GaAs retrofit is a major undertaking? Not at all. Assuming you continue using glass epoxy, your circuit's signals slow down as a function of the material's dielectric constant, but this shouldn't cause concern if lines are short. Such materials are lossy at higher frequencies, so long lines will act as lowpass filters and attenuate higher harmonics. And although this effect might slow rising edges and reduce the maximum frequency at which devices work reliably, the reduced harmonics slightly reduce the ringing that arises if lines are terminated less than perfectly.

In fact, it's likely that you'll often mismatch terminations to the line's characteristic impedance at both the source and the load. Because the characteristics of glass epoxy vary from batch to batch, line impedance will vary similarly. This variation, although not great, causes ringing. However, lossy lines attenuate ringing further with each reflection. Thus, this lossy behavior isn't always a disadvantage when attenuation isn't so great that you can't realize valid logic levels.

Characteristic impedance varies power

Another question concerns tradeoffs with characteristic impedances. Most high-frequency designs use lines with 50Ω characteristic impedance. Commonly available cables generally use 50Ω SMA connectors. (BNC connectors are also typically 50Ω, but the interface's stub length and suboptimal HF design preclude reliable high-frequency performance.) This impedance plays a role in the power consumption of today's GaAs logic circuits. The near-term level of integration for most of these devices is SSI and MSI, so complex systems require many input and output lines. Also, the lower the value of the characteristic impedance, the lower the value of the terminating resistor and the higher the power consumption. Because most high-performance designs are ECL, typical values are 25 mA for each output (approximately 1.2V across 50Ω when outputs are High and $V_{TT}=-2.0V$). When you add output driver dissipation, you realize that a fair amount of power is consumed.

One way to reduce power consumption is to raise the characteristic impedance by using 75Ω or 93Ω terminations. Besides lowering consumption, however, such impedances make it more difficult to construct controlled-impedance lines within a given tolerance. If the load has a significant capacitive component, it generates ringing at high frequencies. (If the load is inductive, though, performance can actually improve.) Such loads require a balun (balanced-unbalanced transformer) when used with most high-frequency test equipment. However, where a high-impedance test probe proves sufficient on 50Ω lines, it also does the job at higher line impedances. Again, short lines and low performance requirements make your decision easier.

SMD characteristics vary at HF

A factor of more immediate concern in your designs is the behavior of passive components at gigahertz frequencies. With stripline and microstrip circuitry, you'll often use surface-mount components. Therefore, you automatically eliminate concerns about lead inductance for resistors and capacitors. The stated values of such components often vary with frequency and can vary significantly at gigahertz frequencies. Because very high-frequency performance isn't relevant for most designs, catalogs and data sheets don't always contain performance curves for component value variation vs frequency. If these performance curves aren't included,

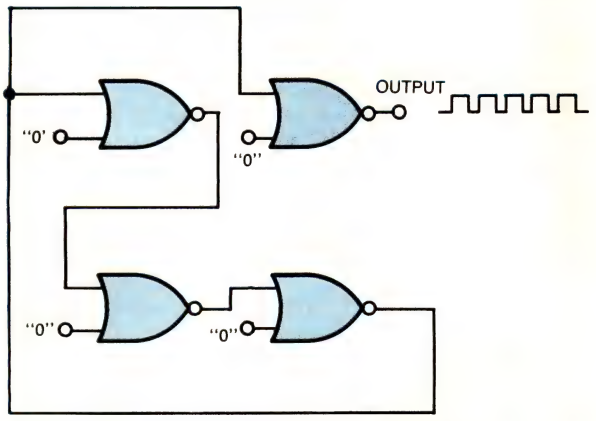


Fig 6—Change the frequency of this ring oscillator, *which consists of three GaAs Nor gates and a GaAs buffer, by varying the lengths of the feedback path.*

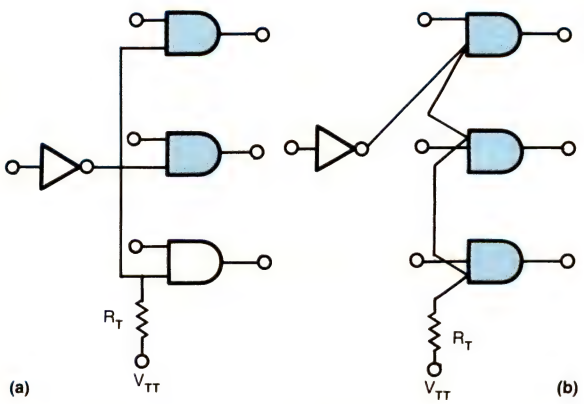


Fig 7—Driving GaAs gates as in (a) *creates false impedances that affect circuit operation. A better method is to distribute one signal to several GaAs gates using the approach in* **(b).**

or if the vendor doesn't make specific guarantees about high-frequency performance, call the factory before placing an order. Remember, it's more difficult to rework a surface-mount multilayer pc board than it is to change a DIP in a socket on a wire-wrap board.

Chip carriers themselves will contain small capacitors in their cavities to minimize inductance and reduce concerns for external bypass requirements at multigigahertz frequencies. However, external bypass capacitors also need good performance in the 500-MHz to 1-GHz range. Furthermore, resistors can take on capacitive values at these frequencies, moving their effec-

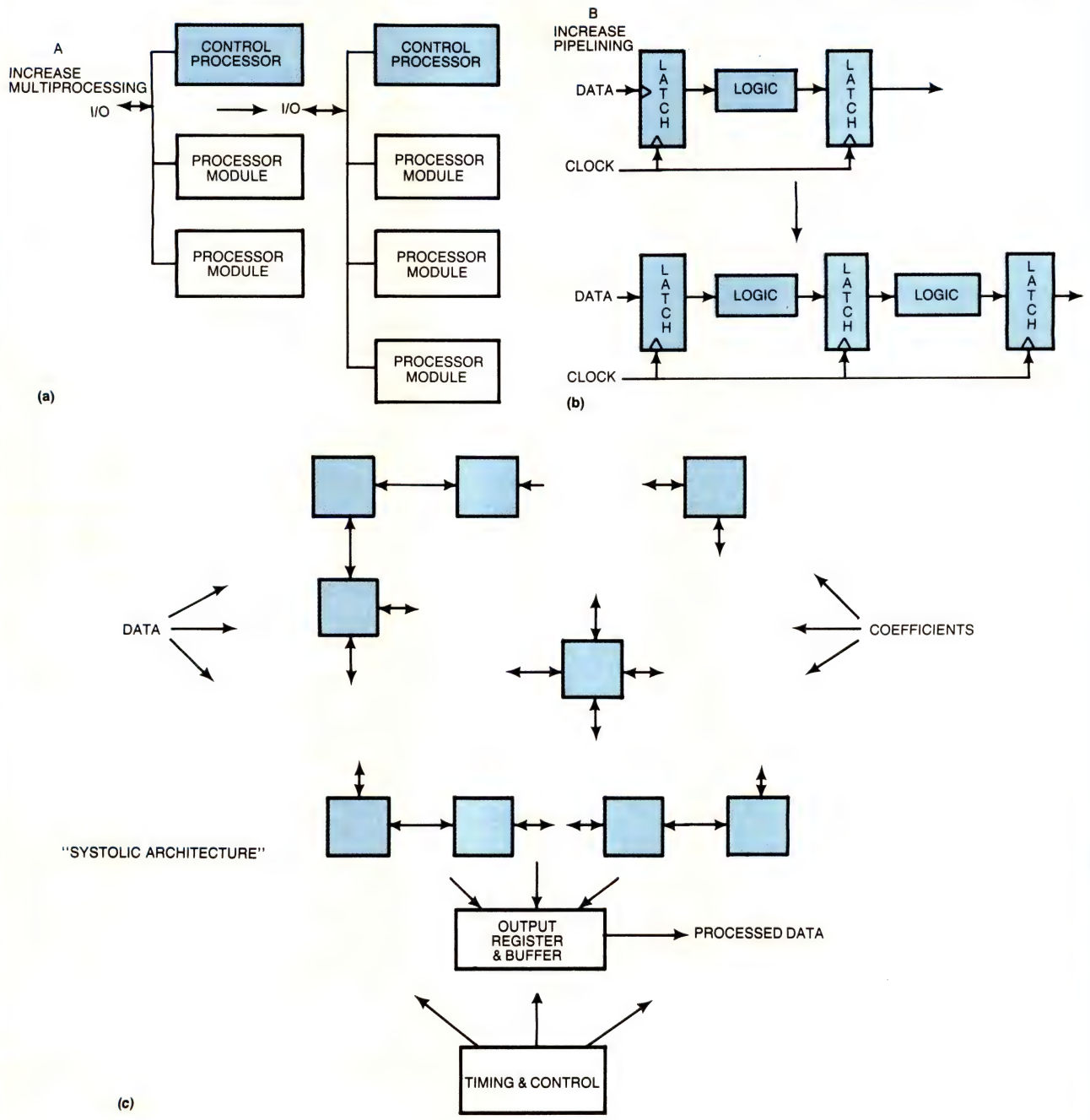


Fig 8—Higher throughput and performance from computers *are leading to new architectures where GaAs logic could play a role. In the multiprocessing system* ***(a)*** *there are many communication paths from the control processors to the slaves. By increasing pipelining* ***(b)****, you can significantly increase the clock rate, a feature well suited for GaAs. In the systolic architecture* ***(c)****, fast setup and hold times with GaAs ease system implementations.*

tive impedance far from the desired 50Ω. Similarly, terminating resistors' capacitive load can slow the rise and fall times of input signals and reduce the circuit's maximum reliable operating frequency. Edge-mount SMA jacks might provide better HF performance than surface-mount jacks because you can reduce the edge-mounts' stub length more easily. As usual, maximum performance with surface-mount SMAs exceeds the best ECL, but edge-mount techniques are preferable to obtain the best performance.

At these frequencies, layout and transmission-line placement become important considerations too. For instance, **Fig 6** shows how changing the length of a feedback path changes a ring oscillator's frequency. With such high frequencies and short propagation delays, it's sometimes practical to adjust frequency with jacks that vary the length of the cable connecting the output to the input. You can also easily provide further control over a narrow range with GaAs diodes. By configuring the diode as a reverse-biased varactor, you can vary the ring oscillator's frequency by varying diode bias and capacitance. In such configurations, frequency changes when you change line lengths or hang devices with nonlinear parameters on signal lines. You should remember this when you place diodes at GaAs logic-device inputs to exploit the diode's speed to further clamp ringing or inputs with unacceptable voltage swings.

Some old design methods won't work

By now you should realize that traditional circuit design techniques aren't universally applicable to gigahertz circuits. Certainly, you should consult one of the many books written about high-frequency design prior to commiting a design to a pc board. Although rigorous paper design and analysis usually save time in the long run, some TTL designers prefer to rough out a design and devote more time to debugging with scope probes and wire-wrap guns than to agonize over timing diagrams while adding delays to account for manufacturers' worst-case specs. This roughing out, however, becomes less and less acceptable as the speed of your circuit increases.

Layout considerations make it difficult to design an easily modifiable prototype. Transmission line length and shape affects cross-coupled noise, losses and rise times. Don't infer, however, that with higher frequencies and rigorous analysis simulations will converge on reality. Even today, good RF designers who work extensively on simulations and analyses of their layouts still revert to beating waveguides with little hammers, bending semirigid coax into bizarre shapes and adding a half turn of wire before their circuits work.

By their very nature, though, digital circuits using GaAs won't require such arcane techniques for debugging. Problems that would preclude acceptable RF analog circuitry are often more than acceptable in digital systems. For instance, running long lines when a signal drives several inputs doesn't present a major problem (**Fig 7**). Bringing the trace close to each package and out to the next package reduces stub length to the distance from the package's edge to the die. Because you need a controlled impedance, you can't run lines directly from one output to several inputs and terminate each because the impedance becomes too low. Similarly, you can't run long lines from one output to several distant inputs and terminate only one because the others act as stubs and generate reflections and ringing. A single oblique line is the only acceptable approach if you want to avoid significantly compromising performance. Further, if a line has multiple impedances along its length, try to place the highest impedance in the middle and place the lower impedances at the source and termination to reduce the malignant effects of ringing.

New architectural possibilities

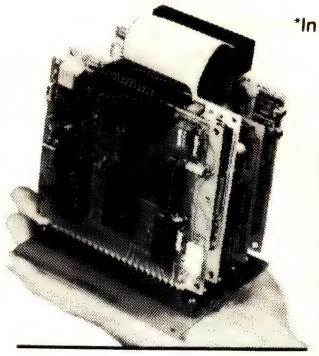
With these design ground rules established, it's worth examining the architectures and possibilities motivated by GaAs logic. Some of the easy and obvious uses or retrofits have already been mentioned, but engineers are also investigating architectures and software for multiple processing. The overhead required to control and communicate between processors limits throughput when running several identical processors in parallel.

Fig 8 sketches multiprocessing and its alternatives for increasing throughput. Multiprocessing, with or without shared memory (**a**), requires a supervisory processor to apportion data and tasks, delegate bus priorities and control communications with the outside world. Pipelining (**b**) reduces the total delay time between clocked stages. Increasing the number of pipelined stages by n delays the flow of processed data by n clock cycles initially, but the clock rate can be raised and the hardware reduced. Finally, systolic arrays (**c**) typically have data flowing through in parallel elements. Coefficients can flow in a different direction or be fixed, and each element transfers information only to its immediate neighbors.

Pipelining often allows an increased clock rate, especially in early GaAs designs. Because the integration level is low, you'll have to deal with a significant number of interconnections. But because the logic is so fast, interdevice communication time requires a high percentage of total system time. Obviously, the fewer the gates and communication delays between latches, the faster the latches can grab new data (setup and hold

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To reduce temperature effects, have mixed logic track one voltage

times for GaAs is roughly 100 psec). Typically, increasing the amount of pipelining increases throughput with only a small penalty in required hardware.

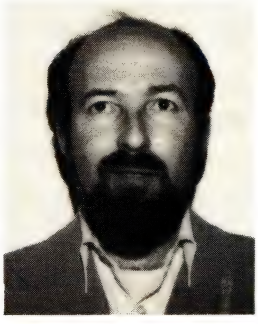
This fact might prove especially useful in systolic architectures undergoing extensive investigation. Many digital signal-processing algorithms and scientific data-processing tasks, such as inverting large matrices, lend themselves to systolic approaches. The major problems currently include partitioning and optimizing array elements to perform the desired algorithm.

Early experiences as well as physics and simulations indicate that GaAs digital devices should withstand 10 times more radiation than silicon devices without failure. Similar studies indicate that GaAs junctions should reliably tolerate much higher temperatures than their silicon counterparts. Certainly, only industry experience with such devices will confirm these and other suspicions. But designers now have a new set of design tools that should allow them to both increase the performance of present designs as well as come up with new concepts. **EDN**

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Author's biography



Jeff Haight is manager of applications engineering at Gigabit Logic (Newbury Park, CA). He previously worked at TRW LSI and Technology Service Corp. Jeff received a BA from the University of Washington in Seattle and also attended the California Institute of Technology in Pasadena. In his spare time he plays tennis and enjoys skiing and bicycling.

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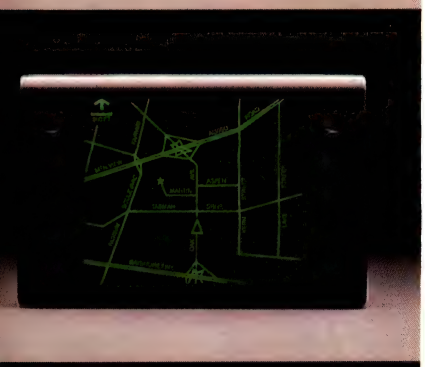
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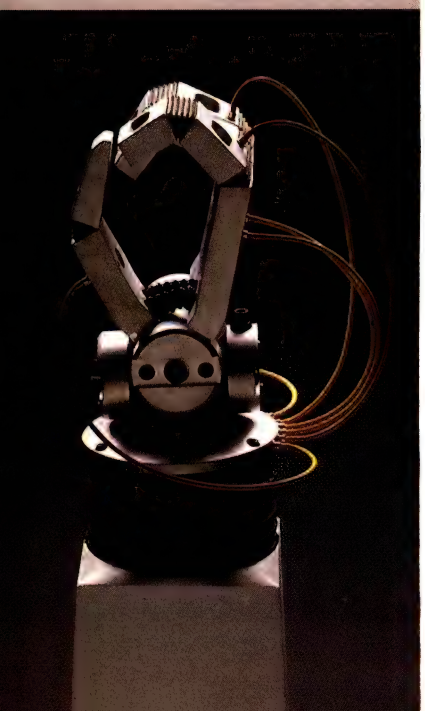
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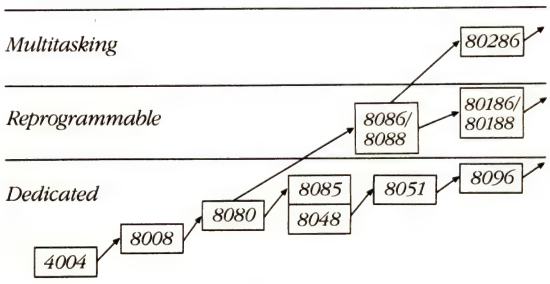
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INTEL MICROPROCESSOR EVOLUTION



This chart shows the genealogy of Intel's microprocessors and how they're tailored for different environments.

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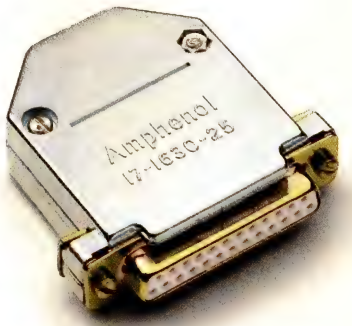
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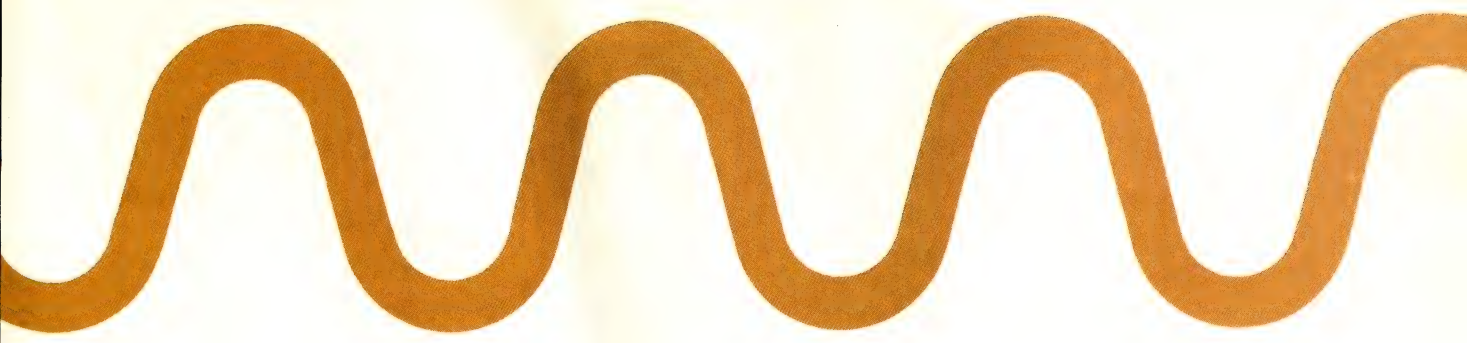
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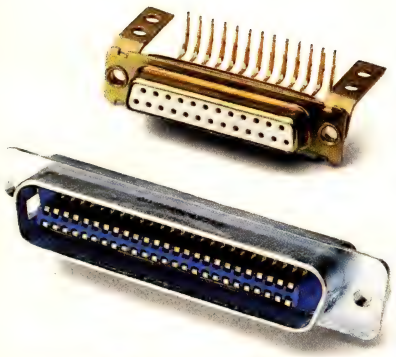


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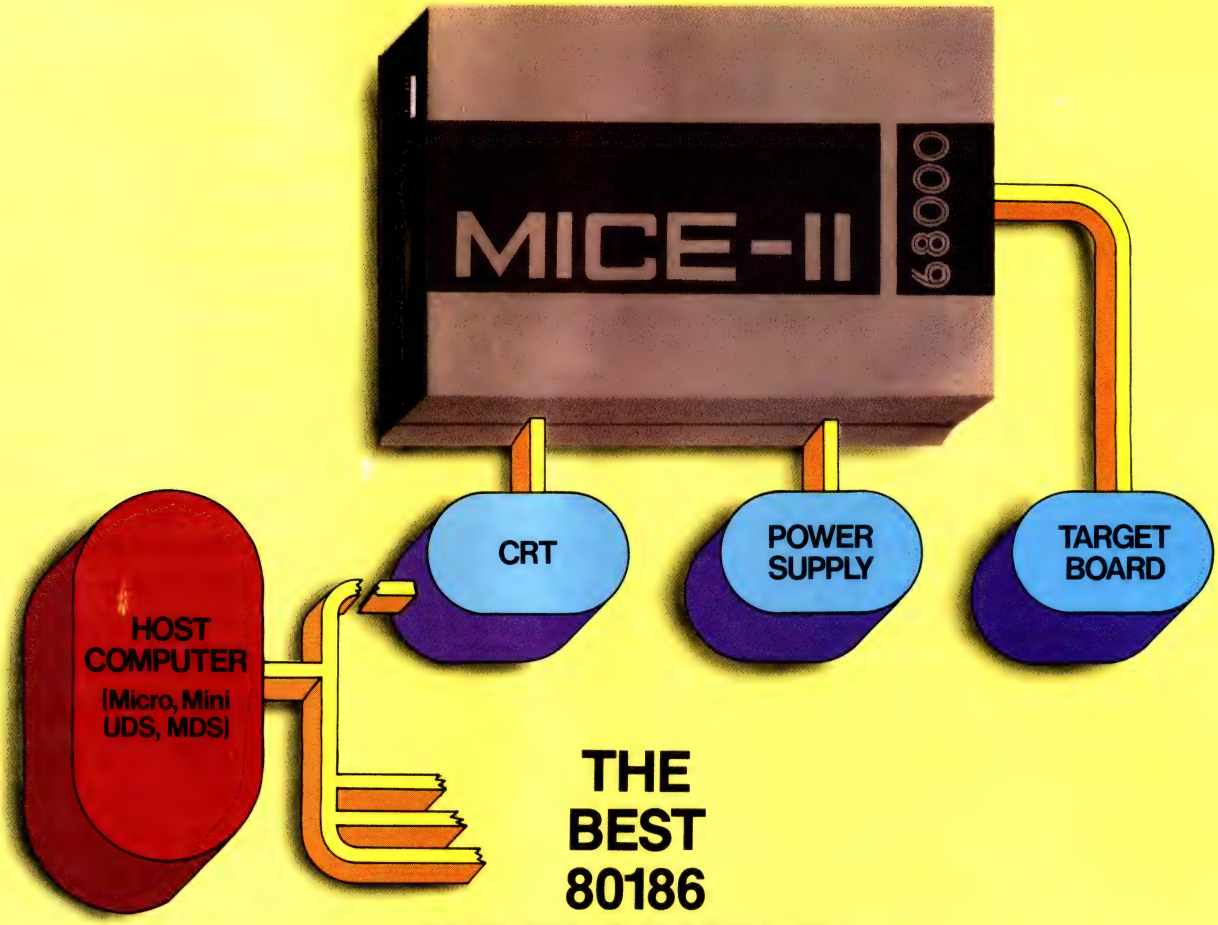
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Take advantage of thermal effects to solve circuit-design problems

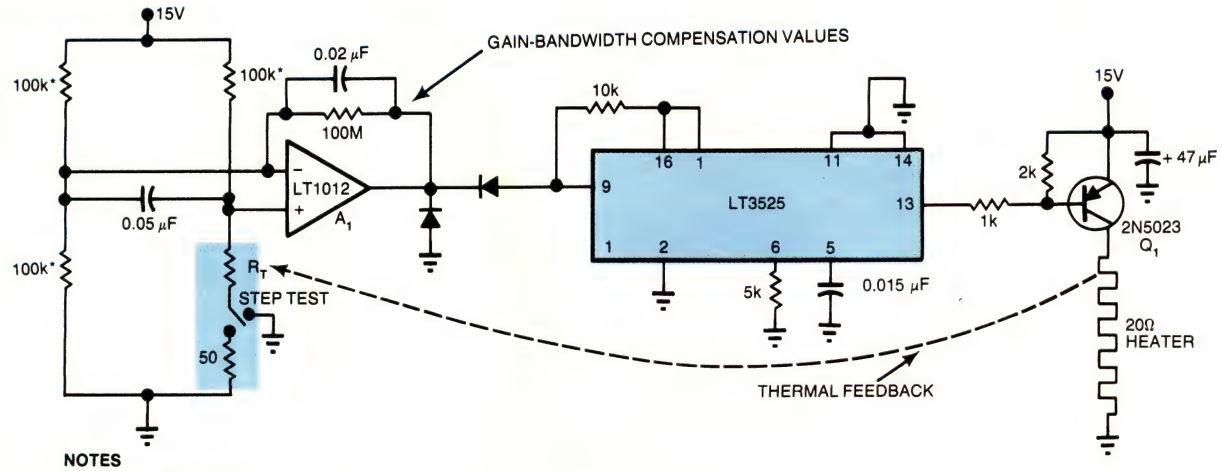
You probably consider thermal effects in circuits your enemy, but they can prove useful in many design situations.

Jim Williams, *Linear Technology Corp*

The direct relationship between temperature and electronic-device failure is the source of more design headaches than any other single consideration. But instead of trying to eliminate or compensate for thermal parasitics in circuits, you can use them to achieve novel solutions to measurement and control problems.

A look at a temperature-control loop illustrates the techniques involved, and familiarity with some of these techniques can help you apply them in less obvious but equally useful ways.

Fig 1 shows a precision temperature controller for a small components' oven. When power is applied to the circuit, the thermistor—a negative-temperature-coefficient device—exhibits a resistance that's high enough to saturate amplifier A_1's output positive. This forces the LT3525 switching regulator's output (pin 13)



NOTES
*TRW MAR-6 RESISTOR
R_T = YSI #44014 (YELLOW SPRINGS INSTRUMENT CO, YELLOW SPRINGS, OH) (R_T = 300k AT 25°C)
ALL DIODES = 1N914

Fig 1—A precision temperature controller for a small oven *makes use of a thermistor's negative temperature coefficient. The 50Ω resistor and switch in series with the thermistor can generate a step input for testing the circuit's response.*

RC networks model a thermal control loop

Low, biasing Q_1 On. As the 20Ω heater warms, the thermistor's resistance decreases, reducing the voltage at A_1's positive input. When that voltage decreases to the inverting input's level, A_1 comes out of saturation, and the LT3525 pulse-width modulates the heater via Q_1, completing a feedback path. Because the heater voltage's modulation rate is much higher than the thermal loop's response, the oven maintains an even, continuous heat flow.

To achieve such high-performance control, you must match A_1's gain-bandwidth product (GBW) to the requirements of thermal-feedback path. Theoretically, achieving this match should be a simple matter using conventional servo-feedback techniques. But practically, the long time constants and thermal delays inherent in thermal systems present a challenge, and thermal-control systems often demonstrate the unfortunate relationship between servo systems and oscillators.

Modeling the thermal loop

A thermal-control loop can be simplistically modeled as a network of resistors representing thermal resistance and capacitors representing thermal capacitance. **Fig 2** models a heater, sensor and heater/sensor interface, each of which has an RC factor that contributes to the lumped delay in a thermal system's ability to respond. To prevent oscillation, A_1's GBW must be limited to account for this delay, although high control performance dictates that A_1's GBW be large. Thus, the delays must be minimized.

The delay associated with the heater itself depends to some extent on the size of the heater, and placing the

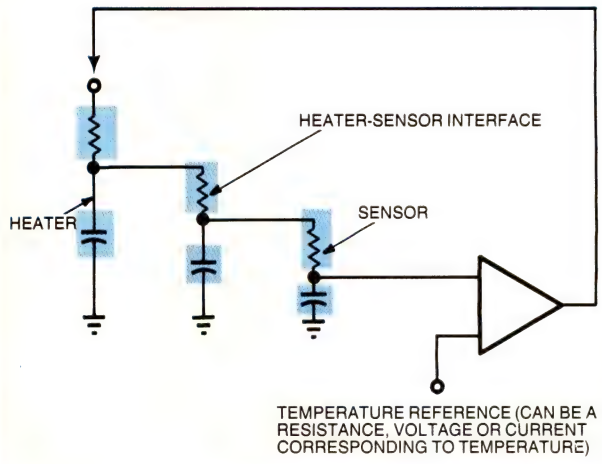


Fig 2—Resistor-capacitor networks can model a heater *and a sensor as well as the heater/sensor interface.*

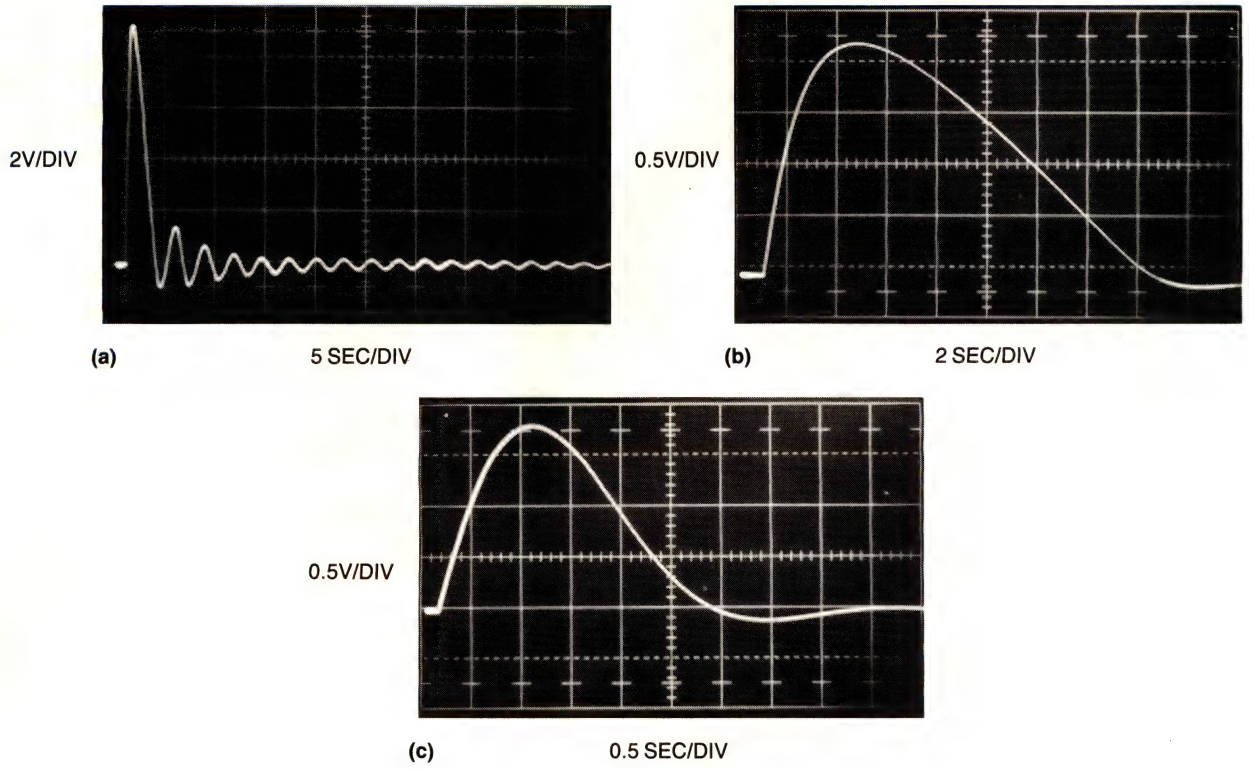


Fig 3—A step input to Fig 1's *circuit can result in underdamped* ***(a)****, overdamped* ***(b)*** *or critically damped* ***(c)*** *responses. The critically damped performance results from the component values shown in* ***Fig 1.***

sensor in intimate contact with the heater reduces the heater-sensor-interface time constant. To minimize the sensor's RC product, you should select a sensor whose size is relatively small compared to the capacity of its thermal environment. Clearly, for an oven with 6-in.-thick aluminum walls, you don't have to use the smallest sensor available. Conversely, for controlling the temperature of a 1/16-in.-thick glass microscope slide, a very small (ie, fast) sensor is in order.

After minimizing thermal time constants, your next step is to choose insulation, which keeps the heat-loss rate down so that the temperature-control system can keep up with the losses. For any given system, increasing the ratio between heater and sensor time constants and the insulation time constants betters performance.

Optimizing the loop

After attending to these thermal considerations, you can optimize the loop's GBW. **Fig 3** shows the effects of different compensation values at A_1. To fine tune the compensation, you can alter the temperature set-point in small steps and observe the loop response at A_1's output. In **Fig 1,** the 50Ω resistor and switch in the bridge's thermistor leg simulate a 0.01°C step.

Fig 3a shows the effects of too much gain bandwidth —the step input forces a damped ringing response that remains at a significant level for more than 50 sec. The ringing eventually dies out making the loop conditionally stable. A further increase in A_1's GBW would result in continuous oscillation. **Fig 3b** illustrates the effect of reducing GBW. Settling time is much faster and more controlled. The waveform is overdamped, indicating that a higher GBW can be achieved without compromising stability.

Fig 3c shows the response for the component values shown in **Fig 1,** and it illustrates a nearly ideal critically damped recovery. Settling occurs within 4 sec. An oven so optimized can easily attenuate external temperature

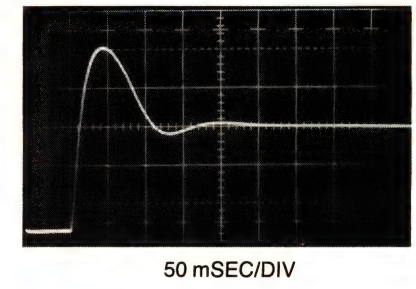


Fig 5—The small die size *of* ***Fig 4****'s transistor array allows a quick, clean response. Settling time in response to a full-scale step input is 250 msec.*

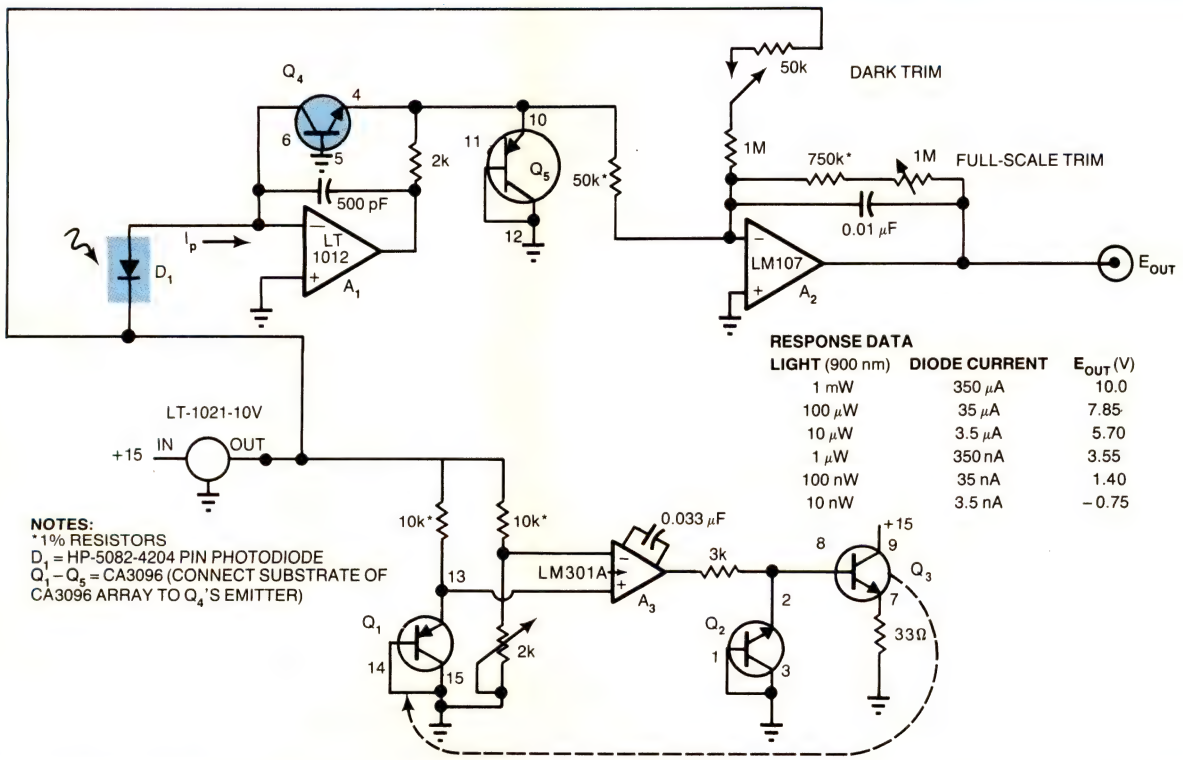


Fig 4—Logarithmic signal conditioning *allows this circuit based on a PIN photodiode to measure light levels over a 100-dB range. The circuit precisely controls the temperature of* Q_4*, the logging transistor.*

Logarithmic amplifiers are temperature sensitive

shifts by a factor of thousands without overshoots or excessive lag.

With this background in the basics of thermal-loop operation, consider some practical applications for temperature control. PIN photodiodes, for example, often serve in photometric circuits. The photodiode in **Fig 4**, for instance, responds linearly to light intensity over a 100-dB range, and digitizing this diode's linearly amplified output would require an A/D converter with 17-bit resolution. Using signal-conditioning circuitry to logarithmically compress the diode's output eliminates this resolution requirement, but it involves using logarithmic amplifiers, which depend on a transistor's V_{BE} vs collector-current relationship.

This characteristic is highly temperature sensitive and often requires special components and layout considerations to achieve good results. Using temperature-control techniques, however, **Fig 4**'s circuit logarithmically signal conditions the photodiode's output and requires no special components or layout.

In **Fig 4**, A_1 and Q_4 convert the diode's photocurrent to a voltage output with a logarithmic transfer function. A_2 provides offset and additional gain. A_3 and its associated components form a temperature-control loop that maintains Q_4 at a constant temperature. (All transistors in this circuit are part of a CA3096 monolithic array.) The 0.033-μF at A_3's compensation pins gives good loop damping if the circuit is built using the array transistors as shown—this configuration achieves optimal temperature control at Q_4, the logging transistor. Because of the array die's small size, response is quick

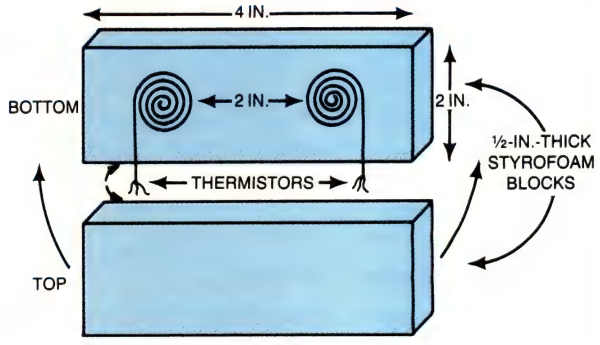
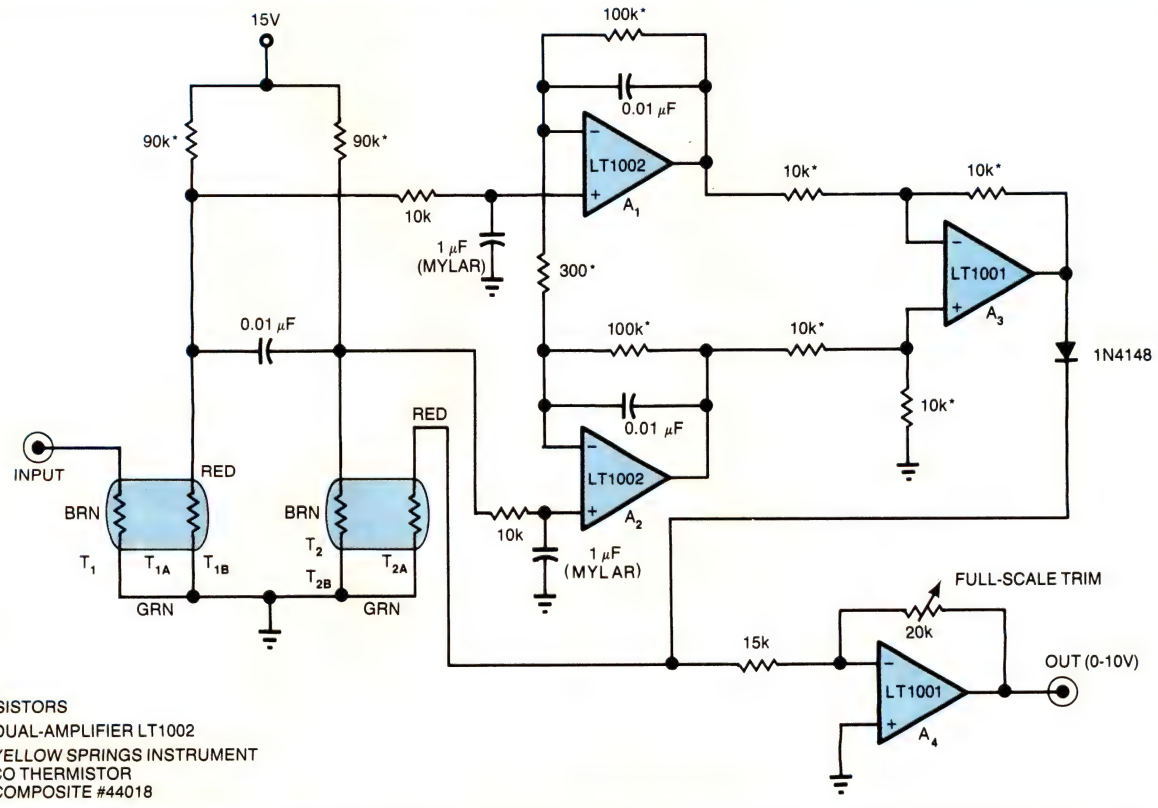


Fig 7—Sandwiching two thermistors *between Styrofoam blocks provides them with an isothermal environment. Coiling the thermistor leads attenuates heat-pipe effects to the outside ambient temperature.*



NOTES:
*1% RESISTORS
A_1, A_2 = DUAL-AMPLIFIER LT1002
T_1, T_2 = YELLOW SPRINGS INSTRUMENT CO THERMISTOR COMPOSITE #44018

Fig 6—Achieving a 50-MHz bandwidth and 2% accuracy, *this circuit measures the dc heating power of an input waveform. Crest factors as high as 100:1 contribute less than 0.1% additional error.*

and clean. Settling time in response to a full-scale step (**Fig 5**) is only 250 msec.

To use this circuit, first set the thermal-control loop by grounding Q_3's base and adjusting the 2-kΩ pot so that A_3's − input voltage is 55 mV higher than its + input voltage. That adjustment places the servo's set point at about 50°C, corresponding to a 25°C rise (2.2 mV/°C×25°C=55 mV) above a 25°C ambient temperature. To complete this first step, remove the ground from Q_3's base and the array will come to temperature.

Next, place the photodiode in a completely dark environment and adjust the 50-kΩ dark-trim pot so that A_2's output is 0V. Finally, either apply or electrically simulate (according to **Fig 4**'s response-data chart) a light level corresponding to 1 mW and adjust the 1-MΩ full-scale-trim pot for a 10V A_2 output. Once adjusted, the circuit responds logarithmically to light inputs from 10 nW to 1 mW with accuracy limited by the diode's 1% error.

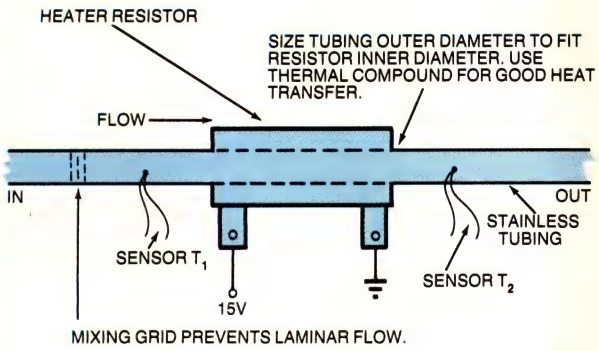


Fig 9—To measure a fluid's flow rate, ***Fig 8****'s circuit depends on a heater to induce a temperature change in the fluid. Sensors on either side of the heater measure the induced change.*

Thermal rms/dc converter

A thermal rms/dc converter demonstrates another application for temperature control. Conversion of ac waveforms to their equivalent dc-power value is usually accomplished by rectifying and averaging or by analog computing methods. Rectification and averaging, however, work only for sinusoidal inputs. Moreover, analog computing methods generally aren't suitable at frequencies above 500 kHz, and crest factors greater than 10 can cause significant reading errors.

Overcoming these drawbacks, **Fig 6**'s circuit

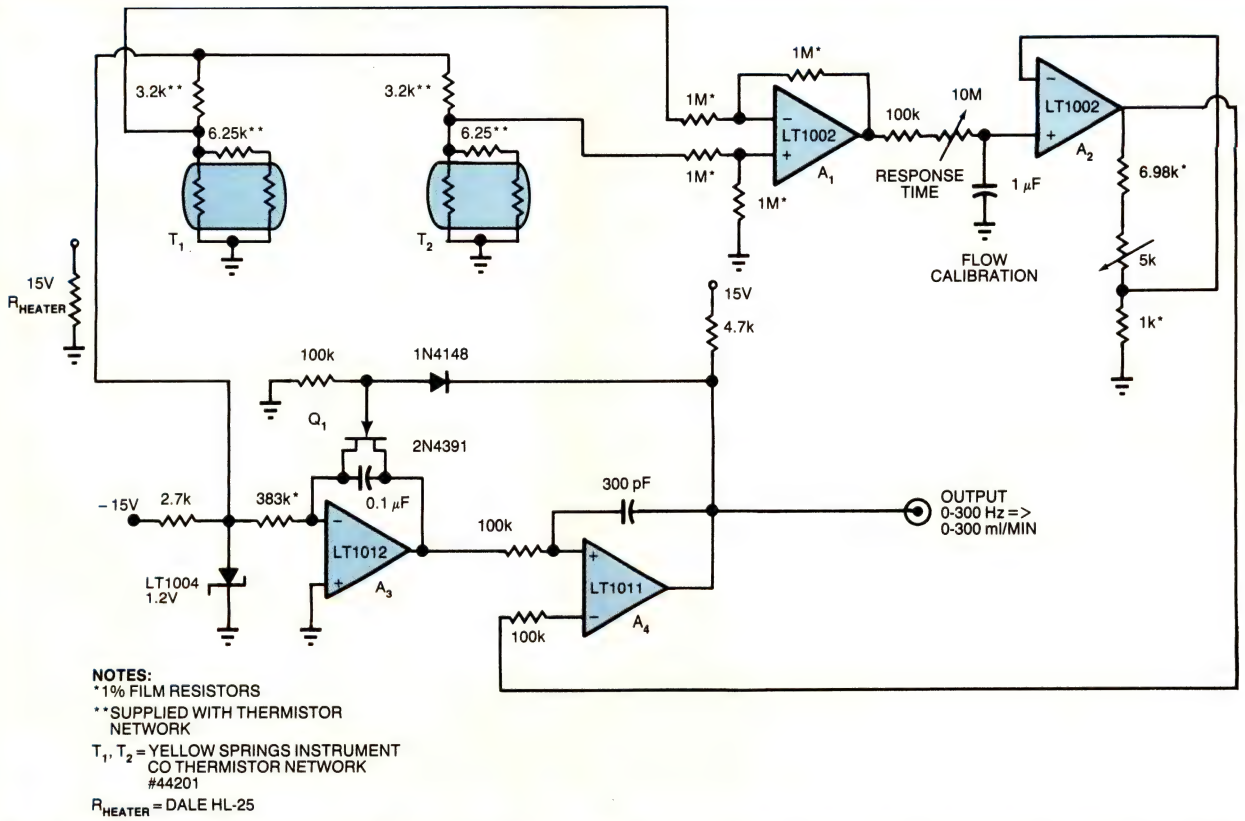


Fig 8—Overcoming the drawbacks of mechanical transducers, *this thermally based flow-meter circuit generates an output whose frequency is proportional to flow rates as low as 1 ml/min.*

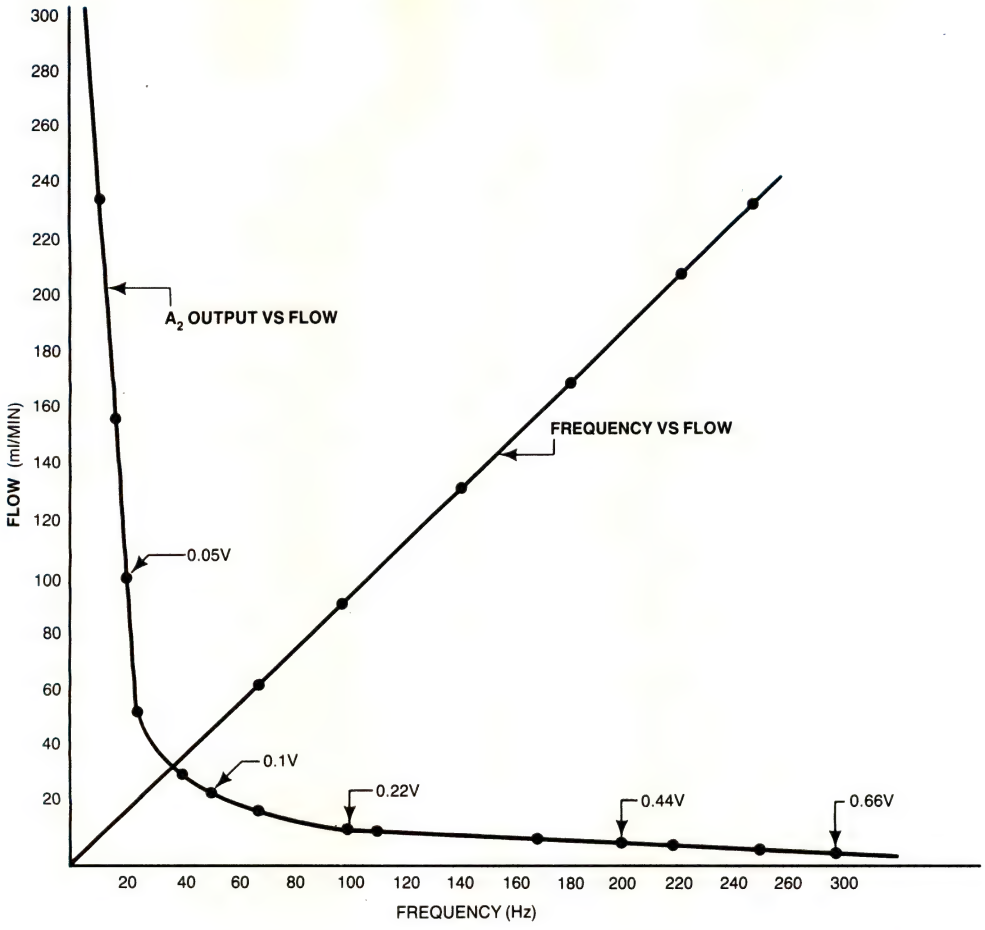


Fig 10—The temperature difference *detected by* ***Fig 8****'s sensors is inversely proportional to flow rate. Amplifiers* A_3 *and* A_4 *in* ***Fig 8*** *linearize this relationship.*

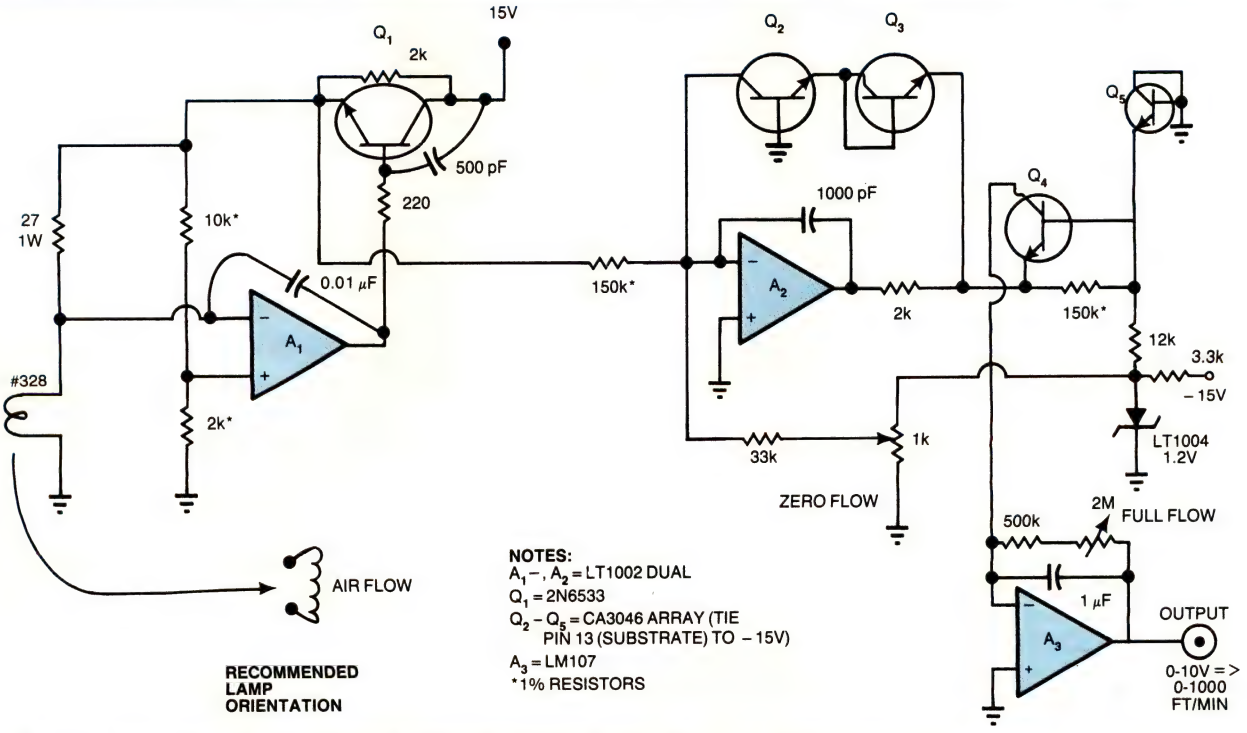


Fig 11—A lamp with its glass envelope removed *serves as the basis for a thermally based anemometer. The lamp's filament should be oriented 90° to the airflow direction.*

Thermal rms/dc converter tolerates 100:1 crest factors

achieves wide bandwidth and high crest-factor performance by directly measuring the dc heating power of the input waveform. Using thermal techniques to integrate the input waveform, it achieves a 50-MHz bandwidth with 2% accuracy. And because the thermal integrator's output is a low-frequency signal, the circuit uses standard components and requires no special trimming techniques.

The circuit works by measuring the amount of heat required to maintain two similar but thermally decoupled masses at the same temperature. The input signal is applied to T_1, a dual-thermistor bead. The power dissipated in one leg of this bead (T_{1A}) forces the other leg (T_{1B}) to shift down in value, unbalancing the bridge completed by the other bead and the 90-kΩ resistors. The A_1-A_2-A_3 combination amplifies this imbalance, and A_3's output, applied to T_{2A}, heats T_{2A} causing T_{2B} to decay in value. As T_{2B}'s resistance drops, the bridge balances, and A_3's output adjusts the drive to T_{2A} to maintain T_{1B} and T_{2B} at equal values.

Under this condition, the T_{2A} voltage should equal the rms value of the circuit's input, although in fact slight mass imbalances between T_1 and T_2 contribute a gain error, which A_4 corrects. RC filters at A_1 and A_2 and the 0.01-μF capacitor eliminate possible high-frequency error due to capacitive coupling between T_{1A} and T_{1B}. The diode in A_3's output line prevents latchup.

Fig 7 details the thermistor's recommended thermal arrangement. The Styrofoam blocks provide an isothermal environment, and coiling the thermistor leads attenuates heat-pipe effects to the outside ambient temperature. The 2-in. distance between the devices allows them to see identical thermal conditions without interacting.

To calibrate this circuit, apply 10V dc to the input and adjust the full-scale-trim pot for a 10V output at A_4. Accuracy remains within 2% from dc to 50 MHz for inputs from 300 mV to 10V. Crest factors as high as 100:1 contribute less than 0.1% additional error, and response time to within rated accuracy equals 5 sec.

Low flow-rate thermal flow meter

Another application for thermal-control techniques involves measuring low fluid flow rates, a task often fraught with difficulty. Paddlewheel and hinged-vane-type transducers, for example, have low, inaccurate outputs at low flow rates, and such transduction techniques become mechanically impractical for small-diameter tubing, such as that used in medical or biochemical work.

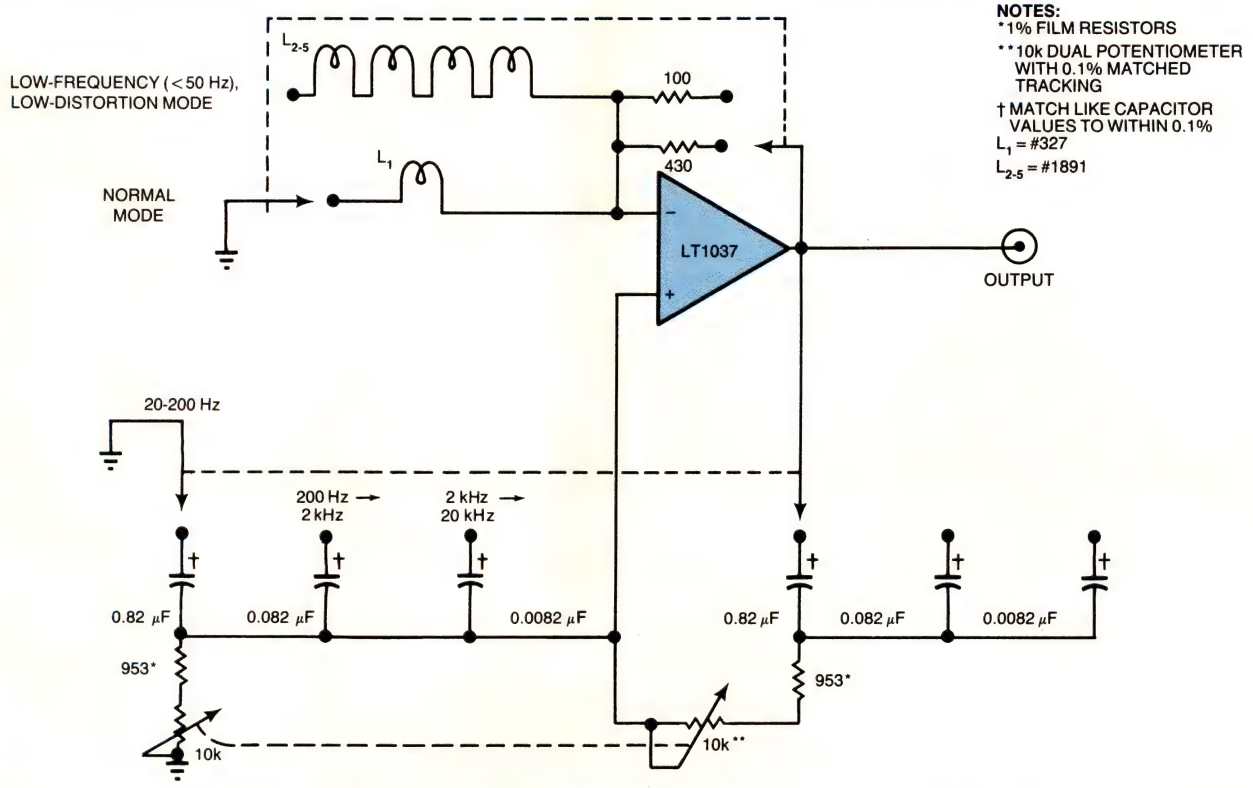


Fig 12—The positive temperature coefficient *of lamp filaments can be used to control an oscillator's gain, thus ensuring that oscillation will occur but preventing saturation limiting. The circuit regulates gain to within 0.25 dB over a 20-Hz to 20-kHz range.*

Thermal technique allows low flow-rate measurements

Fig 8 illustrates a convenient alternative technique; it generates an output whose frequency is a linear function of flow rate, and it achieves high accuracy at flow rates as low as 1 ml/min.

This circuit operates by measuring the differential temperature between two sensors arranged as shown in **Fig 9.** One sensor, T_1, measures the fluid's temperature before the fluid is heated by **Fig 8**'s 15Ω heater. The second sensor, T_2, measures the temperature rise induced into the fluid by the heater. The sensors' difference signal appears at A_1's output and is amplified by A_2, whose time constant is set via the 10-MΩ pot.

Fig 10 shows A_2's output vs flow rate—an inverse relationship. A_3 and A_4 linearize this relationship while providing a frequency output. A_3 functions as an integrator biased by the LT1004 diode and 383-kΩ input resistor; its output is compared with A_2's output at A_4. Large inputs from A_2 force the integrator to run for a long time before A_4 can go high, turning Q_1 On and resetting A_3. For small inputs from A_2, A_3 does not have to integrate very long before resetting action occurs. Thus, the configuration oscillates at a frequency inversely proportional to A_2's output voltage, yielding a frequency that linearly corresponds to flow rate.

This circuit requires attention to several thermal considerations. First, the amount of power dissipated into the fluid stream should be constant to maintain calibration. Ideally, you could measure the volt-ampere product at the heater resistor and construct a control loop to maintain constant dissipation. However, the resistor specified in **Fig 8** has a sufficiently small drift with temperature that you can assume constant dissipation with a fixed-voltage drive.

In addition, the fluid's specific heat affects calibration. **Fig 10**'s curves illustrate circuit performance for distilled water. To calibrate this circuit, set the flow rate to 10 ml/min and adjust the flow-calibration-trim pot for a 10-Hz output. The response-time adjustment allows you to filter out flow aberrations due to mechanical limitations in the pump driving the system.

A thermally based anemometer

Fig 11 shows another thermally based flow meter, but this design measures air or gas flow. It operates by measuring the energy required to maintain a heated resistance wire at a constant temperature. A type 328 lamp makes a good sensor for such a circuit because of the lamp's positive temperature coefficient and ready availability. The lamp is modified for this circuit by removal of its glass envelope.

The lamp forms one leg of a bridge, which amplifier A_1 monitors. Q_1 then current amplifies A_1's output and drives the bridge. The 500-pF and 0.01-μF capacitors and the 220Ω resistor ensure stability.

When power is applied to this circuit, the lamp's resistance is low, and Q_1 tries to turn full On. As current flows through the lamp its temperature quickly rises, forcing its resistance to increase, raising the voltage at A_1's minus (−) input. Q_1's emitter voltage then reduces, and the circuit finds a stable operating point. To keep the bridge balanced, A_1 attempts to force the lamp's resistance—and hence its temperature—to remain constant.

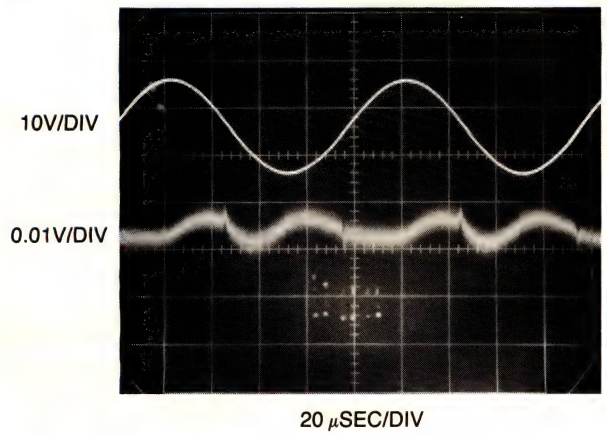


Fig 13—At a 10-kHz output, *the circuit in* ***Fig 12*** *exhibits less than 0.003% harmonic distortion. Most of this distortion is due to second-harmonic content, though some crossover disturbance is also noticeable.*

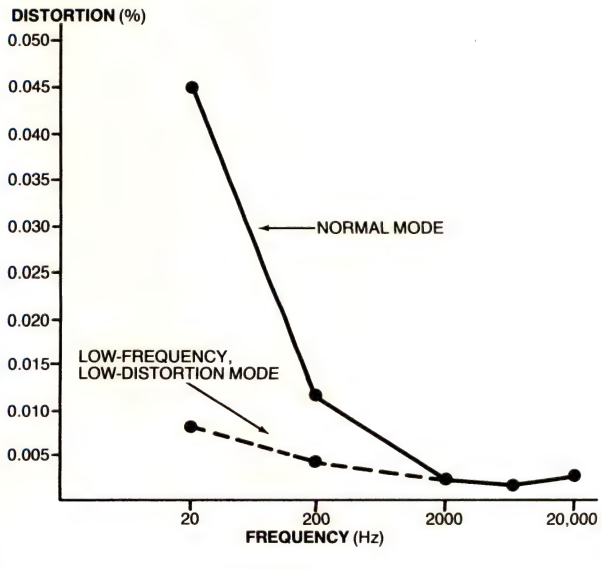
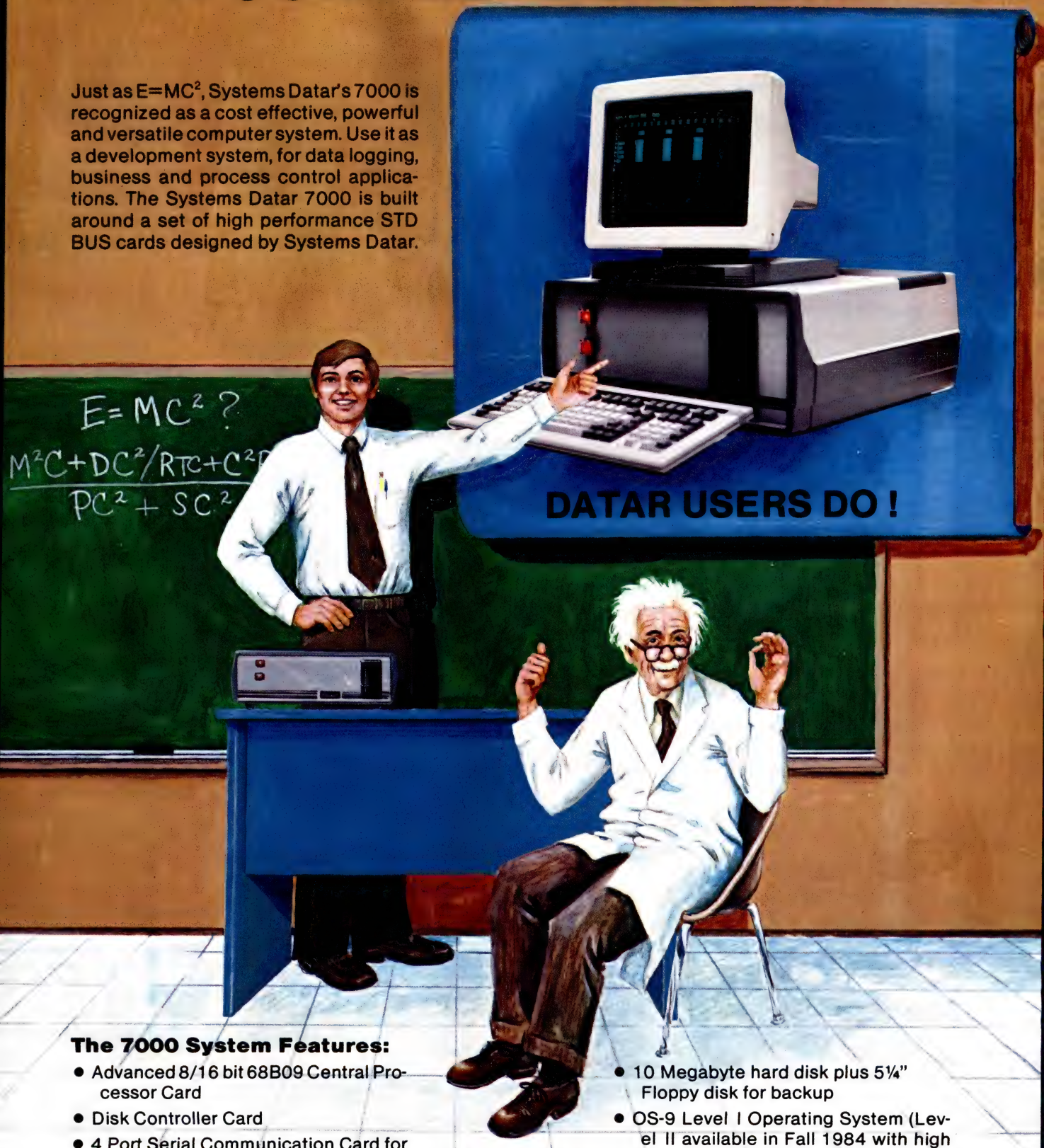


Fig 14—At low frequencies, *the* ***Fig 12*** *circuit's distortion increases. Achieving better distortion performance at the expense of reduced output amplitude, a low-frequency mode makes use of four lamps to increase the thermal time constant.*

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A lamp filament can serve as an anemometer

The 10-kΩ and 2-kΩ bridge resistance values allow the lamp to operate just below the point of incandescence—a temperature sufficiently high to minimize the effect of ambient temperature shifts on circuit operation. Under these conditions, the only physical parameter that can influence the lamp's temperature is a change in the dissipation characteristic, and airflow provides such a change. Air moving past the lamp tends to cool it, and Q_1's emitter voltage must therefore increase to raise the lamp's temperature back up to its normal operating point. Q_1's emitter voltage is thus nonlinearly but predictably related to the airflow rate. A_2, A_3 and the array transistors form a circuit that squares and amplifies Q_1's emitter voltage to yield a linear, calibrated output vs airflow rate.

To use the circuit, place the lamp in the airflow so its filament is at a 90° angle to the flow direction. Next, either shut off the flow or shield the lamp from it and adjust the zero-flow pot for a 0V circuit output. Then, expose the lamp to a 1000-fpm airflow and adjust the full-flow pot for a 10V output. These adjustments influence each other and must be repeated until both end points are at the correct level. When adjustment is completed, the circuit is accurate to within 3% over the 0- to 1000-fpm range.

A thermally stabilized oscillator

Fig 12 employs the positive temperature coefficient of lamp filaments in a modern adaptation of a classic circuit. In any oscillator, it is necessary to control gain, as well as phase shift, at the frequency of interest. If gain is too low, oscillation won't occur, and too much gain can cause saturation limiting.

The circuit in **Fig 12** uses a variable Wien bridge to provide frequency tuning from 20 Hz to 20 kHz. The lamps' positive temperature coefficients furnish the gain control. When power is first applied in the normal mode, lamp L_1's resistance is low; thus gain is high, and the oscillation amplitude builds. As amplitude builds, though, the lamp current increases, causing heating and an increase in resistance. This resistance increase in turn reduces amplifier gain, and the circuit finds a stable operating point. The lamp's gain-regulating behavior is flat within 0.25 dB over the circuit's 20-Hz to 20-kHz range. **Fig 13**'s top trace shows circuit operation at 10 kHz.

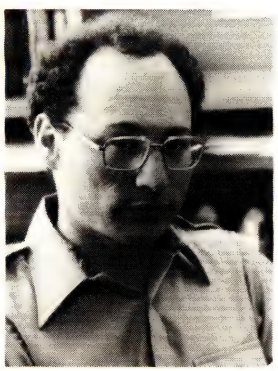
The lower trace in **Fig 13** shows harmonic distortion, which is less than 0.003%. The distortion is primarily due to second-harmonic content, and some crossover disturbance is also noticeable. The low resistance values in the Wien network and the LT1037's 3.8-nV/$\sqrt{\text{Hz}}$ noise spec eliminate amplifier noise as an error term.

At low frequencies, the thermal time constant of the small L_1 lamp begins to introduce distortion levels higher than 0.01%. Such distortion is due to hunting as the oscillator's frequency nears a level corresponding to the lamp's thermal time constant. Switching to the low-frequency, low-distortion mode eliminates this effect at the expense of reduced output amplitude and longer amplitude settling time. This mode employs four larger lamps to provide a longer thermal time constant. **Fig 14** illustrates the performance of both modes. **EDN**

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Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments.

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Understand system partitioning to optimize custom-IC use

Custom and semicustom ICs provide myriad system benefits. But realization of these advantages requires effective partitioning of large systems into economically integrated segments.

Clement Lee, Tony Valentino *and* **Dan Yoder,**
VLSI Technology Inc

Custom and semicustom ICs offer system designers the ability to decrease product size and cost while increasing product performance and design security. Exploiting this potential, however, requires more than just thoughtful IC design. It also requires careful attention to how you divide systems into easily and economically integrated sections. Indeed, system partitioning is often the most significant factor in determining the rewards of custom- or semicustom-IC application.

System partitioning, however, is a highly subjective task. Partitioning decisions depend heavily on IC, system and design-cycle economics, and optimum partitioning methods vary widely with system cost, performance and design-time needs. In addition, although ideal partitioning schemes call for chips of minimum die size, lowest packaging cost and fastest design time, these objectives are often mutually exclusive. To partition your system properly, and realize the advantages of user-designed silicon, you must assess a set of tradeoffs involving level of system integration, design flexibility, IC-design time and component costs.

A 3-dimensional problem

Because of the many factors that influence partitioning decisions and because of the variety of approaches to splitting system functions, partitioning becomes a 3-dimensional problem (**Fig 1**). Most designers partition a design by collecting in a user-designed IC all logic not included in standard-component LSI. Although this method works satisfactorily in some cases, more sophisticated alternatives such as partitioning by function or by building block often prove simpler and economical.

Along a second axis, partitioning decisions must reflect design-methodology choices. Including complex

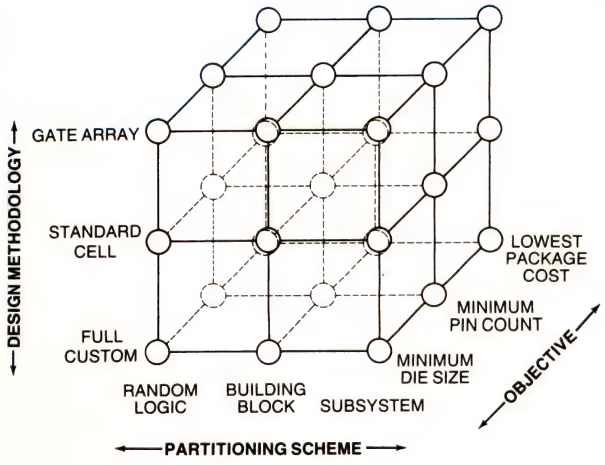


Fig 1—Because design partitioning *requires consideration of many factors, you can look upon it as a 3-dimensional problem. You must simultaneously consider the partitioning scheme, design methodology and design objective.*

Partitioning can be the key factor in semicustom designs

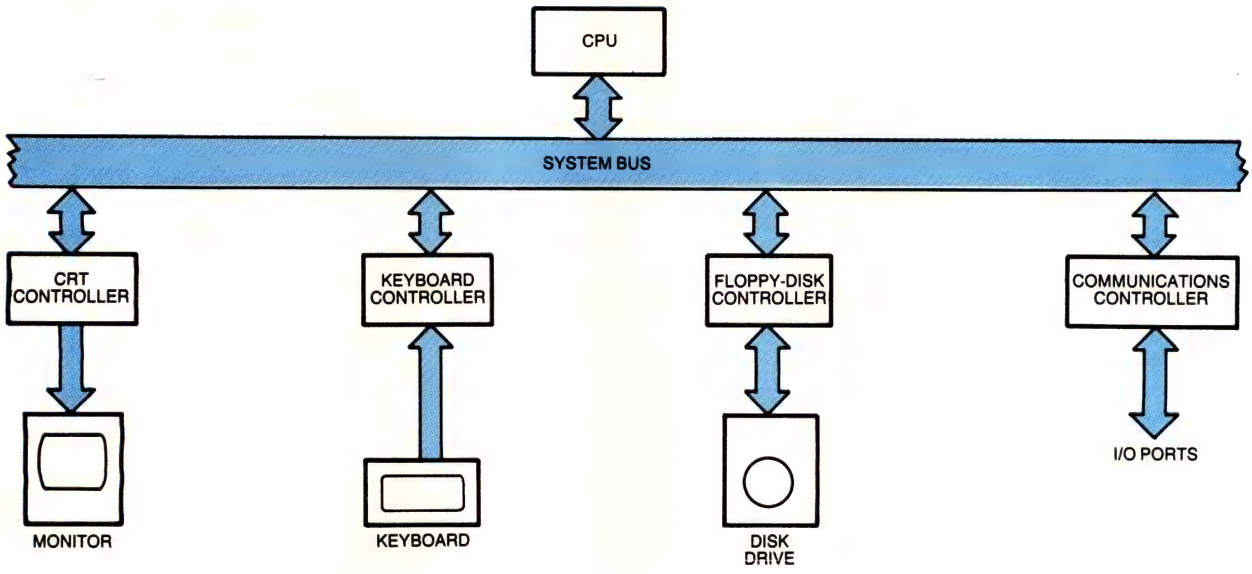


Fig 2—To understand partitioning by subsystem, *consider this block diagram of a personal-computer system. Here you divide the total system into subsystems that require minimal interconnection and that operate flexibly in a variety of applications.*

LSI circuits in custom or semicustom ICs often forces the use of specific design methodologies. Conversely, using a specific design methodology can impose constraints on partitioning alternatives. Therefore, you must consider system segmentation in light of methodology tradeoffs (see **box,** "Match methodologies to partitioning schemes").

Finally, partitioning decisions depend on semiconductor economics. Chip costs hinge on die size, pin count and package style—factors determined by IC densities and I/O requirements. As a result, segmentation decisions must reflect the cost impact of each partition's transistor count and interconnection requirements. Assessing this impact, though, requires

Match methodologies to partitioning schemes

The tradeoffs inherent to each custom and semicustom-IC methodology directly affect partitioning decisions. For example, partitioning plans that call for the integration of complex LSI circuits such as CPUs and large memory arrays rule out gate arrays. They typically don't provide the density or functional flexibility needed to implement these LSI elements. Chips incorporating such subcircuits are best suited for implementation using full-custom or cell-based-semicustom methods.

On the other hand, partitioning schemes that yield pad-limited chips are frequently good candidates for integration using gate arrays. Gate arrays typically furnish low gate/pin ratios and thus suit circuits partitioned through random-logic collection.

Just as partitioning decisions often drive methodology decisions, some methodology choices mandate specific circuit-segmentation methods. For example, a decision to exploit gate-arrays' fast design-turnaround times precludes partitioning methodologies that call for chips with on-board CPUs or memory.

Subtle differences between cell-based methodologies also affect partitioning decisions. For example, cell libraries that include fixed-dimension LSI-equivalent functions might allow you to integrate a complex circuit. But the architectural and performance constraints imposed by fixed cell dimensions might prohibit the layout of an economically producible chip. More advanced cell libraries such as those based around compliable cells allow user-defined function characteristics and thus make practical some system partitions that conventional methods render impractical.

In addition, by providing a wide variety of performance and functional options, cell-compiler libraries ensure that the cells called for by a particular partitioning scheme will be available in silicon-efficient forms.

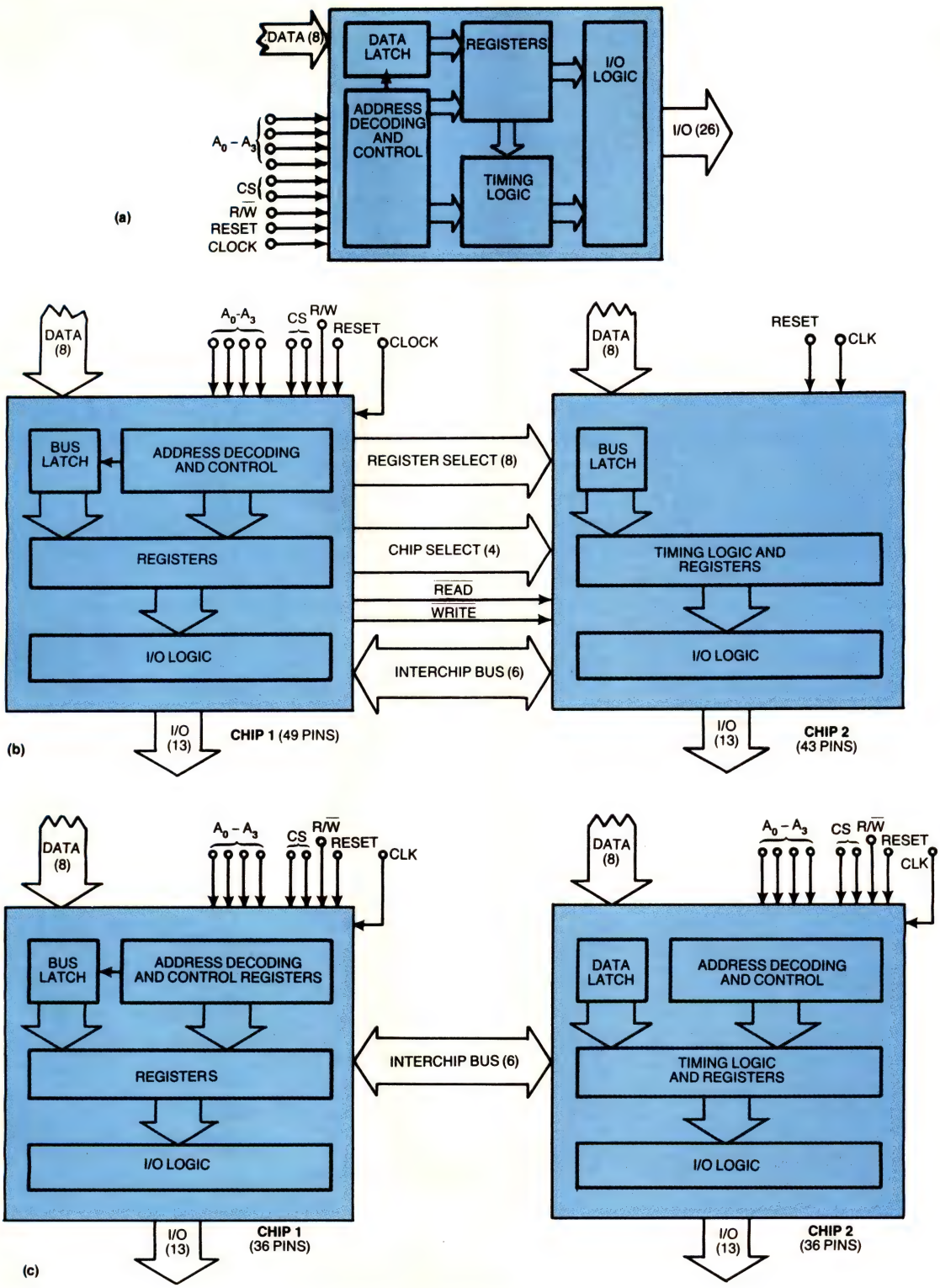


Fig 3—Examining one subsystem *helps you appreciate the decisions associated with partitioning by subsystem. In* **(a),** *the floppy-disk controller needs only 17 pins to connect to other system functions but needs 26 more pins to tie into peripherals. Using two chips for this function* **(b),** *however, raises each chip's pin count above that for the single-chip solution. Adding address decoding to each of those chips* **(c)** *requires adding only a few gates but eliminates a total of 13 pins.*

understanding of the ways in which density and I/O needs influence device cost (see **box,** "Understanding chip economics"). In addition, you must consider chip costs in light of overall system-cost concerns.

Despite the importance of methodology decisions and economic considerations, system partitioning should begin with an analysis of the three major segmentation approaches. The first approach, partitioning by subsystem, breaks a large system into a series of less complex, stand-alone subfunctions. For example, a personal computer's subsystems might include a CRT controller, floppy-disk controller, keyboard controller, communications controller and CPU (**Fig 2**). Each subsystem constitutes a complete function block and requires few connections to system buses and other subsystem blocks.

Partitioning by subfunction not only divides a large system into blocks requiring minimal interconnection, it also yields circuits usable in multiple designs. A CRT controller, for example, might prove useful in a video terminal as well as in a personal computer. Sharing one custom controller among multiple product lines reduces inventory costs, allows component cost reductions due to higher purchase volumes and speeds amortization of development expenses.

Subsystem functions entail varying complexities, but

Understanding chip economics

Effective system partitioning depends on a thorough understanding of the factors that determine IC cost. Partitioning decisions, after all, are only effective if they yield specifications for chips that reduce system costs. But to understand chip economics, you must become familiar with factors that differ significantly from the considerations of standard-component-based systems.

Basically, as you increase the number of functions included on an IC, chip die size increases. This increase results in costlier circuits because it reduces the number of dies that can be fabricated on a fixed-dimension silicon wafer (**Fig A**). In addition, as chip complexities increase, so does susceptibility to manufacturing defects. Therefore, the relationship between increases in die area and device cost are sharply nonlinear (**Fig B**). Adding large functions to already large dies entails a considerable die-cost penalty.

But added functions don't always incur increased die costs. In addition to its active circuitry, every IC includes a ring of I/O bonding pads. In high-pin-count circuits, the dimensions of these pads—and not the dimensions of active circuitry—often determine

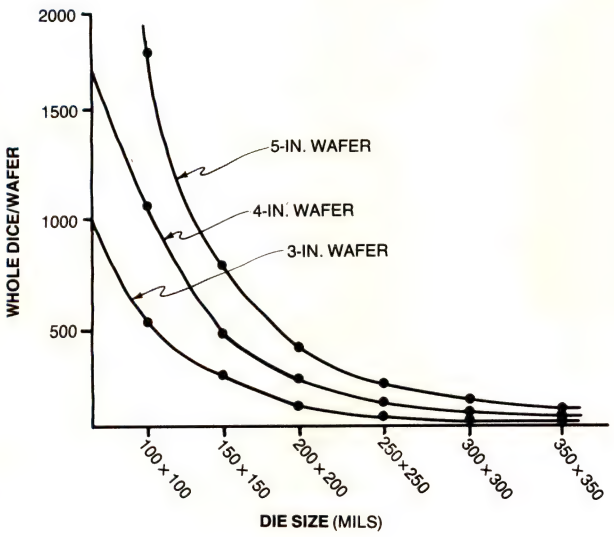


Fig A—To determine the effect of adding functions to your partitioning scheme, *consult this graph. It shows that as you add functions and increase die size, you also reduce the number of dies you can fabricate on a wafer and increase susceptibility to manufacturing defects.*

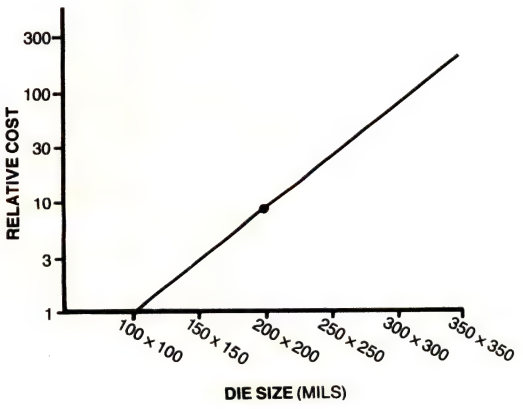


Fig B—This logarithmic curve *shows that the relationship between increase in die area and device cost are sharply nonlinear.*

all require relatively high pin counts. Although subsystems typically communicate with other system elements through efficient system buses, each requires connection to its own dedicated peripheral. These connections often require large numbers of chip-I/O pins. For example, **Fig 3a**'s floppy-disk controller requires only 17 pins to connect to other system subfunctions but needs 26 additional pins to connect to peripherals.

In some cases, you can reduce pin counts by splitting subsystem functions among multiple chips. Thus, you can reduce the peripheral-interface requirements for each chip. Unfortunately, unless carefully conceived, such schemes might increase overall I/O demands because you need additional pins to connect subsystem sections. In **Fig 3b**'s circuit, for example, each chip requires only 13 connections to peripheral devices in addition to its bus-interface pins. But 20 interchip connections raise each chip's pin count to a total greater than that for the single-chip solution.

A more effective approach to pin-count reduction involves duplicating logic in the two subsystem chips. Eight of the 20 interchip connections in **Fig 3b**'s circuit carry register-decoding data between a demultiplexer on the first chip and a register bank on the second. By including address decoding functions in both chips, you can reduce the first chip's pin count by eight pins and

die size. As long as added circuitry entails no additional I/O pins, you can add functions to pad-limited chips without significantly increasing die costs. The only cost increases incurred in such cases result from added susceptibility to manufacturing defects and added test expenses.

Adding pins to IC designs, though, often results in large cost increases. In pad-limited circuits each added I/O connection stretches die perimeters, thereby increasing manufacturing costs. In addition, even for circuits where active-device dimensions determine die size, added pins often increase packaging costs. Package costs remain a nonlinear function of pin count, especially as pin counts exceed 68 (**table**), so pin-count reductions directly affect packaged-chip expenses. In addition, each added pin entails extra test costs.

Indeed, in most designs, I/O pins cost much more than active functions. Unlike standard-component design where each added logic functions entails increased component cost, custom- and semicustom-IC design involves a series of tradeoffs between active-component and I/O costs. Because of the high costs associated with I/O pins, partitioning schemes that result in high-I/O-count circuit sections often cost more than partitions resulting in highly complex, low-pin-count ICs. Moreover, active circuitry that reduces a partitions' pin count often costs nothing.

In addition, circuitry added to pad-limited chips comes free, so you can add functions to some chips without adding cost. This situation not only adds flexibility to the system-partitioning process, but it also lets you create chips economically for multiple uses.

Most important, you must consider these chip-cost concerns in light of overall system economics. A circuit partition that combines a core μP with its peripheral circuitry might result in a large—and expensive—custom IC, but its total cost might remain less than the cost of a solution involving multiple, smaller custom chips. Such savings are especially pronounced in systems with space limitations.

Be aware, though, that because increased chip complexity is often reflected in die costs, partitions involving the integration of functions equivalent to standard LSI circuits might not be economical. But such partitioning schemes often reduce the pin counts and packaging costs of resulting custom ICs. As a result, they often represent viable partitioning approaches.

TABLE—PACKAGE TYPE VS RELATIVE COST

24-PIN DIP (PLASTIC)	$1.0
28-PIN DIP (PLASTIC)	1.18
40-PIN DIP (PLASTIC)	1.50
48-PIN DIP (PLASTIC)	3.07
68-PIN LCC (PLASTIC)	3.07
24-PIN DIP (CERAMIC)	6.78
28-PIN DIP (CERAMIC)	6.96
40-PIN DIP (CERAMIC)	9.54
48-PIN DIP (CERAMIC)	10.37
64-PIN DIP (CERAMIC)	22.68
68-PIN LCC (CERAMIC)	12.19
84-PIN GRID ARRAY	24.39
100-PIN GRID ARRAY	29.27
120-PIN GRID ARRAY	36.59

eliminate five pins from the second IC; eliminating them adds only a few gates to the second chip. Similarly, you can eliminate several additional connections by duplicating chip-select and read-write decoders on the second chip. Thus each segmented chip requires only 36 I/O pins (**Fig 3c**).

In many cases, subsystem-oriented partitioning schemes demand the integration of LSI functions similar to those available as off-the-shelf components. Thus, to effectively partition by subsystem, you must use a cell library that includes high-level, LSI-equivalent functions. Constructing such functions from low-level elements, like those found in gate-array and limited standard-cell libraries, is risky unless you understand the technical ambiguities of the required LSI circuits.

Build it with blocks

A second partitioning method, with building blocks, suits systems with highly structured or repetitive architectures, or circuits involving no clearly definable stand-alone subsystems. Instead of requiring the definition of large system blocks, this method requires you to isolate less complex basic system elements that can be used repeatedly throughout single or multiple systems. Often, by imbuing these building blocks with small amounts of added logic, you can create general-purpose ICs that suit use in widely differing systems.

You can employ the building-block approach to any system by stripping from its design all the glue logic that makes the circuit application specific. The remaining elements, such as registers, ALUs, controllers and I/O elements, constitute the circuit's basic building blocks. You'll often find that these elements are common to many systems. In addition, the building-block approach is useful in circuits involving arrays of similar elements, such as multibit data-path and CPU designs, which you can break down into identical bit-, nibble- or byte-wide structures.

As an example of a circuit that lends itself to building-block partitioning, consider **Fig 4a**'s printer controller. Six 8-bit parallel ports and an 8k×8 ROM connect to one processor bus. By dividing the circuit

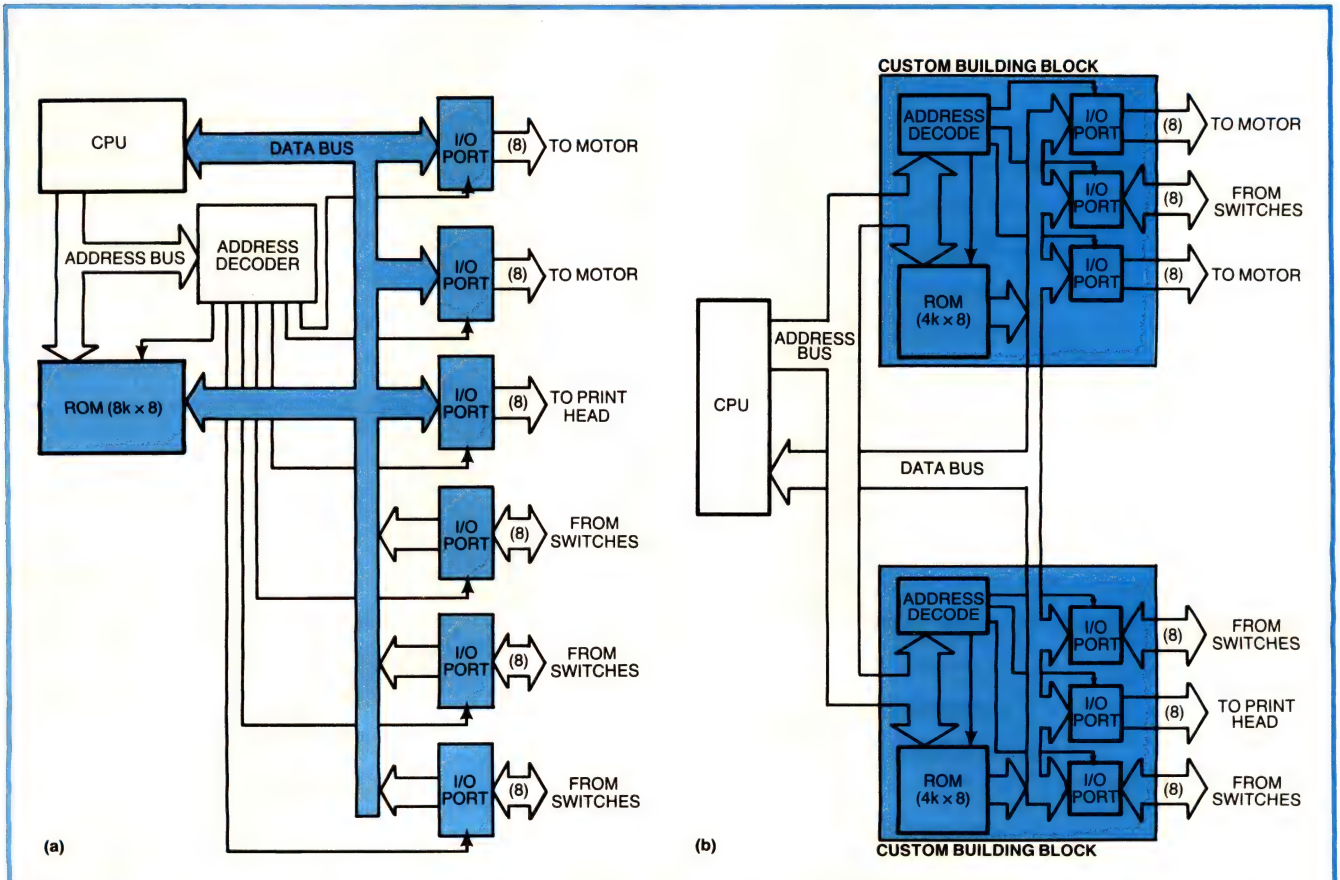


Fig 4—Use the building-block approach to partitioning *in systems with regular architectures or those without definable stand-alone subsystems. This example of a printer controller* ***(a)*** *ties six parallel ports and a ROM to one processor bus. By dividing it into two 3-port blocks* ***(b)*** *you must add address decoding but you eliminate five pins and also produce a chip that could easily suit other systems.*

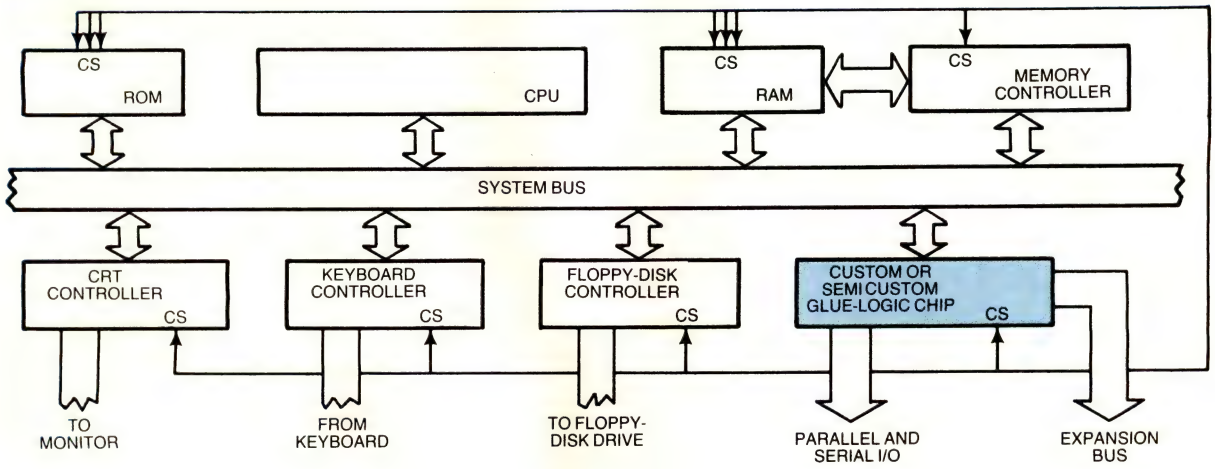


Fig 5—Partitioning by random-logic collection *typically integrates all functions not performed by standard LSI circuits. The personal-computer system puts chip-select decoding, expansion-bus buffering and standard I/O functions in a semicustom chip.*

into two 3-port, 4k-byte building blocks (**Fig 4b**), you can implement it using two custom or semicustom ICs and a standard-component microprocessor. In addition, by doing so you create a combination ROM/parallel-interface chip that might suit use in other systems.

Note that you should include address-decoder logic in both chips. Not only does this logic duplication allow you to implement the system using two identical custom or semicustom chips, it also saves pins. The μP address bus must enter the building block to feed the ROM array, so internal address decoding saves the need for dedicated I/O-select inputs. In **Fig 4b**'s example, the small amount of logic added by the internal 2-to-4-line decoder is more than offset by the elimination of three package pins.

By allowing the definition of ICs suited for use in multiple designs, partitioning by building blocks often allows multiple systems or design projects to share non-recurring engineering (NRE) charges. Adding a few gates to enhance circuit versatility requires considerably less engineering expense than the design of a new IC. You can reduce the design times and costs for several applications through the development of general-purpose, proprietary building blocks.

Moreover, custom building blocks benefit from economies of scale. Because they're used in multiple applications, you typically purchase them in higher volumes

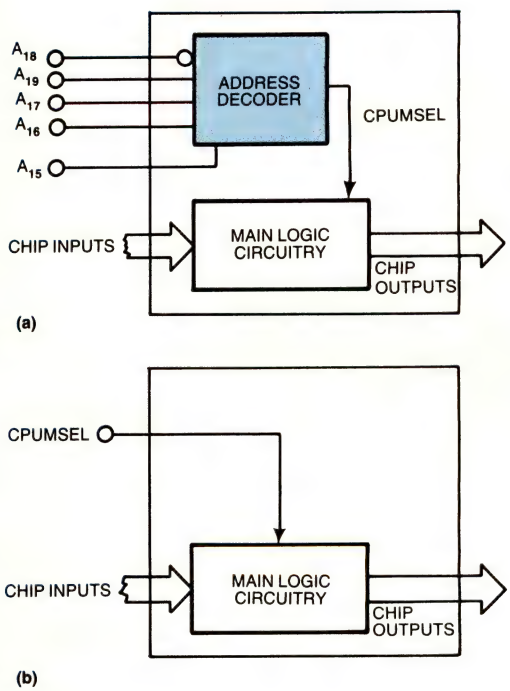


Fig 6—Removing circuitry from random-logic partitions *can sometimes reduce pin counts. The peripheral in* ***(a)*** *requires five input lines for the chip-select signal; using an off-chip address decoder eliminates four pins* ***(b).***

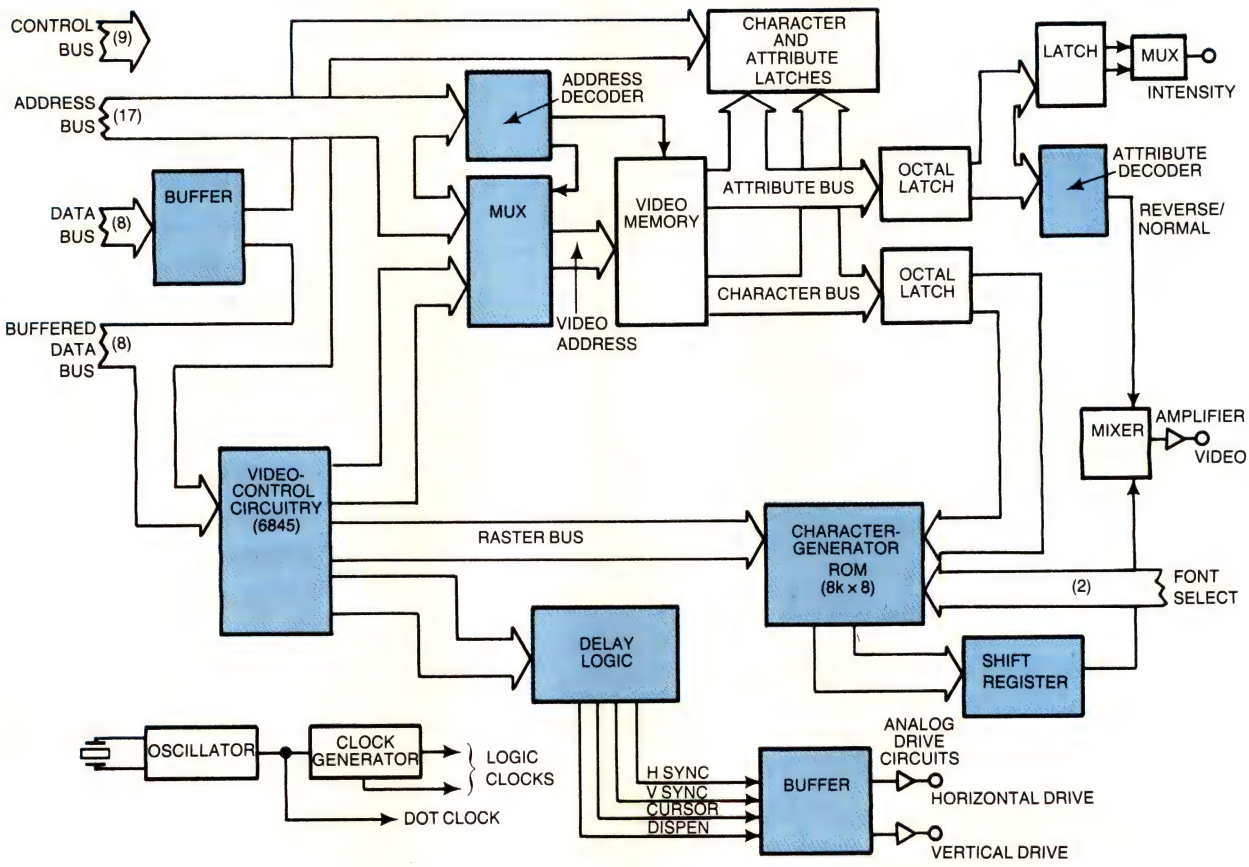


Fig 7—Use this CRT controller circuit *to examine each of the three partitioning schemes discussed. The resulting partitions are given in* ***Figs 8, 9*** *and* ***10.***

than single-system custom or semicustom chips with corresponding lower purchase prices. Furthermore, standardization of user-designed building blocks results in simplified inventory and field-service procedures.

Bear in mind, however, that the development of effective, widely applicable building blocks requires considerable forethought. To isolate those circuits that are candidates for multiproduct use, you must consider the nature of current design projects as well as the characteristics of future projects. Remember that the extra active circuitry required to increase the versatility of a circuit partition often costs nothing.

Logic collection provides fast turnaround

Despite the advantages of more sophisticated partitioning schemes, partitioning by random-logic collection can result in efficient system integration. By integrating all functions not performed by standard LSI circuits, you can quickly exploit semicustom ICs' advantages without incurring the risks inherent in the customization of LSI functions. Partitioning by random-logic collection is best suited to gate-array designs because it yields semicustom devices devoid of CPUs, large memories and other LSI functions. In addition, chips created as a result of random-logic partitioning typically feature low gate counts and high pin counts so they're often pad limited.

As an example of a system partitioned by random-logic collection, consider **Fig 5**'s personal-computer circuit. The system CPU as well as controllers for the keyboard, floppy disk, CRT and memory are implemented with off-the-shelf LSI components. Chip-select decoding, expansion-bus buffering and basic I/O functions, normally the province of SSI and MSI devices, are performed by a semicustom chip. By incorporating all SSI and MSI functions in one package, the system exploits the benefits of user-designed ICs without requiring the design of complex LSI circuits.

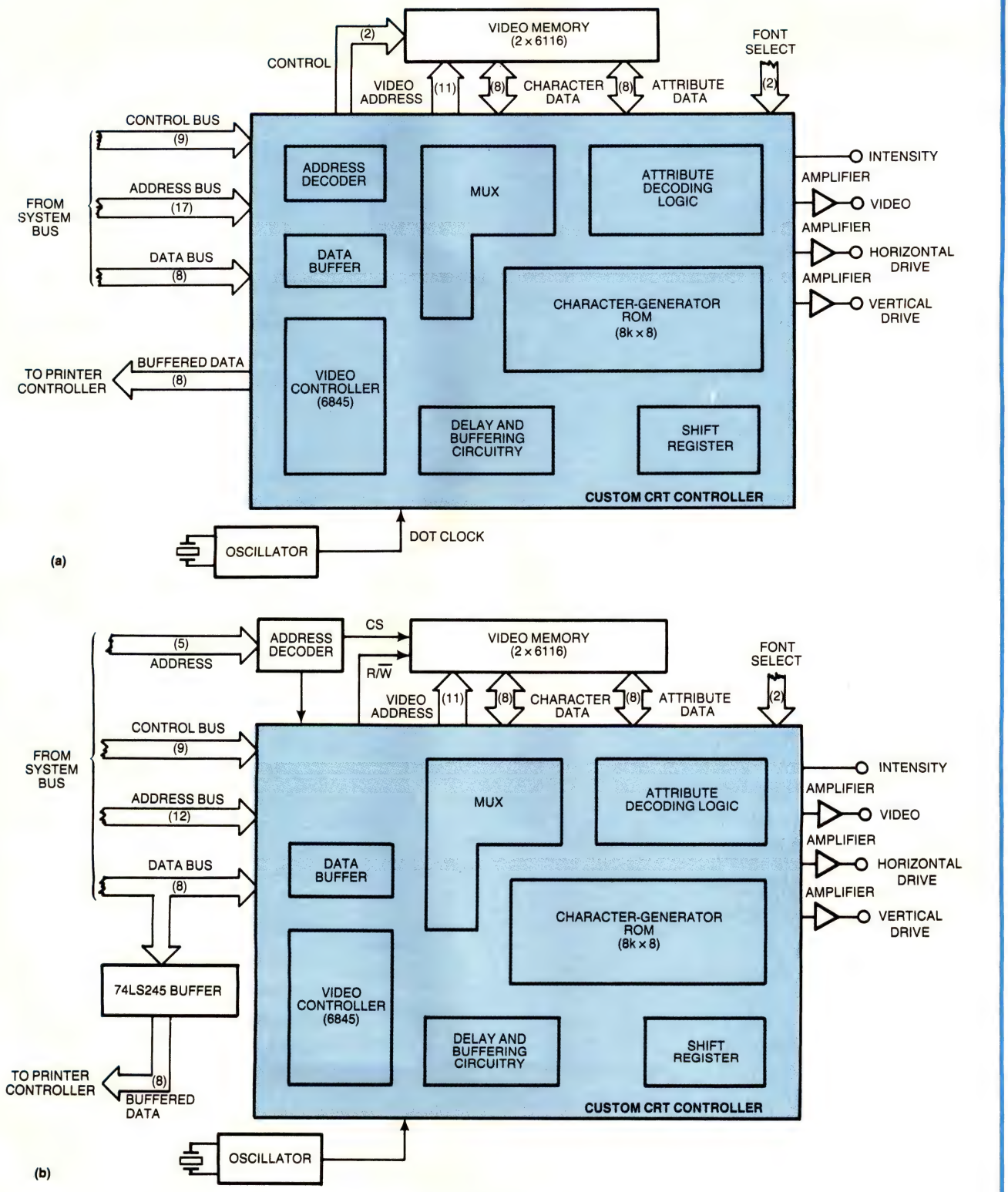


Fig 8—When you integrate as much of Fig 7's logic as possible, *you get this partitioning. The scheme in* ***(a)*** *requires 78 I/O pins and makes low-cost packaging difficult if not impossible. Duplicating a transceiver off-chip reduces pin count by eight, and eliminating the on-chip address decoder does away with another five pins.*

Try duplicating logic to reduce total system pin count

Because ICs designed through random-logic collection often include only loosely related functions, their gate-to-pin ratios remain low compared with those of more structured chips. You can improve these ratios, and thereby allow die-size reductions in some cell-based devices, by carefully examining the need for I/O-intensive on-chip circuitry.

For instance, you can often eliminate pins from a random-logic IC by duplicating logic. As in **Fig 4b**'s building-block example, demultiplexers included within random-logic partitions often save package pins. For example, including a 3-to-8-line decoder saves five pins while adding minimal active circuitry.

On the other hand, removing circuitry from random-logic partitions can sometimes reduce circuit pin counts. In **Fig 6a**'s peripheral circuit, for example, an on-chip address decoder requires five input lines to generate a chip-select signal (CPUMSEL). Moving the address decoder off chip eliminates four package pins (**Fig 6b**).

In addition, you can often reduce random-logic circuits' die sizes by multiplexing or encoding output signals. Typically employed in 16-bit μPs, this technique often results in significant pin-count reductions with only minimal increases in active-component areas.

Examine the tradeoffs

To understand the tradeoffs involved in circuit partitioning, consider an example based on a CRT controller similar to that in the IBM PC's monochrome-display adapter. The basic circuit (**Fig 7**) includes a bus interface, address and chip-select decoders, memory-address multiplexers, CRT timing generators, display formatter, character generator, video memory, output shift register and a data-bus buffer that feeds both CRT-control and printer-port circuitry. A standard-component implementation of this circuit requires two 6116 2k×8 static RAMs, a 2364 8k×8 character-generator ROM, a 6845 CRT controller, 21 SSI circuits and 31 MSI chips—a total of 56 ICs. The percentage of this logic incorporated on a custom or semicustom chip depends on partitioning approach.

One approach to partitioning the CRT controller circuit integrates as much logic as possible. This method results in the greatest level of integration and thus affords the greatest system size and cost savings. But because most chip functions are performed by fixed, on-chip logic, this approach furnishes minimal performance flexibility.

Fig 8a illustrates a partitioning scheme that integrates as much of the controller's logic as is practical with custom or semicustom MOS processes. In general, MOS processes don't lend themselves to integrating analog functions, so this sample partition doesn't include the controller's analog CRT-drive circuits. In addition, this partition excludes video-memory circuits because these relatively large memories are most cost effective when purchased as standard components.

Fig 8a's first-pass partition requires 78 I/O pins: 42 for system- and printer-bus interfaces, 29 for video-memory-interface functions and seven for video-output, font-selection and clock functions. Unfortunately, low-cost DIPs are available with only as many as 48 pins, and low-cost plastic leaded chip carriers with more than 68 pins aren't widely available. To eliminate the need for expensive ceramic or custom-tooled plastic packages, you must reduce the controller's pin count.

One way to reduce pin count for the controller partition is to eliminate bus-interface logic. For example, the circuit's data bus inputs feed an octal transceiver that buffers data transfers. The buffered data signals (BD_0-BD_7) feed both the CRT controller and a printer-interface circuit. Thus, when the latch resides only on the CRT-controller chip, eight I/O lines bring buffered data signals off the chip. Duplicating the transceiver off chip, however, eliminates the need to bring out the BD bus, thereby saving eight pins (**Fig 8b**). You could also eliminate package pins by eliminating the data buffer from the custom chip. But unlike **Fig 8b**'s logic-duplication scheme, that approach requires you to bring data-direction signals off chip, and thus requires extra pins.

Moreover, eliminating the on-chip address decoder reduces the controller's pin count by five more pins, resulting in a total I/O count of 65 pins. As a result, the circuit can reside in a low-cost 68-pin leaded enclosure. With this partitioning scheme, a custom or semicustom chip replaces a total of 18 SSI chips, 26 MSI ICs and two LSI circuits. The chip includes 72,600 transistors, and, if built using 3-μm HMOS processes, requires die dimensions of 240×240 mils. If predefined cells for the 6845 and 2364 LSI circuits are available, the chip might require 18 to 20 weeks to design; building those LSI circuits from SSI elements might increase chip-design time to 35 to 40 weeks.

Off-chip ROM adds flexibility

Fig 8's partitioning schemes result in chips that afford greatest cost savings over standard-component implementations, especially in high-volume applications. But because they call for an on-chip character-generator ROM, they lock in the CRT controller's display capabilities. A more versatile approach allows modification of the circuit's character repertoire.

One means for allowing character-generator alteration involves designing several versions of **Fig 8b**'s circuit and combining them on a multiproject wafer. Each version could include different ROM data and thus

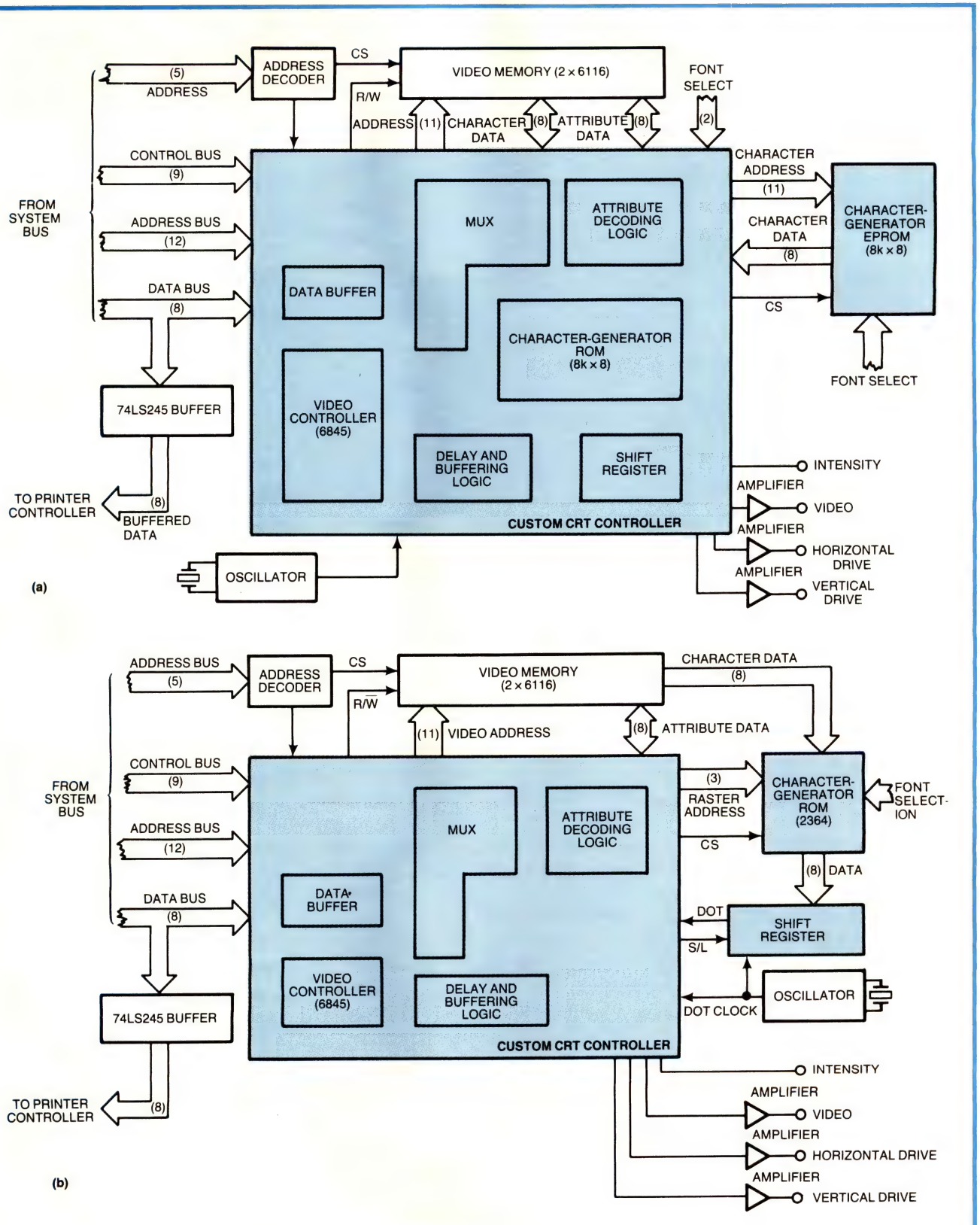


Fig 9—Enhance this circuit's flexibility *by bringing character-generator-ROM address and data lines off chip* ***(a).*** *This approach requires 85 I/O pins, forcing the design into an expensive ceramic package. When you take the entire ROM off chip along with the video shift register* ***(b),*** *you can get by with 61 I/O pins and eliminate 90% of the chip's transistors.*

Block partitioning suits systems without definable subsystems

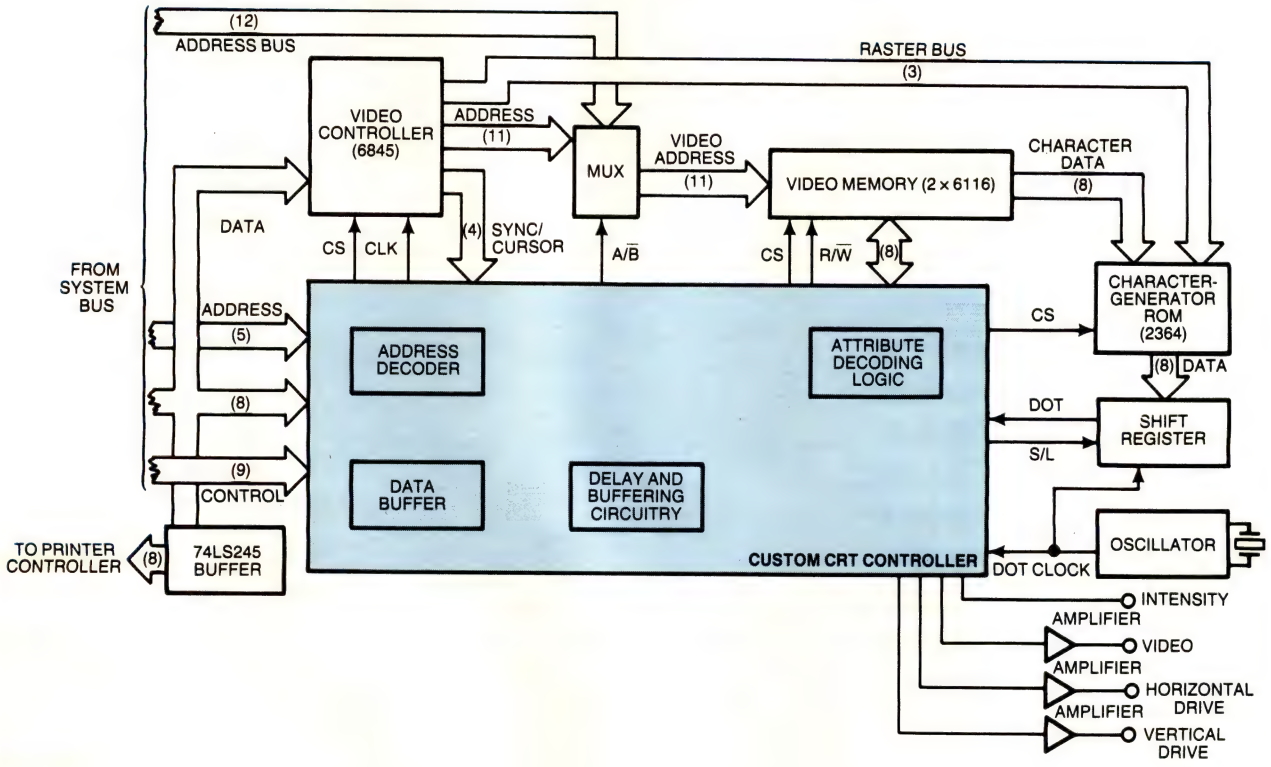


Fig 10—Partitioning the controller to include only SSI and MSI circuits *reduces transistor count to 3000. The glue-logic chip requires 46 I/O pins.*

produce a different character set. Each multiproject wafer would include a fixed number of each chip version; because they're produced in parallel on one wafer, all versions can be accommodated by a single set of production tooling.

As an alternative, you could add flexibility to the CRT controller's character set by bringing character-generator-ROM address and data lines off chip. Then an external EPROM or EEPROM could determine the circuit's video repertoire. This memory could shadow the internal ROM, thus providing a tool for prototyping and character-set debugging as well as furnishing means for adding chip versatility. Unfortunately, such a partitioning scheme (**Fig 9a**) requires 85 I/O pins and forces the controller circuit into an expensive ceramic package.

A third method for enhancing circuit flexibility removes the character-generator ROM and video shift register from the controller chip. Doing so not only provides external character-set programmability, it also eliminates nearly 90% of the chip's transistors and 37% of its area. The resulting chip (**Fig 9b**) requires 61 I/O pins and occupies 190×190 mils. However, because the chip still requires a high-pin-count package and because it demands the use of several external components, its die-cost savings don't necessarily contribute to decreased system costs.

For greatest flexibility and least risk, you could partition the CRT controller to include only SSI and MSI circuits (**Fig 10**). By relying on a standard-component LSI controller, you could create a chip that performs all of the example circuit's glue-logic functions, but one that requires only 3000 transistors. The glue-logic chip requires 46 I/O pins and could be designed in 16 weeks. Although this approach results in a custom chip with a level of integration far lower than that of the other options, it entails the least risk.

The nearby **table** summarizes the tradeoffs of each approach. As you can see, **Fig 8**'s high-level-integration approach affords the greatest system cost savings but requires the longest development time. On the other hand, the random-logic approach provides 75% of the cost savings of the first method but enables faster development. Note that cost-savings estimates are

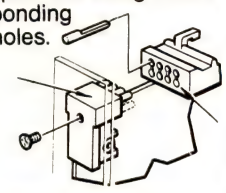
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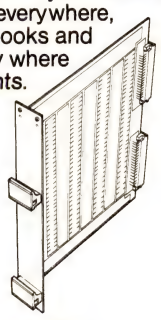
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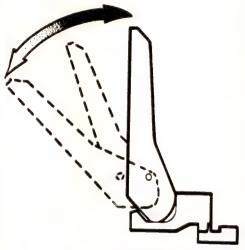
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1983

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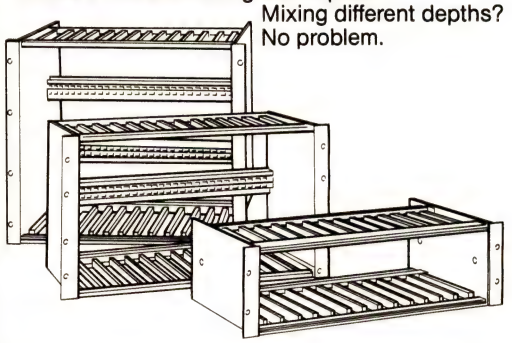
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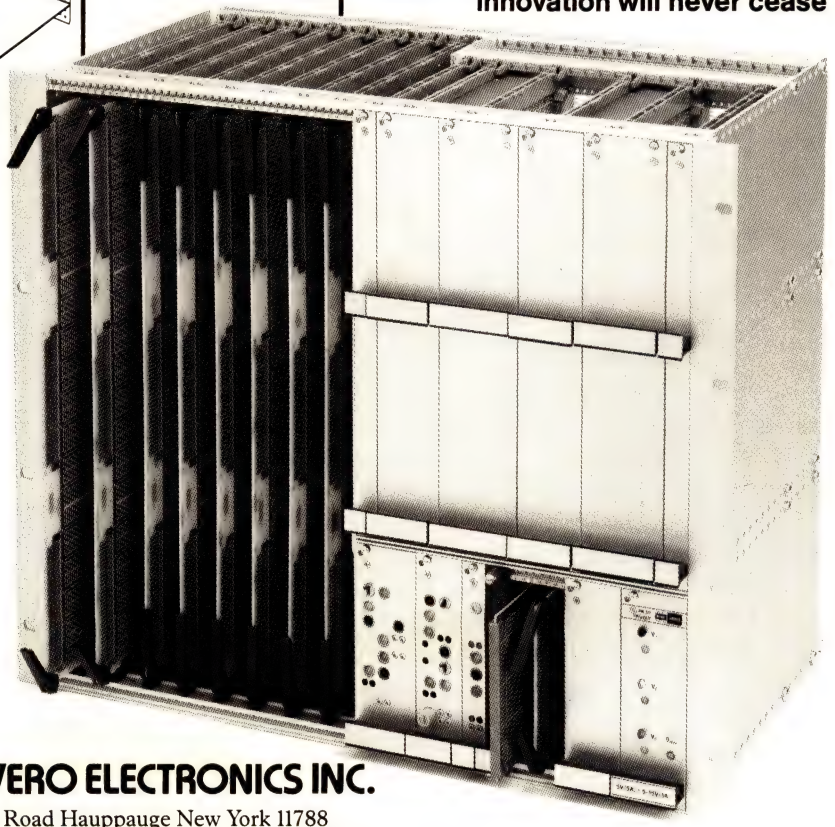
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TABLE—SUMMARY OF PARTITIONING ALTERNATIVES

APPROACH	ISC REPLACED	PINS	DIE SIZE (MILS)	TRANSISTOR COUNT	TRANSISTORS/PIN	MIL² PER TRANSISTOR	ICs IN SYSTEM	DEVELOPMENT TIME (WEEKS)	COST SAVING/SYSTEM
HIGH-LEVEL INTEGRATION	46	65	240 x 240	72,600	1117	0.79	5	18 TO 40	$23.00
EPROM AND INTERNAL ROM	43	85	248 x 248	72,800	856	0.84	6	18 TO 40	$21.50
EXTERNAL ROM AND S/R	41	61	190 x 190	7100	116	5.08	7	17 TO 39	$20.50
RANDOM-LOGIC PARTITION	34	46	180 x 180	3000	65.2	10.8	8	16 TO 18	$17.00

based on pc-board, power-supply, inventory and insertion costs averaging $0.50 per chip. In addition, the table's cost data assumes that a custom or semicustom IC's cost equals the total cost of the standard components it replaces.

Partition efficiency is reflected in the ratios of pins to transistors and transistors to die area. Transistor/pin ratios are highest for the densest chips and fall sharply as densities decrease. Similarly, each transistor in the high-level-integration approach occupies 0.79 mil² compared to 10.8 mil² for the random-logic approach. These figures not only reflect the pad-limited nature of the random-logic chip but also suggest the relatively high densities of chips incorporating large ROM arrays.

Be sure to consider the advantages and disadvantages of each approach in light of system-design and -cost concerns. The first approach provides the best silicon utilization but might prove unsuitable in applications requiring product versatility and extremely fast turnaround times. Conversely, the last approach provides the fastest time to market but might violate system-size constraints in some applications.

Most important, consider development expenses in light of system-cost savings. Although this example's first partitioning approach might mandate high development expenses, its $23 cost reduction per system provides a fast payback. For instance, you can recoup a $100,000 development cost after the production of fewer than 4500 units. **EDN**

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

Authors' biographies



Clement Lee is strategic marketing manager at VLSI Technology Inc (San Jose, CA) involved in product planning and applications. He also helps customers partition their systems in cost-effective ways. He worked previously for Supertex and Synertek. His educational background includes a BSEE from the University of Michigan (Ann Arbor) and two years of graduate work there.



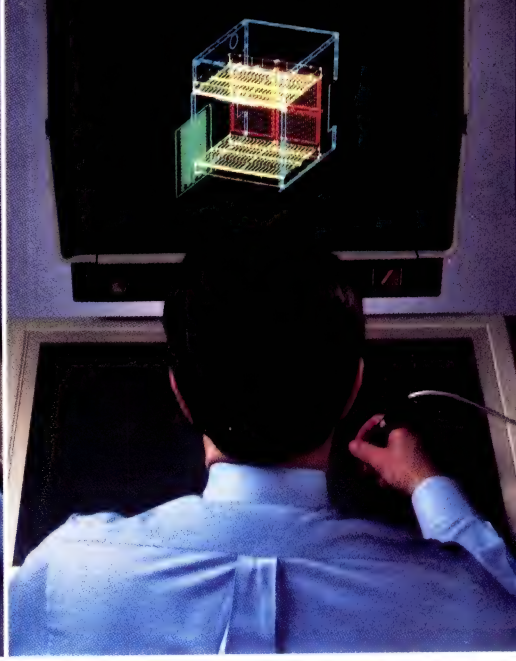
Tony Valentino, custom products marketing manager for VLSI Technology Inc, has worked at that firm for two years. He has also worked for Texas Instruments and has earned a BSEE at the University of Michigan (Ann Arbor) and an MBA at the University of Missouri (St Louis). In his free time, Tony enjoys designing and constructing windows and lamps with stained glass.



Dan Yoder is manager of customer services in VLSI Technology's customer specific product group, where his duties involve systems integration and megacell development. Dan joined the firm only one year ago after working for Timex Corp. He received his BSEE from the University of Santa Clara.







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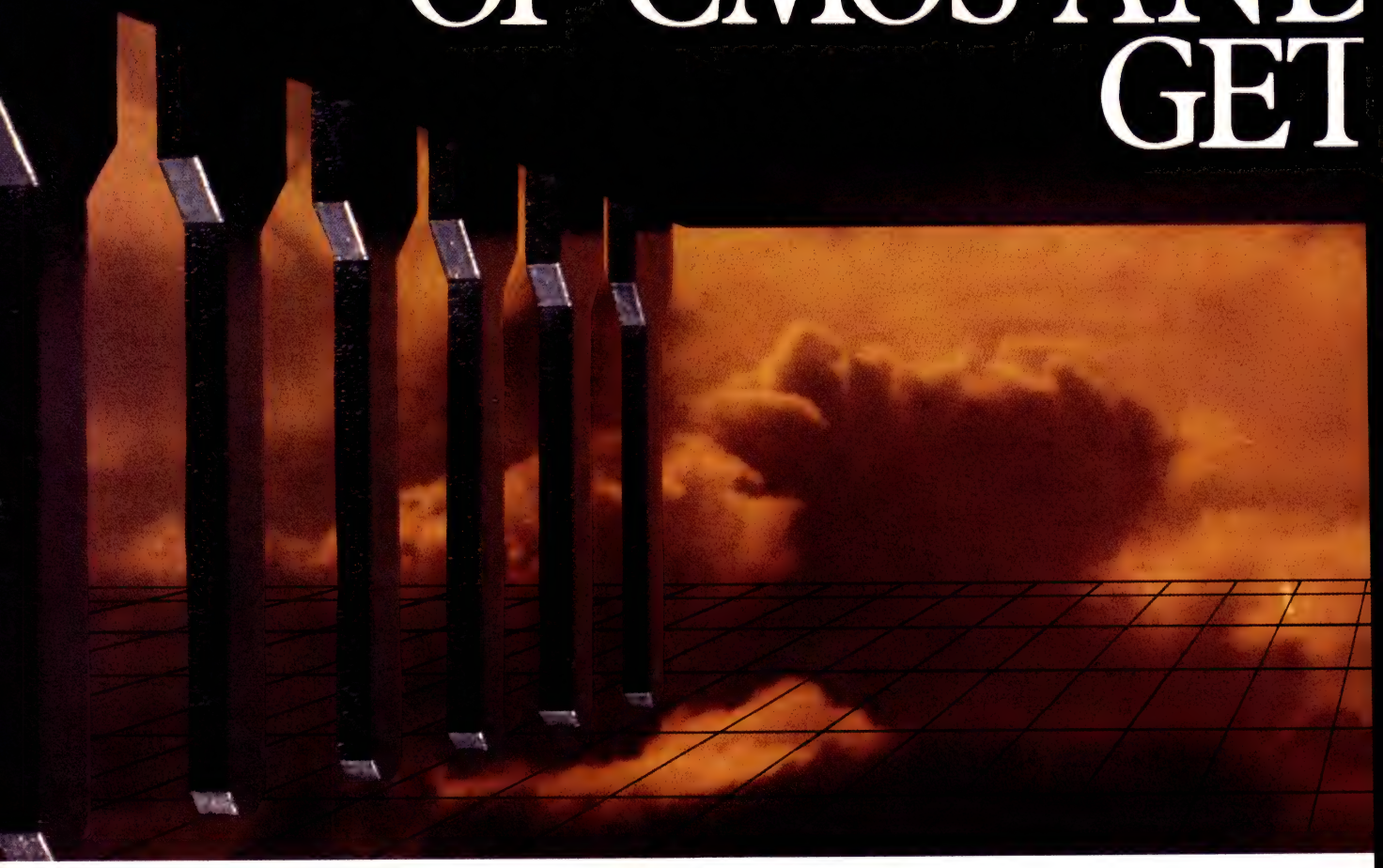
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TMP80C49	CMOS	2K	128	6MHz	10mA	10μA
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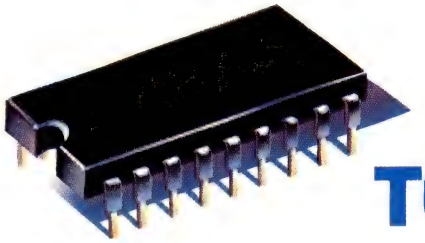
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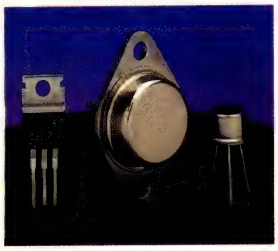
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RFL1N15L	TO-39	1A	150V	8.33	2.15Ω	1.79
RFL1N18L	TO-39	1A	180V	8.33	3.65Ω	1.29
RFL1N20L	TO-39	1A	200V	8.33	3.65Ω	1.79
RFP2N18L	TO-220	2A	180V	25	3.50Ω	.74
RFM8N18L	TO-3	8A	180V	60	0.60Ω	2.57
RFM8N20L	TO-3	8A	200V	60	0.60Ω	3.56
RFP8N18L	TO-220	8A	180V	60	0.60Ω	1.59
RFP8N20L	TO-220	8A	200V	60	0.60Ω	2.20
RFM12N08L	TO-3	12A	80V	100	0.20Ω	2.51
RFM12N10L	TO-3	12A	100V	100	0.20Ω	3.48
RFP12N08L	TO-220	12A	80V	75	0.20Ω	1.59
RFP12N10L	TO-220	12A	100V	75	0.20Ω	2.20
Available second quarter 1984.						
RFL2N05L	TO-39	2A	50V	8.33	0.80Ω	
RFL2N06L	TO-39	2A	60V	8.33	0.80Ω	
RFP2N08L	TO-220	2A	80V	25	1.25Ω	
RFP2N10L	TO-220	2A	100V	25	1.25Ω	
RFP2N12L	TO-220	2A	80V	25	2.00Ω	
RFP2N15L	TO-220	2A	100V	25	2.00Ω	
RFP2N20L	TO-220	2A	200V	25	3.50Ω	
RFP4N05L	TO-220	4A	50V	25	0.80Ω	
RFP4N06L	TO-220	4A	60V	25	0.80Ω	
RFM10N12L	TO-3	10A	120V	60	0.30Ω	
RFM10N15L	TO-3	10A	150V	60	0.30Ω	
RFP10N12L	TO-220	10A	120V	60	0.30Ω	
RFP10N15L	TO-220	10A	150V	60	0.30Ω	
RFM15N05L	TO-3	15A	50V	60	0.15Ω	
RFM15N06L	TO-3	15A	60V	60	0.15Ω	
RFP15N05L	TO-220	15A	50V	60	0.15Ω	
RFP15N06L	TO-220	15A	60V	60	0.15Ω	

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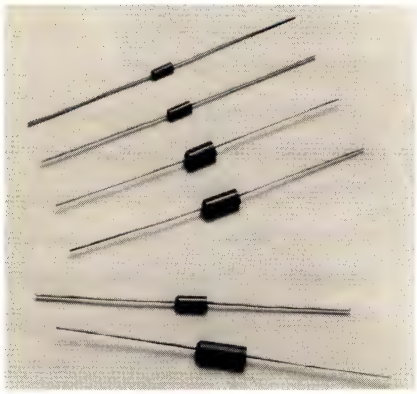
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CIRCLE NO 103

DESIGN IDEAS

Edited by Bill Travis

Nested functions calculate standard Rs

David Bidwell
RFL Industries Inc, Boonton, NJ

If you program in BASIC, you can use nested user-defined functions to perform repetitive calculations too complex for a single function. As an alternative to a subroutine call, this technique can result in a smoother flow to the source code. Consider, for example, the algorithm for selecting standard 1% resistors (EDN, March 3, 1982, pg 167). If you include the following four lines of code anywhere in a BASIC program,

```
100 DEF FNN%(R)=INT(0.5+96*LOG10(R))
110 DEF FNO(R)=10 ↑ (FNN5(R)/96)
120 DEF FNP%(R)=INT(LOG10(FNO(R)))-2
130 DEF FNR(R)=10 ↑ (FNP%(R))*
    INT(0.5+FNO(R)/10 ↑ (FNP%(R)))
```

then (FNR)R will be the closest standard 1% value for any computed value of resistance R.

The following examples illustrate the program's execution:

```
READY
PRINT FNR(15.97)
16.2
READY
PRINT FNR(2397),FNR(148.5E3),FNR(148.6E3)
2370        147000        150000
READY
```

In the example, note that once this segment of code has been executed, the functions have been defined and can then be used in the immediate mode. The technique has been used successfully with Digital Equipment's RT-11 BASIC on a PDP-11, and will probably work with most BASICs. However, an attempt to use it with a VIC-20 proved unsuccessful. The algorithm is subject to minor inaccuracies for median values as discussed in the referenced article. **EDN**

To Vote For This Design, Circle No 750

Write protect 8-in. disk drives

Donald Patterson
Argonne National Lab, Argonne, IL

The circuit in **(b)** adds a write-protect switch and indicator light to Shugart Models SA801 and SA800 8-in. disk drives. You can also use the circuit for other manufacturers' drives or other Shugart models. The scheme provides a switch that write protects the disk via hardware the same way the disk is write protected by an uncovered notch. The LED turns on whenever the disk is hardware write protected, either by the switch or by removal of the tab from the notch.

Despite the fact that most systems already have a hardware and software write-protect mechanism, the method here is useful for several reasons. CP/M includes a software write-protect mechanism that requires you to type Control C before writing on any newly inserted disk. However, the method does not allow you to write on one disk after inserting it into a drive while keeping a disk in another drive write protected. You can also accidentally defeat the software write protection. For example, if you remove a disk from drive B and replace it with a second disk, any file on the newly inserted disk can be erased simply by using the ERA command with the correct file name before reading the disk for any other reason.

Although the notch on most 8-in. disks does activate a hardware write-protect circuit that overcomes the problems of using the software write-protect mechanism, this feature is often awkward to use. It works well if you want to protect a disk for long periods between updates, but when developing programs or changing databases frequently, it's often desirable to write protect a disk for a short time, then remove the protection so you can update the disk's data. The awkwardness of removing the disk from the drive and then removing tape from the notch discourages short-term use of the normal hardware write-protect feature.

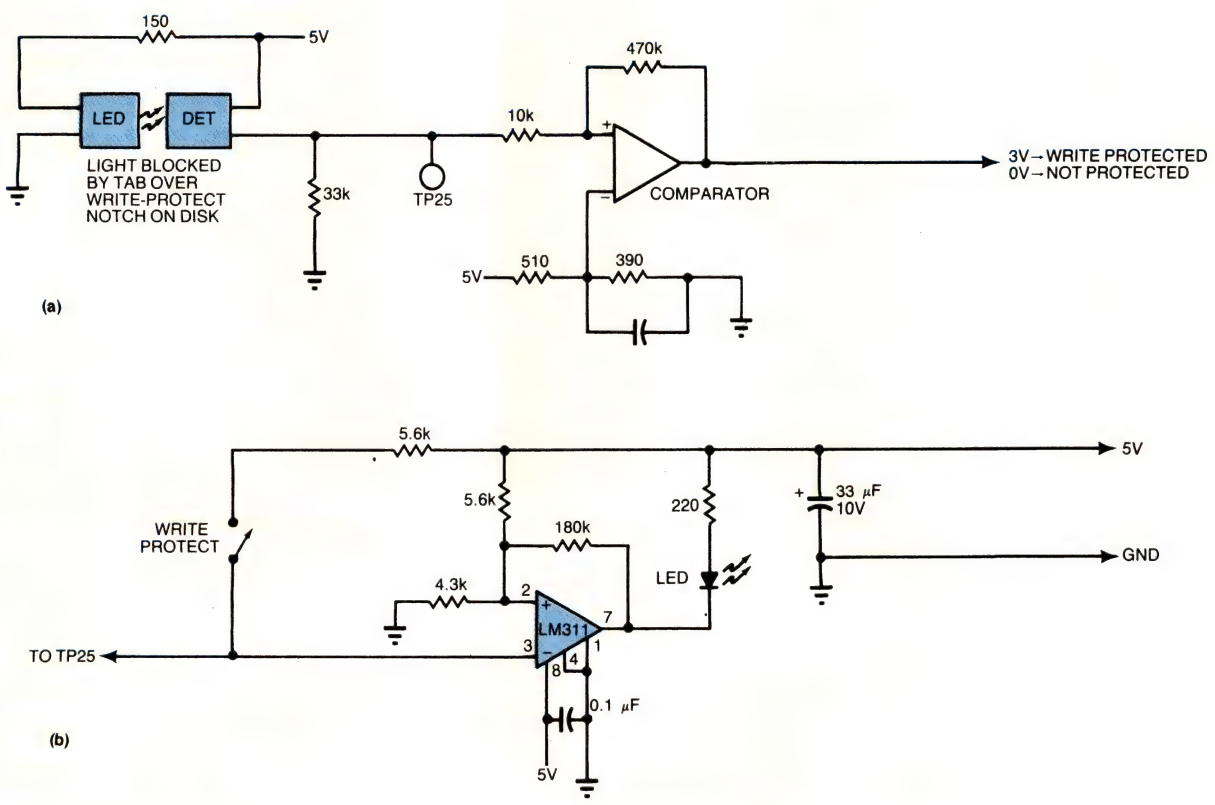
The **figure (a)** shows the write-protect circuit found in the two cited Shugart drives. An LED constantly directs a beam of light toward a nearby photodetector. If the disk's write-protect notch is covered (disk not protected), the light doesn't reach the detector. The detector resembles a high-value resistor when no light is present; a low-value one when it receives enough light. Therefore, the detector's output is nearly 5V for a protected disk, nearly 0V for an unprotected one. The comparator's output is Low whenever the voltage at its positive input is less than 2.2V and High otherwise. The 470-kΩ resistor provides a small amount of hysteresis to prevent comparator chatter.

The additional circuit needed to add a write-protect switch and indicator LED is shown in **(b)**. The only direct connection to the disk drive is through a connector to test point TP25 (the photodetector output). When closed, the write-protect switch simply pulls the detector output to nearly 5V regardless of the presence or absence of a tab covering the disk's protection notch. If you don't need a write-protect indicator, only this switch and the 5.6-kΩ resistor are required.

The LM311 comparator essentially duplicates the comparator circuit in **(a)**, except that the inverting and noninverting inputs are interchanged. Therefore, the LM311's output is Low and the LED lights when the disk is write protected. Note that the LED indicates the write-protect status of the disk regardless of whether the disk is protected through use of the notch or the added switch. Moreover, the added switch can protect an otherwise unprotected disk, but can not override a disk that's write protected through removal of its tab.

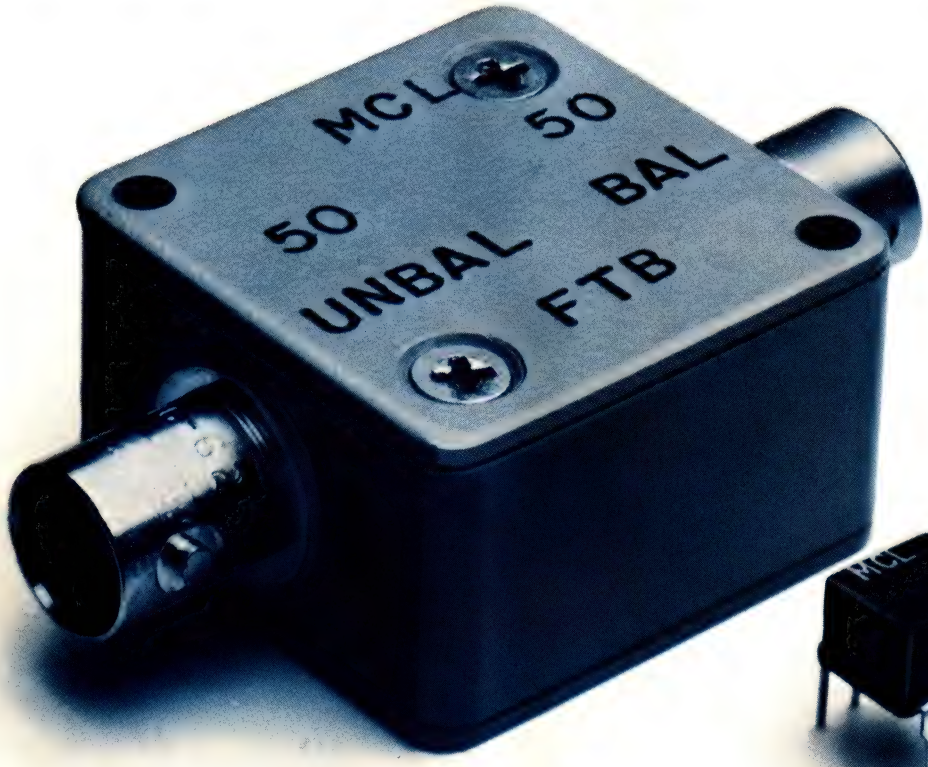
Test point TP25 is a pin the same size as a pin on a wire-wrap IC socket. Therefore, you can use a connector intended to mate with a wire-wrap pin to connect the add-on write-protect circuit without modifying the drive. The 5V supply is available from the drive's supply. You can build the comparator circuit on a small perforated board and mount it near the switch and indicator light, mounted on an unused section of the computer's front panel. **EDN**

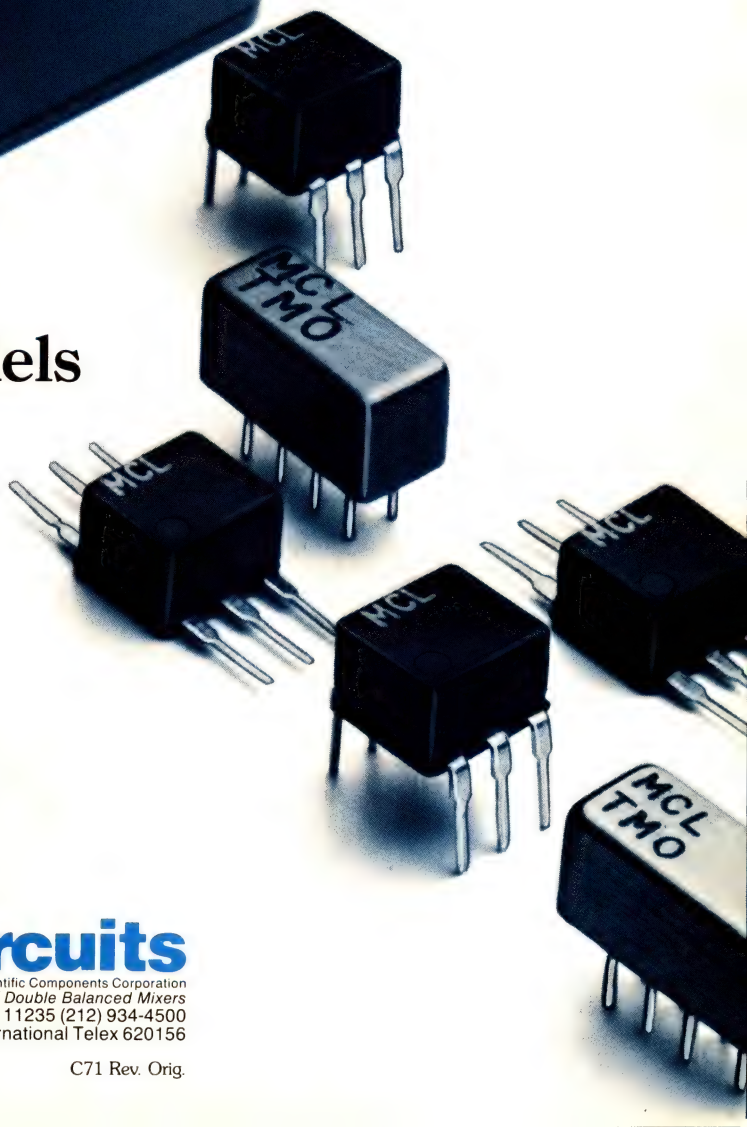
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CIRCLE NO 104

C71 Rev. Orig.

Algorithm converts BCD fractions to binary

V K Agrawal and S Murugesan
ISRO Satellite Centre, Bangalore, India

Although integer number conversions from BCD to binary are quite common, algorithms for fractional numbers are less well known. The **table** gives an example of the application of an algorithm that converts a D-digit fractional BCD number to the equivalent n-bit binary number. You can use either a μP or conventional logic circuitry to execute the routine.

The algorithm is based on repetitive multiplication of the fractional BCD number by two. It's performed by shifting each decade one bit left with carry from one decade moved to the one on its left, and by further correcting the digits for proper BCD representation. The unity-weight carry (after multiplication and correction) from the most significant BCD digit is also shifted left for each multiplication. After repeating this operation n times, the resulting carries from the most significant BCD digit correspond to the integer part of 2^n times the BCD data. Dividing this by 2^n (equivalent to simply placing the binary point to the left of the most significant binary digit) yields the fractional binary representation of the BCD number.

During multiplication of a BCD digit by two (by left shifting), if a one crosses a decade boundary, its relative weight becomes only 10 rather than 16. Adding six to that decade corrects the weight. Alternatively, you could add three to the decade prior to the shift, if its value is greater than or equal to eight. Another correction is required if the value of a digit after shifting is greater than nine, a situation that can arise when the decade value prior to shifting is from five to seven. This correction involves adding one to the next higher decade and subtracting 10 from (or adding six to) the current decade. You could also accomplish this before shifting, by adding binary three to a decade.

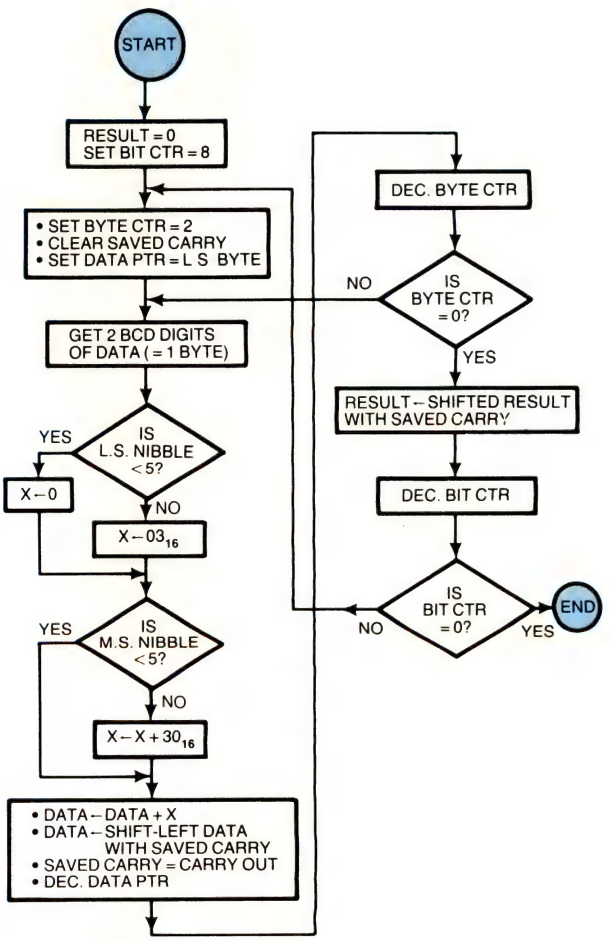
Both these corrections can occur jointly before shifting, for all the BCD decades simultaneously and independently, if you add binary three to a decade having a

FRACTIONAL BCD-TO-BINARY EXAMPLE

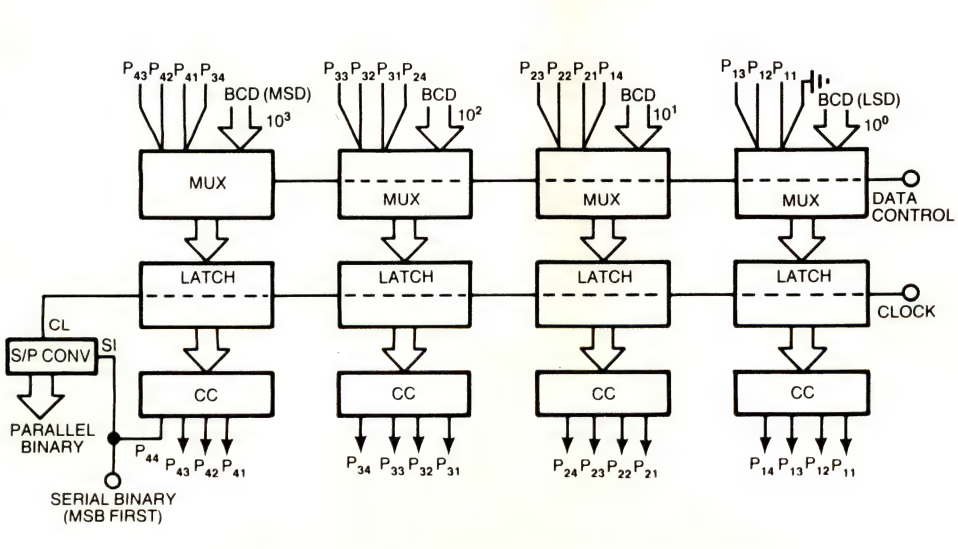
OPERATION	CONVERTED BINARY NUMBER	FRACTIONAL BCD DECADES		
		MSD, D_1 (10^{-1})	D^2 (10^{-2})	D_3 (10^{-3})
LOAD BCD NUM.	$b_1 \ldots b_6$ 000000	1000	0011	0010
1. A) ADD 3*	000000	1011	0011	0010
B) SHIFT LEFT	000001	0110	0110	0100
2. A) ADD 3*	000001	1001	1001	0100
B) SHIFT LEFT	000011	0011	0010	1000
3. A) ADD 3*	000011	0011	0010	1011
B) SHIFT LEFT	000110	0110	0101	0110
4. A) ADD 3*	000110	1001	1000	1001
B) SHIFT LEFT	001101	0011	0001	0010
5. A) ADD 3*	001101	0011	0001	0010
B) SHIFT LEFT	011010	0110	0010	0100
6. A) ADD 3*	011010	1001	0010	0100
B) SHIFT LEFT	110101	0010	0100	1000
RESULT	110101			

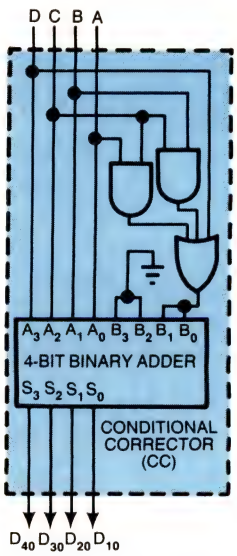
*ADD 3 TO EACH BCD DIGIT IF ITS VALUE, AFTER THE PREVIOUS STEP, IS GREATER THAN OR EQUAL TO 5.

CONVERTED BINARY RESULT $b = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4} + b_5 2^{-5} + b_6 2^{-6}$



```
0100                    ORG 100H                    ;START
0100 310002             LXI SP,200H                 ;SET SP
0103 1600               MVI D,0H                    ;CLEAR RESULT
0105 0608               MVI B,8H                    ;SET BIT CTR
0107 0E04       LB4:    MVI C, 2H                   ;SET BYTE CTR
0109 210003             LXI H,300H                  ;SET DATA PTR=LS BYTE
010C AFF5               XRA A!PUSH PSW              ;CLR CY & STR
010E 1E00       LB3:    MVI E, 0H                   ;CLR TEMP.REG.
0110 7E                 MOV A,M                     ;GET DATA
0111 E60F               ANI 0FH                     ;SELECT LOWER NIBBLE
0113 FE05               CPI 05H                     ; IF <05H
0115 DA1A01             JC LB1                      ; GOTO LB1
0118 1E03               MVI E,03H                   ; ELSE STR 03H IN TEMP.REG.
011A 7E         LB1:    MOV A,M                     ;SELECT UPPER NIBBLE
011B E6F0               ANI 0F0H                    ; OF DATA
011D FE507B             CPI 50H!MOV A, E            ; IF <50H
0120 DA2501             JC LB2                      ; GOTO LB2
0123 F630               ORI 30H                     ; ELSE,OR 30H WITH TEMP.REG.
0125 8677       LB2:    ADD M ! MOV M,A             ;ADD TEMP.REG.WITH DATA
0127 F17E               POP PSW ! MOV A,M           ;SHIFT LEFT WITH SAVED
0129 17F577             RAL ! PUSH PSW ! MOV M,A    ; CARRY,STR DATA &
                                                    ; SAVE CARRY
012C 2B0DC20E01         DCX H ! DCR C ! JNZ LB3     ;DEC DATA PTR & BYTE CTR.
                                                    ; IF <>0 GOTO LB3
0131 F17A1757           POP PSW ! MOV A,D !         ; ELSE STR RESULT
                        RAL ! MOV D,A
0135 05                 DCR B                       ;DEC BIT CTR
0136 C20701             JNZ LB4                     ; IF<>0 GOTO LB3
0139 76                 HLT                         ; ELSE STOP
013A                    END
```





Convert fractional BCD numbers to binary *with this method. The* ***table*** *gives an example of the routine; the* ***figure*** *shows a hard-wired circuit that does the job; the* ***flow chart*** *and* ***listing*** *illustrate a μP implementation.*

value greater than or equal to five. Thus, the conversion process is:

- Load the D-digit fractional BCD data into a register and clear the n-bit binary register.
- Independently perform the addition of binary three (0011) to each decade if its value is greater than or equal to five.
- Shift left one bit from all the BCD decades and the binary register, with the carry from one decade moved to the one on its left and the carry from the most significant BCD decade moved to the binary register.
- Perform the two preceding steps n times.

The binary register gives the equivalent binary fraction, with 2^{-1} and 2^{-n} weighting of the most and least significant bits, respectively. The **table** shows the conversion of the 3-digit BCD number 0.832 to its 6-bit binary equivalent 0.110101 (0.828125_{10}). Note that for certain BCD fractional numbers the exact binary representation might not terminate with a finite number of bits.

The **figure (a)** shows a hard-wired BCD-to-binary converter. It consists of multiplexers and a "conditional corrector" that adds three to the input if the latter is greater than or equal to five. The multiplexer selects the BCD data input to be converted (or corrected data, based on the MUX's control input) and feeds it to the latch. At the beginning of conversion, the MUX selects the BCD input and latches it, and the correctors perform their function. The corrected data loads back to the latches through the MUX at the next clock pulse, with a required skew of one bit (corresponding to the shift-left operation). This process repeats n times for an n-bit binary result. Finally, the **flow chart** and **listing** show the conversion routine for an 8080/8085 μP. **EDN**

To Vote For This Design, Circle No 749

Techniques simplify active filters

Manuel Cereijo
Florida International University, Miami, FL

The circuits in **(a)** and **(b)** provide easy approaches to the realization of biquartic bandpass filters and second-order allpass networks, respectively. A biquartic filter is a modification of the classic biquad circuit. To tune the biquartic filter shown in **(a)**, use the following procedure:

- Apply input signal V_{IN} at center frequency f_0.
- Detune the second integrator by connecting a 10-kΩ resistor across C_2 to obtain V_2.
- Tune the first integrator for a complete null at V_1, by adjusting its Q and resonant frequency via R_8 and C_5.
- Remove the detuning resistor from the second integrator and tune R_6 for a complete null at V_2. The full output now appears at V_3, even with f_0 null at V_1 and V_2.
- Adjust bandwidth by varying the integrator gains via R_1 and R_2.

The second-order allpass network shown in **(b)** is used to vary a system's phase characteristics without affecting signal magnitude. The allpass function is given by

$$T(s) = \frac{s^2 - s\frac{\omega_0}{Q} + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \quad (1)$$

$$T(j\omega) = \frac{(\omega_0^2 - \omega^2) - j\omega\frac{\omega_0}{Q}}{(\omega_0^2 - \omega^2) + j\omega\frac{\omega_0}{Q}}, \quad (2)$$

where

$$|T(j\omega)| = 1 \quad (3)$$

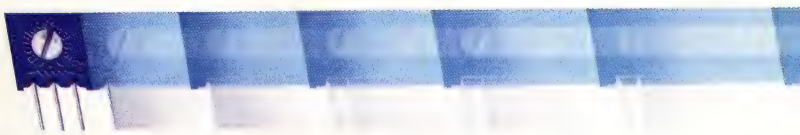
$$\text{Phase}\ (\omega) = -2\tan^{-1}\left[\frac{\frac{\omega}{\omega_0 Q}}{1 - \left(\frac{\omega}{\omega_0}\right)^2}\right]. \quad (4)$$

The main technique used to realize an active second-order allpass network is based on the following expressions:

$$1 - T_{BP} = 1 - \frac{K_s}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}, \quad (5)$$

where T_{BP} is the transfer function of a second-order bandpass filter. If $K=2\omega_0/Q$, then

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$$T(s) = \frac{s^2 - s\frac{\omega_0}{Q} + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}. \quad (6)$$

To design the allpass network, refer to (b). With the switch at position A,

$$V_{OA} = \frac{V_{IN}\, T_{BP}\frac{R}{k_1} + V_{IN}\frac{R}{k_2}}{\frac{R}{k_1} + \frac{R}{k_2}} \quad (7)$$

$$V_{OA} = V_{IN}\frac{T_{BP}\, k_2 + k_1}{k_1 + k_2} \quad (8)$$

$$\frac{V_{OA}}{V_{IN}} = \frac{k_1}{k_1 + k_2}\frac{s^2 + s\left(\frac{\omega_0}{Q} - \frac{k_2}{k_1}2Q\omega_0\right) + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}. \quad (9)$$

Adjust k_1 and k_2 so that

$$\frac{k_2}{k_1} = \frac{1}{Q^2}. \quad (10)$$

This yields

$$\frac{V_{OA}}{V_{IN}} = T_{AP} = \frac{Q^2}{1 + Q^2}\frac{s^2 - s\frac{\omega_0}{Q} + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}. \quad (11)$$

If the switch is at position B,

$$\frac{V_{OB}}{V_{IN}} = \left(\frac{1}{k_1 + k_2}\right)\frac{V_{OA}}{V_{IN}}, \quad (12)$$

which means that V_{OB} is actually a scaled form of V_{OA} in Equation 11. Next, select again

$$\frac{k_2}{k_1} = \frac{1}{Q^2} \quad (13)$$

and

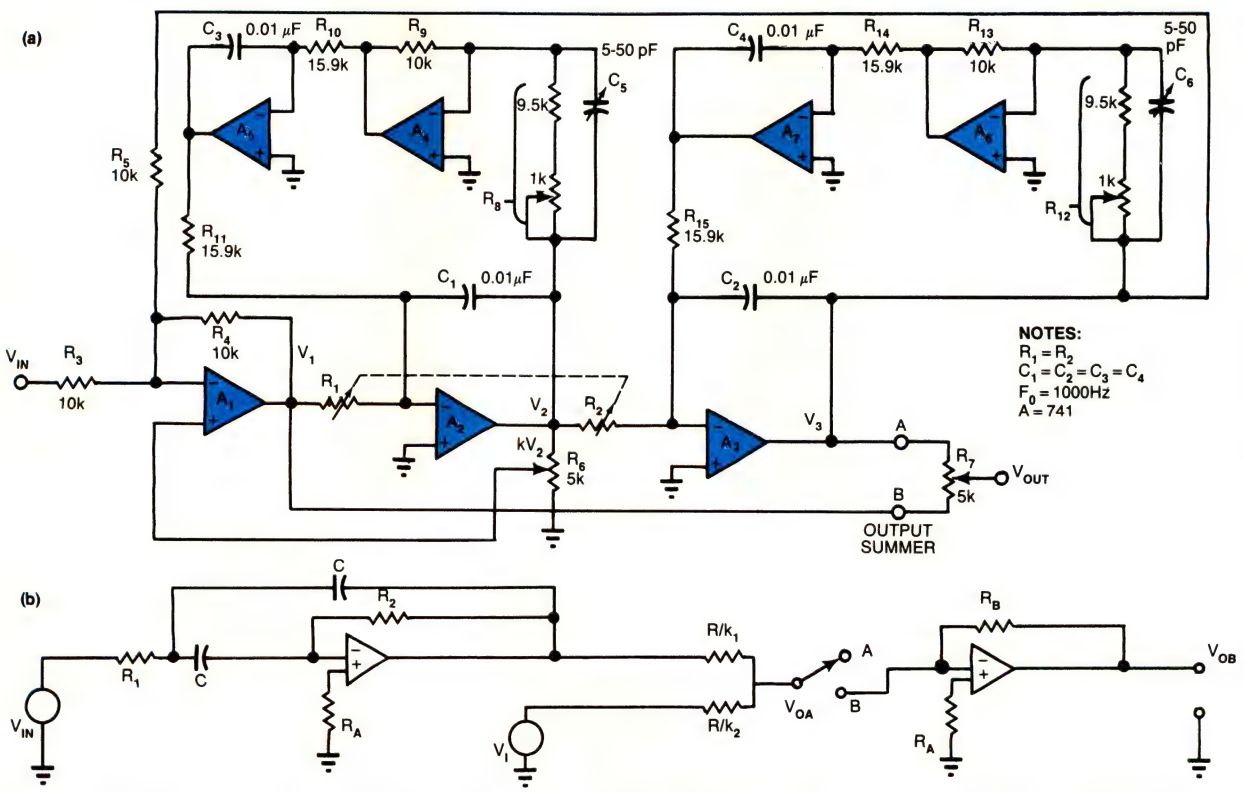
$$\frac{V_{OB}}{V_{IN}} = \frac{1}{k_1 + k_2}\left(\frac{Q^2}{1 + Q^2}\right)\left[\frac{s^2 - s\frac{\omega_0}{Q} + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2}\right]. \quad (14)$$

To conclude, to implement a second-order allpass active network, configure a second-order bandpass active filter. Then, adjust the potentiometers to obtain

$$\frac{k_2}{k_1} = \frac{1}{Q_2}.$$

EDN

To Vote For This Design, Circle No 747



Configure bandpass and allpass networks easily *with these circuits. The text gives procedures for both configurations.*

Who gets blamed when your applications grow and your single board computer doesn't?

Choosing a Single Board Computer (SBC) isn't easy. First, you've got to make sure that the SBC you choose is right for the job you're doing now. With enough speed, memory and flexibility to do what you want.

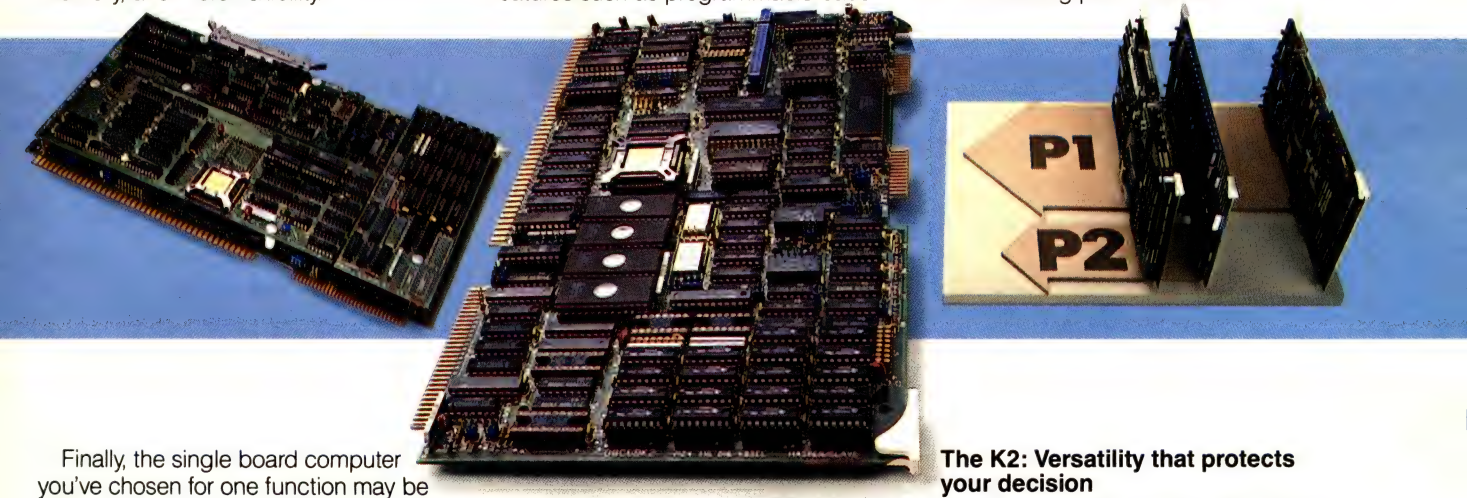
Next, you've got to make sure that you look far enough ahead, because what may have seemed like a simple enough application at the start can grow very quickly. Suddenly, you need more speed, more memory, and more flexibility.

Multimodule interface, capacity for 128K bytes of PROM, and Microbar's unique Dual Bus™ architecture. That's the basic DBC68K2, the K2.

You'll also get–standard with the K2–features such as programmable baud rates, two 16-bit timers, two RS232C serial ports with asynchronous and synchronous protocols, and dynamically-selectable byte-swapping and word reversing.

munication between the CPU and all that off-board memory on the P2 connector. With data transfer between memory and other processors handled on the P1 path.

Which means you can "add off"–add more memory boards that back up the K2's on-board memory. Or add other SBCs, with their own processors and memory, for very high-powered computing applications that demand multi-user, multi-tasking performance.



Finally, the single board computer you've chosen for one function may be called on later to handle completely different tasks as well–not just word processing, for instance, but graphics computation, communications, process control or data base management.

In other words, the computer that's at the heart of your system must be the right choice for now, the right choice as your applications grow, and the right choice as your applications change.

Begin with high performance

You won't go wrong starting with the powerful Motorola MC68000 microprocessor, in 10 or 12 MHz versions, 128K bytes of dual-ported on-board memory, the iSBX™

The K2: The SBC with Add-Ons

Then add on RAM modules that boost on-board memory to 256Kb or 512Kb, the SBX-compatible parallel I/O module from Microbar, or any of the wide variety of available SBX modules. And, you can add on your choice of memory management options–either a segment-oriented (68451) or 2-level page-oriented MMU. That means you can support high performance operating system software such as XENIX.™

The K2: The SBC that also "Adds Off"

Because of Microbar's clever use of the IEEE 796 bus architecture, you also get the advantages of direct high speed com-

The K2: Versatility that protects your decision

So if you've got the responsibility for choosing an SBC that's right for today's *and* tomorrow's systems, choose Microbar's DBC68K2. With its add-on and add-off flexibility, and its performance versatility, you'll know the K2's the board that will grow as your applications grow. Call or write **Microbar Systems, Inc. 1120 San Antonio Rd., Palo Alto, CA 94303, 415/964-2862, Twx: 910 373 2047**

MICROBAR SYSTEMS, INC.

iSBX is a trademark of Intel Corporation
Dual Bus is a trademark of Microbar Systems, Inc.
XENIX is a trademark of Microsoft Corporation

CIRCLE NO 106

FLOPPY SUBSYSTEM. The StacPac floppy subsystem provides 8-in. media for the Micro/PDP-11 and lets you transfer data between 8- and 5½-in. disks. The table-top system measures 3.25×14.08×16.25 in. Two RX02-compatible versions are available: the DS 100, a 0.5M-byte, single-sided drive with controller; and the DS 105, a 1M-byte, double-sided drive, also with controller. Units are available without a controller and can be daisy-chained for a dual-drive configuration. The DSD 4140 controller is compatible with the DEC RX02 dual-floppy subsystem and fits into any Q Bus backplane. It's transparent to DEC operating systems, back-up utilities, user-written applications and RX02 support diagnostics. It supports 22-bit addressing with an optional DSD software handler. Used with the DS 100 and 105 drives, the board's microcoded diagnostic routines can be invoked from a terminal to verify module operation and provide detailed status reports. DS 100, $1995; DS 105, $2295; DSD 4140, $1250. **Data Systems Design,** 2241 Lundy Ave, San Jose, CA 95131. Phone (408) 946-5800. TWX 910-338-0249.

Circle No 320

STORAGE SYSTEMS. The 895 disk storage system and the 7990 back-up storage system are compatible with Cyber 170 Series 800 computers. The 895 comes in two versions: the 895-1, which interfaces directly to the 7165 storage controller, and the 895-2, which attaches to the 895-1 to expand storage. A single controller controls as many as four systems. Each version has four independent disk spindles. Each spindle provides a sectored capacity of 2.4G bytes for a total of 9.6G bytes per system. Average disk seek time is 16 msec. Thin-film heads extend the recording density to 12.3M bits/in^2. The basic 7990 storage system includes a controller and storage module. Module capacity is 55G bytes, achieved with 175M-byte IBM-3850-type tape cartridges. Four modules can be connected to the controller for a total on-line capacity of 220G bytes. Model 895, $93,710; 7990, $460,000. All systems will be available in the 4th qtr of 1984. **Control Data Corp,** 8100 34th Ave S, Box 0, Minneapolis, MN 55440. Phone (612) 853-4253.

Circle No 321



IMPACT PRINTERS. The 5000 Series of daisy-wheel printers—the 25-cps 5025, the 40-cps 5040 and the 55-cps 5055—operate at a 50-dBA noise level and have built-in Centronics parallel and RS-232C interfaces. Each printer comes with a parallel printer cable and handles 132-column forms. The units use a specially designed printing wheel that furnishes as many as 125 characters on a single wheel. The print wheels for the 5040 and the 5055 are interchangeable. External software controls allow the units to print as many as 309 Teletex characters. Included with each printer is a daisy wheel, ribbon-cassette cartridge, paper guide and documentation. Model 5025, $799; 5040, $1675; 5055, $1990. **Amdek Corp,** 2201 Lively Blvd, Elk Grove Village, IL 60007. Phone (312) 364-1180. TLX 254786.

Circle No 322

GRAPHICS GENERATOR. The VP-2 stand-alone graphics/character generator includes a keyboard and micro disk drive. Resolution is 1510 pixels×483 lines. The color palette contains 512 colors, eight of which can be combined on a page. Any six fonts from the supplier's library of 45 fonts can be used simultaneously. You can perform individual character edging and full horizontal and vertical character overlapping. Other effects include palette animation at variable rates and background-color changes every two raster lines. Graphics pages from the disk memory can be called up and displayed at variable rates and in any sequence. The unit rolls a page at any of four speeds. Menus, prompts and cursor commands assist operation. An internal keyer allows superimposition of graphics over an input video signal. The unit locks onto any NTSC video signal. All video outputs are BNC-type connectors with signal levels spec'd to 75Ω termination. Standard output is NTSC. $7500. **Chyron Corp,** 265 Spagnoli Rd, Melville, NY 11747. Phone (212) 986-6668.

Circle No 323

HIGH-SPEED MODEM. The MP-192 SM is a voice-grade, 19.2k-bps modem with an integral statistical multiplexer. Aggregate speeds to 38.4k bps can be achieved over a single leased line (3002) with D1 conditioning. The modem provides eight or 16 channels of statistical multiplexing with a 2:1 max concentration ratio. It achieves a 1×10^{-6} bit error rate at a 28-dB S/N ratio for the 3-kHz bandwidth. An automatic adaptive digital transversal equalizer accomplishes channel equalization. For synchronous operation, the modem supports several protocols including BiSync (ASCII and EBCDIC), HDLC/SDLC (NRZ and NRZI), CCITT X.24 Level 2 and a transparent RTS/CTS mode. The modem accommodates synchronous speeds from 1.2k to 12k bps and asynchronous speeds from 50 to 9.6k bps. A command port allows an asynchronous ASCII terminal to initiate local and remote diagnostic tests and implement port configurations. $16,900 to $18,900. Deliveries begin in October. **Paradyne,** Box 1347, Largo, FL 33540. Phone (813) 530-2000.

Circle No 324

ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 8031 AND 8051 ALTERNATIVES.

Rockwell's R6500 single-chip family—including the R6501Q "Super Microprocessor" —offers available solutions to long lead times.

Models	R6501Q	R6500/11	R6500/12	R6500/1	R6500/41
ROM (x8)	—	3072	3072	2048	1536
RAM (x8)	192	192	192	64	64
I/0 Lines	32	32	56	32	23
Serial Comm.	UART	UART	UART	—	—
Counters	2 x 16	2 x 16	2 x 16	1 x 16	1 x 16
Expansion Bus	65K	16K	16K	—	4K
Interrupts External Internal Host	6 4 —	6 4 —	6 4 —	3 1 —	4 1 2
Standby RAM (mW)	12	12	12	35	—
Package	64-pin QUIP	40-pin DIP	64-pin QUIP	40-pin DIP	40-pin DIP
Replaces	8031	8051		8048/49	8041

In as little as six weeks, Rockwell International can deliver alternatives to the 8051/31, 8048/49 or 8041 families of single-chip products. Our field applications engineers are ready to answer conversion questions and Rockwell's development aids can provide an MDS II cross-assembler and in-circuit emulation hardware to aid in your redesign process.

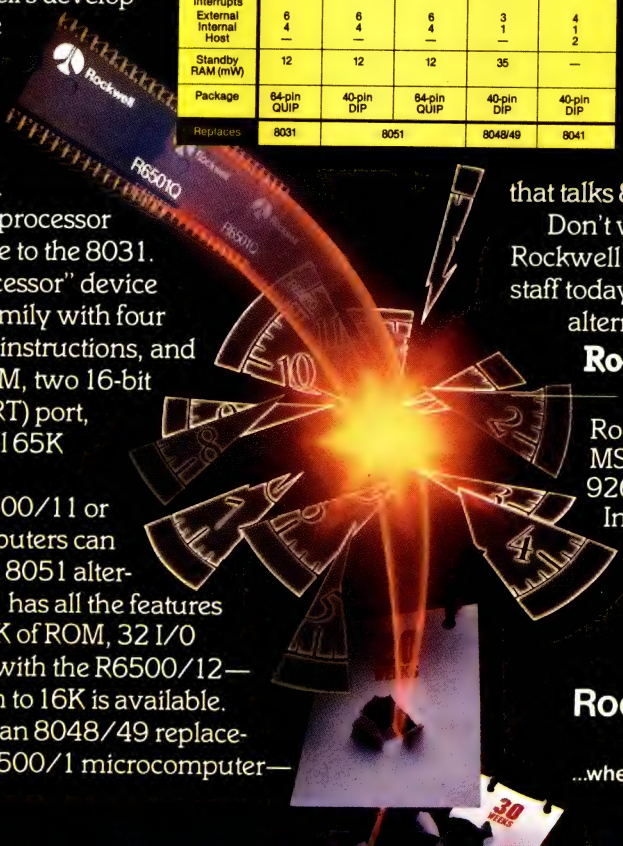
Our R6501Q microprocessor provides an alternative to the 8031. This "super microprocessor" device extends the R6500 family with four new bit manipulation instructions, and offers 192 bytes of RAM, two 16-bit counters, a serial (UART) port, 32 I/O lines, plus a full 65K address bus.

In addition, the R6500/11 or R6500/12 microcomputers can end your search for an 8051 alternative. The R6500/11 has all the features of the R6501Q, plus 3K of ROM, 32 I/O lines—or 56 I/O lines with the R6500/12—and address expansion to 16K is available.

If you're looking for an 8048/49 replacement, look into our R6500/1 microcomputer—its in over half the world's 5" hard disks. With 2K ROM, 64 bytes of RAM, a 16-bit counter and 32 I/O lines, it's ideal for moderate sized jobs.

And if you're waiting for an 8041 to off-load tasks from your central CPU, look at the R6500/41. It has 1.5K ROM, 64 bytes of RAM, a 16-bit counter, multiplexed address expansion to an additional 4K and a host that talks 8050/Z80 or 6500/6800.

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92660. Call Toll Free (800) 854-8
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CIRCLE NO 107

COPROCESSING SYSTEM. The ZIP 3216 array processor suits signal- and image-processing applications. Its dual processors operate concurrently, are synchronized in hardware and can be programmed together in a single-source program. The 29116 processor controls data flow, while a pipelined processor with a full ALU handles 16-bit computations at speeds to 20M floating-point operations/sec and 32-bit operations at speeds to 5M floating-point operations/sec. Software-development tools provided with the system run under MS-DOS, CP/M, UNIX and DEC operating systems, so array-processor programs can be written and debugged on computers ranging from IBM Personal Computers to VAX systems. Tools include a ZIP/C programming language and compiler, a linker, and a simulator/debugger that times and measures program efficiency. A library containing algorithms for I/O, arithmetic, and signal and image processing can be called from the user's program. The 3216 interfaces to the Multibus, Q Bus and VME Bus. $8000. **Mercury Computer Systems Inc,** Wannalancit Technology Center, 600 Suffolk St, Lowell, MA 01854. Phone (617) 458-3100.

Circle No 325

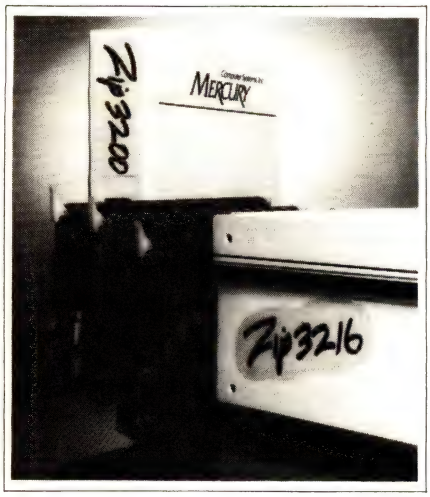


IMAGE PROCESSOR. The Model 794 real-time image processor digitizes and stores either 525-line, 60 Hz or 625-line, 50-Hz video signals. Its recursive-filtering feature improves the S/N ratio by taking a moving average of the input signal. The processor's 16-bit-wide memory can store 256 frames for image integration. Pictorial details are extracted from image data using a variety of arithmetic operations. For example, a stored reference image can be subtracted from an input image, and the resulting difference can be sent to a video monitor. Stored images can also be interspersed with live displays. The remotely controllable unit measures 6×17×20 in. and weighs 39.6 lbs. $15,000. **Hughes Image and Display Products,** 6155 El Camino Real, Carlsbad, CA 92008. Phone (619) 438-9191.

Circle No 326



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CIRCLE NO 108

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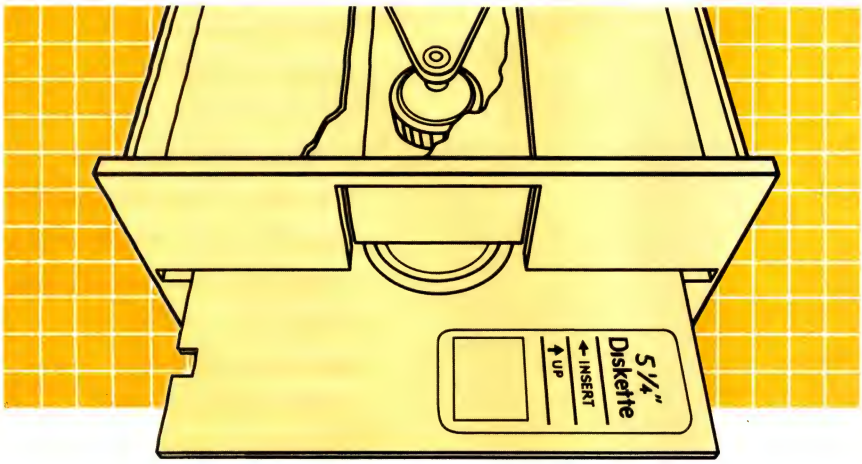
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CIRCLE No. 1 9

WINCHESTER-BASED μC. All configurations of this Q Bus-compatible, Winchester-based μC include the system enclosure, fixed or removable peripherals and LSI-11 processors and memory. Series 1000 Model 40 is DEC compatible and runs all systems and application software developed for the LSI-11/23 or LSI-11/73 CPUs without modification. A foundation module integrates the mass-storage device controller, two serial communication ports, all backplane circuitry and the Support Monitor Subsystem on a single board without requiring one of the backplane slots. You can customize the subsystem's user interface and operate it from the front panel or from a menu-driven console terminal. The system incorporates a quad-wide 22-bit Q Bus backplane with six free slots, and it emulates the DU handler/device driver via the mass storage control protocol (MSCP). Single or dual 5¼-in. Winchester-disk drives provide 12M to 70M bytes of capacity. Main memory ranges from 256k to 2.5M bytes. The μC supports real-time and timesharing operating systems, including RT-11, RSX-11M, RSX-11M+, RSTS/E, UNIX and TSX-Plus. From $5800. Delivery, 8 wks ARO. **Scientific Micro Systems Inc,** 777 E Middlefield Rd, Mt View, CA 94043. Phone (415) 964-5700.

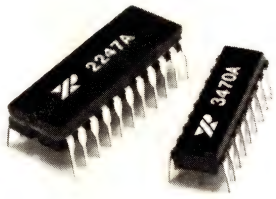
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WRITE AMPLIFIER ICs		
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Circle No 328

ROCKWELL SEMICONDUCTOR TECHNOLOGY BREAKS THE CMOS SPEED BARRIER.



Led by the R65C02 microprocessor, Rockwell's R65C21, R65C24, R65C51 and R23C64 are the latest members of our high-speed, low-power CMOS family.

500 ns instruction time is our CMOS microprocessors' record-breaking speed—two times faster than NMOS—with power consumption of only 80mW. And now Rockwell International offers peripheral devices such as the R65C21 (PIA), R65C24 (PIAT) and the R65C51 (ACIA) for your system design.

Our low-power, high-speed combination is not all you get from Rockwell's CMOS; you also get latch-up immunity, a bit manipulation and byte operation instruction set, power and temperature variance toleration, low noise generation, high noise immunity and a small die size. All these features combine to save you design time, lower your costs and improve system performance.

If all that doesn't convince you, write on your letterhead for a free sample of our R65C02 CPU.

(It's pin-and bus-compatible with the popular R6502). Using is believing.

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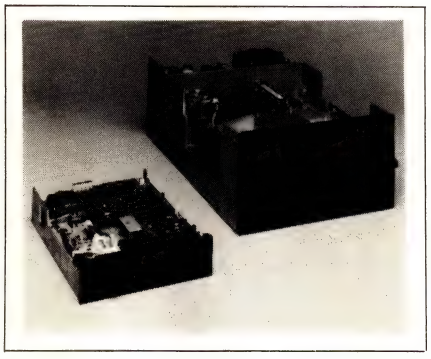
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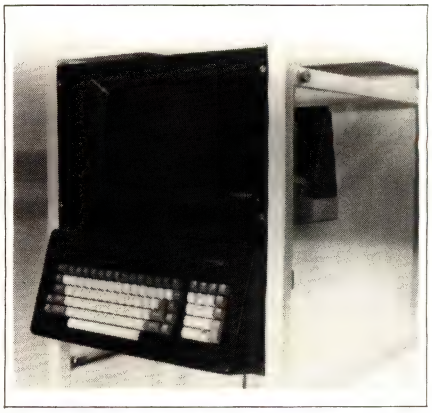
HARD-DISK SUBSYSTEM. Medley is a 5¼-in. Winchester-disk and ¼-in. cartridge-tape SCSI drive that provides transparent storage and back-up capability for users of the DEC Q Bus and Unibus computers. The subsystem is packaged in a desktop or standard RETMA rack-mount chassis (5.25×22×19 in.). The Winchester drive stores 36M or 110M bytes of formatted data, and the tape drive stores as much as 70M bytes. The subsystem is Q Bus or Unibus compatible with the appropriate host adapter (included in the subsystem package). The quad-wide UC02 adapter plugs into a single Q Bus slot and supports full 22-bit addressing. The hex-sized UC12 adapter plugs into a single Unibus CPU slot. Each adapter emulates the DEC Mass Storage Control Protocol (MSCP) and handles as many as four drives. The tape drive uses 3M cartridges and records data in streaming mode per ANSI X3.55-1977. Tape speed and density are 55 ips and 8000 bpi, respectively. From $9795. **Emulex Corp,** Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; in CA, (714) 662-5600.

Circle No 329



FLOPPY DRIVE. The Model 475 half-height disk drive stores 1.6M bytes on a double-sided, 96-tpi, 5¼-in. floppy disk. It has a data-transfer rate of 500k bytes/sec and a 3-msec track-to-track access time. The unit can also read data written on 48-tpi, 5¼-in. diskettes. For high-density storage, disks with 600-Oe coercivity, rather than the 300-Oe media currently used with most floppy drives, are required. To achieve the high transfer rate, the low-profile, brushless, direct-drive dc spindle motor revolves the spindle at 360 rpm. Power requirements are 12.5W active, 3.6W standby. Evaluation units are available now; volume deliveries begin 3rd qtr. Less than $200 (OEM qty). **Shugart Corp,** 475 Oakmead Parkway, Sunnyvale, CA 94086. Phone (408) 733-0100.

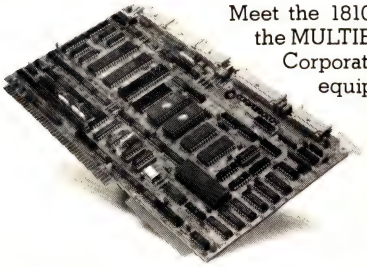
Circle No 330



RACK-MOUNT TERMINALS. This family of ANSI X3.64-compatible rack-mount terminals is available in RS-301C configuration for use in factory control systems and laboratory consoles. The family consists of Model 7 (2-pg, soft-key, soft-controls editors), Model 16 (4- or 8-pg, soft-key editors) and Model 100 (DEC VT102 and -131 block-mode editors). Each terminal comprises a display unit and keyboard assembly. The displays are 12-in. nonglare CRTs with a logic pc board and power supply, mounted in a 12¼×19-in. rack. The keyboard arrangement is panel mounted, with its key plane tilted approximately at 30°. A detachable keyboard with a 6-ft cable is optional. $1590 to $1900. Delivery, 5 to 6 wks ARO. **Teleray,** Box 24064, Minneapolis, MN 55424. Phone (612) 941-3300.

Circle No 360

MULTIBUS MOTOR CONTROL



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CIRCLE NO 112

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This mask-programmable 64K CMOS OM has an access time as fast as 150 ns, yet power dissipation is extremely ow—10mW active, 50µW passive—so t's ideal for your low-power application equirements.

And with our 24-hour code-pproval process and competitive lead nes, you get high-speed CMOS ithout a lot of waiting.

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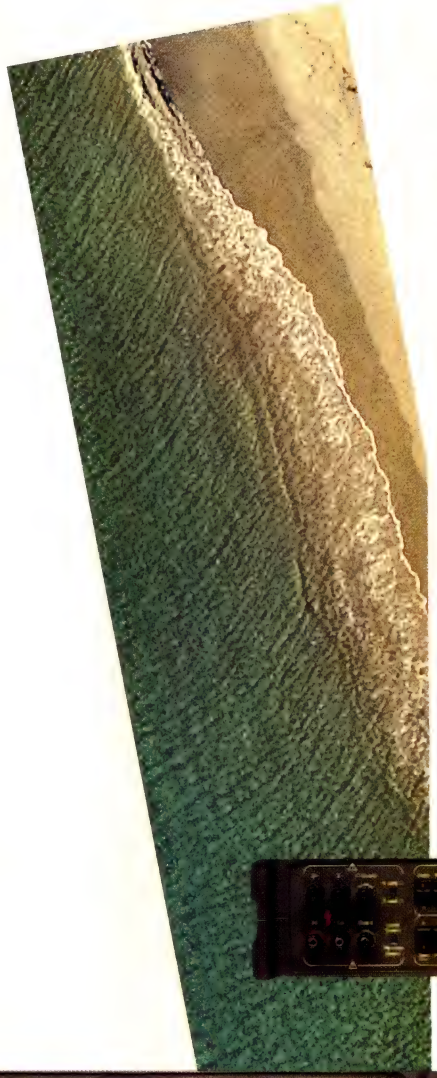
It exists in an imaginary world, of course. A world without temperature change or human error. A world without drift.

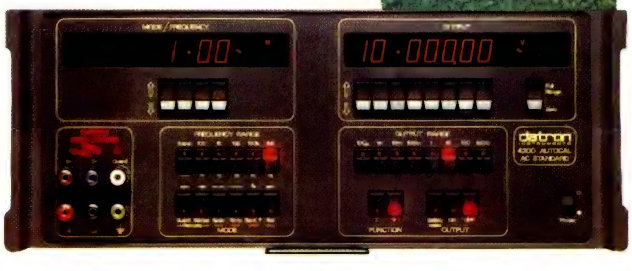
At Datron, we don't claim to have reached that perfect standard. We've merely come closer to it than anybody else. Which is why our precision calibrators and top-of-the-line digital multimeters can bring unprecedented levels of performance, accuracy and reliability to your Standards or Calibration Laboratory.

Consider Datron's AUTOCAL™ 4000 Series calibrators. Instruments that not only surpass anything else in their class, but which incorporate a number of unique design features that allow you to transport traceable Metrology standards out into a production environment where comprehensive calibration of any DMM is now possible.

Both our 4000 and 4000A DC Calibrators, and our 4200 AC Calibrator, feature AUTOCAL™, Datron's exclusive, all-electronic calibration technique which permits calibration of any Datron AUTOCAL™ instrument in a matter of minutes. With unparalleled "hands-off" and "cover-on" ease and exactitude.

For standard-setting performance, consider our solid-state 4200 AC Calibrator. It delivers twice the accuracy available in any other instrument. Providing performance up to 40 ppm on a 6½ digit scale, with output ranges from 1 millivolt to 1000 volts. AC current is optionally available.





But performance is no less critical when it comes to selecting a Standards Laboratory DMM.

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Datron's unique standard features include: AUTOCAL™, extended IEEE-488 capabilities and instant 'Spec' read-out, a patented technique for providing the limits of uncertainty. These features can be found in every Datron AUTOCAL™ Instrument. And nowhere else. Also standard is a no-nonsense, no-worry warranty which, on some of our instruments, gives you protection for five full years. A clear sign of our confidence and our commitment.

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Datron Instruments, Inc., 3401 SW 42nd Avenue, Stuart, FL 33497. Telephone: Toll-Free 800-327-0938. In Florida: 305-283-0935. Telex: 525724.

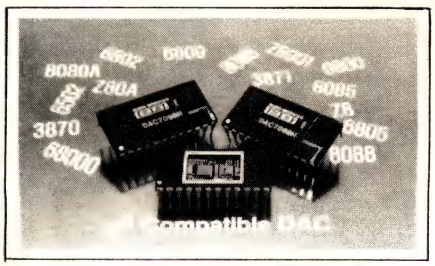
Datron Instruments, Ltd., Hurricane Way, Norwich Airport, Norwich NR6 6JB, ENGLAND. Telephone: Norwich (0603) 404824. Telex: 975173.

datron
INSTRUMENTS

THE AUTOCAL PIONEERS

Circle 196 for demonstration

Circle 197 for additional information

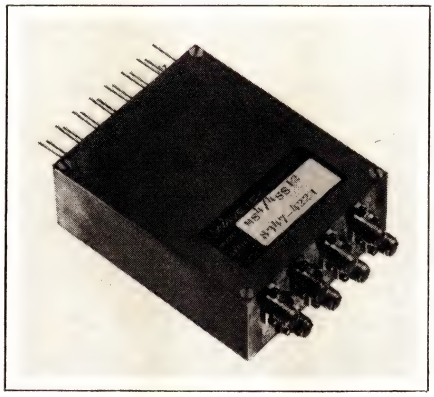


16-BIT D/A CONVERTERS. Incorporating built-in μP interfaces, Models DAC708 and -709 A/D converters feature maximum linearity error of ±0.003% FS reading. They are monotonic to 14 bits over their specified temperature ranges. KH models operate over 0 to 70°C and spec ±10-ppm/°C gain drift. BH versions accommodate −25 to +85°C operation and feature ±7-ppm/°C gain drift. The μP interface has two 8-bit input registers and one 16-bit D/A register, each with its own Enable line. An 8-bit data port connects to both high and low byte registers for 8-bit bus compatibility. Chip Select, Write and Clear control lines are available. Input data is loaded one bit at a time with each bit strobed by a write pulse. Bipolar input coding is two's-complement, and unipolar coding is straight binary with the addition of an external inverter on the MSB line. In bipolar output mode, the Clear control line zeros the input registers and sets the 16-bit D/A register to the input code that gives 0V at the outputs. Maximum differential linearity error equals ±0.006% FS reading, and settling time to ±0.003% FS reading measures 8 μsec for V_{OUT} units and 1 μsec for I_{OUT} models. From $44 (25). **Burr-Brown Corp,** Data Products Div, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 331

VME BUS CHASSIS. The DSSERCK20 VME Bus chassis accommodates 20 double-Eurosize boards. It comes in table-top and rack-mount versions and is supplied with two cooling fans and a switch-mode power supply, which provides 5V at 45A (1% regulation), ±12V at 10A, −5V at 4A and 24V at 4A. The mother board provides transfer rates to 20 MHz and a daisy-chain system for interrupt and arbitration. A key-operated power switch is at the back of the chassis, and a removable plate covers the rear connectors. Two half-height, 8-in. floppy-disk drives can be mounted on the 9- and 20-slot table-top versions. From $1995 (single qty). **Data-Sud Systems/US Inc,** 2219 S 48th St, Suite J, Tempe, AZ 85282. Phone (602) 438-1492. TLX 165788.

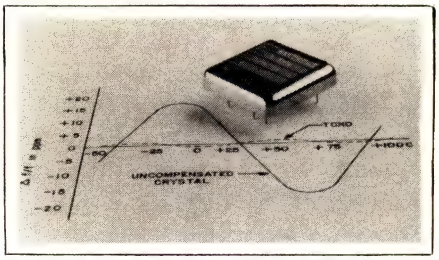
Circle No 332



MATRIX SWITCH. This 50Ω programmable 4×4 matrix switch operates over a dc to 1000-MHz frequency range. Insertion loss is less than 2 dB at 1000 MHz, and VSWR is less than 1.5:1 at 1000 MHz. Isolation is greater than 30 dB at 1000 MHz. Any of the four inputs can be individually connected to any of the four outputs. All unused ports are 50Ω terminated. The operating voltage is 5, 6, 9, 12, 18 or 26V. Power-handling capability equals 1W cw, and switching speed specs at 6 msec max. The switch operates over −55 to +71°C. The unit's connectors are SMA female for RF I/O and solder terminals for control. $695. Delivery, 8 wks ARO. **Wavetek Indiana Inc,** Box 190, Beech Grove, IN 46107. Phone (317) 788-5975. TWX 310-687-6033.

Circle No 333

HYBRID TCXOs. The Series CO-258 temperature-compensated crystal oscillator measures only



1.5×1.5×0.32 in. The RF circuit (oscillator, automatic gain control, buffer amp, and CMOS or TTL output device) is housed in a double-DIP resistance-welded case. The hybrid package is mounted on a pc board, which is housed in a solder-sealed case. The hybrid meets MIL-O-55310 requirements and is screened to MIL-STD-883. Its companion Series CO-259 measures 1.5×2×0.4 in., includes an internal mechanical frequency adjustment and provides for a TO-8-housed crystal to withstand severe shock and vibration. Both series have TTL outputs in the 20-kHz to 60-MHz range or CMOS outputs in the 400-Hz to 15-MHz range. From $243 (10). Delivery, 14 wks ARO. **Vectron Laboratories Inc,** 166 Glover Ave, Norwalk, CT 06850. Phone (203) 853-4433. TWX 710-468-3796.

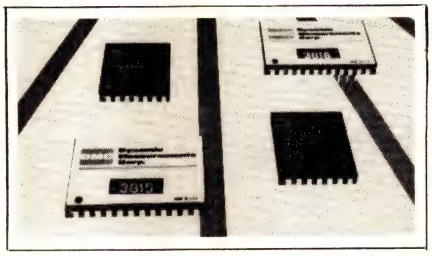
Circle No 334



MEMBRANE SWITCH. Featuring tactile feedback, the MCS Series switch has a built-in metal dome of chrome nickel steel with a partial gold coating that guarantees 1M operations min. Operating travel is 0.5 mm. Maximum switching current is 125 mA over a 5 to 48V range. Gold contacts can be ordered for voltages of less than 5V. The switch comes in seven colors for both bezel and actuator area. Legends with as many as

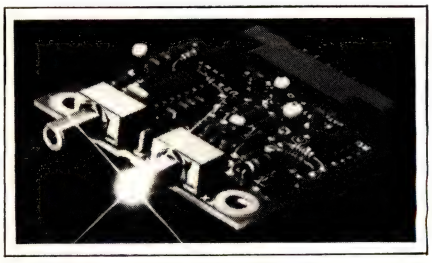
six letters can be silk-screened. Snap-in panel or pc-board mounting versions are available; additional mounting hardware provides a water-tight seal for the front panel. $1.16 (1000). Delivery, 4 to 6 wks ARO. **Schurter Inc,** 1016 Clegg Ct, Petaluma, CA 94952. Phone (707) 778-6311. TLX 176084.

Circle No 335



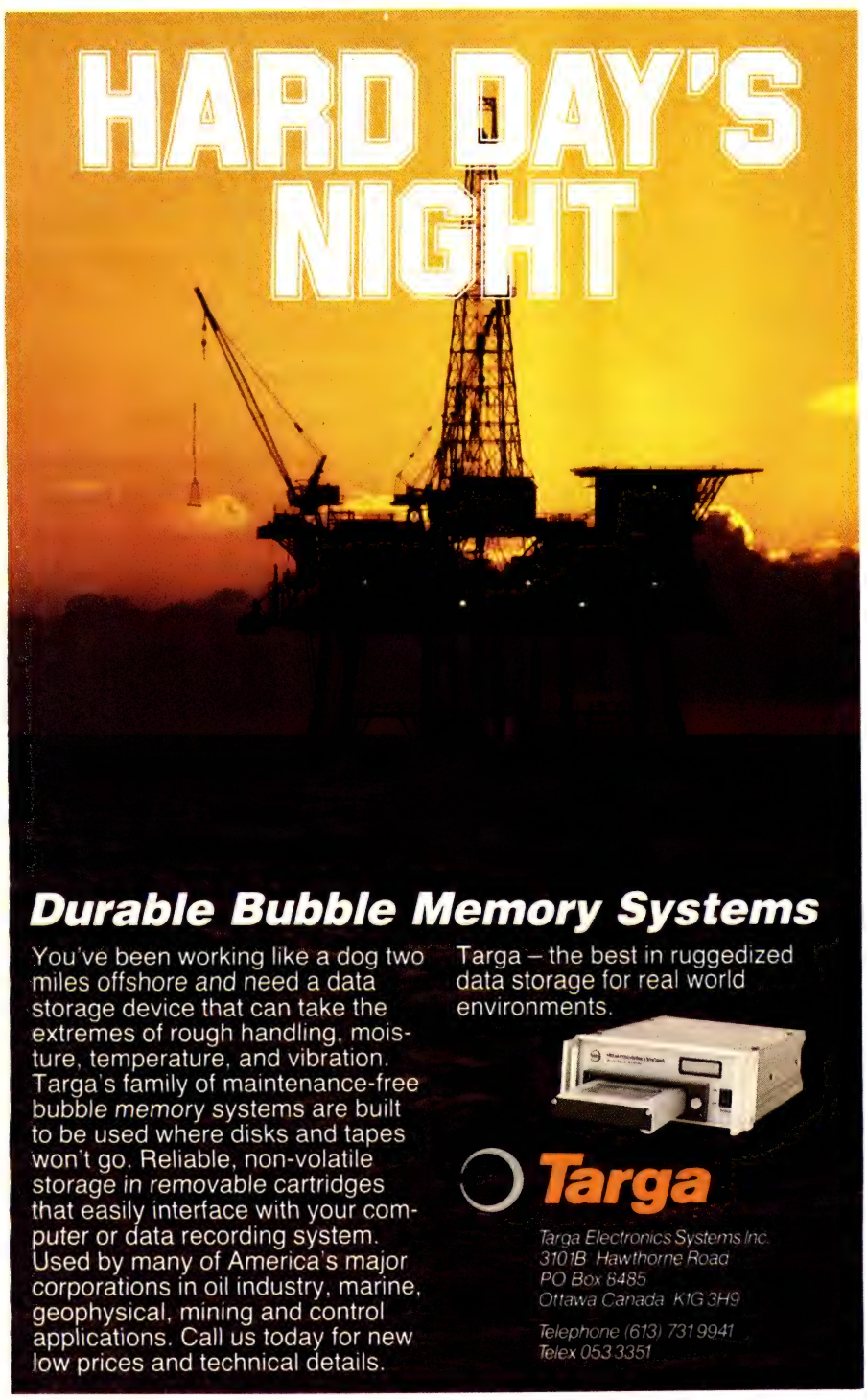
HYBRID V/F CONVERTERS. No external components are needed for these hybrid, self-contained, V/F converters. Systems of 10, 25 and 100 kHz are available in 14- and 24-pin packages. Each unit can be operated from a ±15V or a single +15V supply in either V/F or F/V mode. Linearity is guaranteed to within ±0.005%. 10-kHz version, $19 (100). **Dynamic Measurements Corp,** 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870. TWX 710-348-6596.

Circle No 336



F-O TRANSCEIVERS. These four transceivers are pc-board assemblies with HFBR-1201 and -1202 transmitters, HFBR-2203 and -2204 receivers and support circuitry for TTL I/O. The units' performance at 20M bps is guaranteed over 0 to 70°C. Although they're optimized for 20M-bps operation, the transceivers' board-mounted support circuitry can be optimized for other data rates. Featuring connectors made by the supplier, Model HFBR-0221 has a 33 to 67% duty factor and is for use with code schemes like Manchester and biphase; the similar -0222 version uses the SMA connector style. Model HFBR-0223 also uses the supplier's connectors and has a 5 to 95% duty factor to accommodate code schemes like NRZ and NRZI; the similar -0224 version uses SMA connectors. The devices can be mounted parallel or perpendicular to a reference pc board via an edge-card connector. A right-angle edge-card connector for parallel mounting is included with each transceiver. $175 (250). **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local sales office.

Circle No 337



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Welch Allyn HBD-E2.

Welch Allyn brings you a versatile method to track production and materials, control WIP, manage inventory and increase productivity. The HBD-E2 decoder family offers the compatibility, simplicity and accuracy you need to link manufacturing to management with real-time data.

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With four models in the line it's easy to integrate models into your data collection system.

You can use the basic E2 as a stand alone terminal or along with a CRT. The E2 DISPLAY DECODER features a highly visible 24-character display. In addition to the display, the E2 MINI-TERMINAL has a 57 key, full ASCII keyboard and four function keys.

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All E2 decoders read eleven codes and talk via RS-232-C, RS-422 or modified RS-485 Multidrop for maximum data management compatibility.

The easiest decoders to use.

Welch Allyn has made bar code terminal configuration easy. All you do is scan a bar code menu to read all or any of eleven codes, or program parity, baud rate, I/O format and more. Bright, readable displays, along with the adjustable beeper, verify data input.

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All E2 decoders come with Welch Allyn stainless steel, industrial scanners. Superior optics provide excellent depth of field for higher read rates and fewer non-reads. Plus, programming by scanning eliminates external switches and makes the E2 series the most tamper-proof decoders on the market.

Welch Allyn speaks your language.

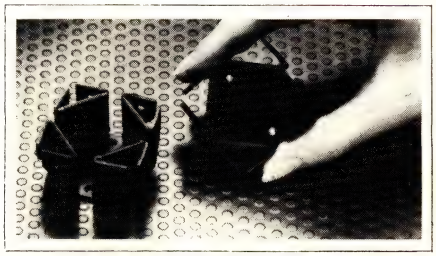
Whether you "speak bar code" or not, we can help solve your data collection problems with good products and good advice. For more data on our E2 series or applications assistance contact us today. Welch Allyn, Inc., Jordan Rd., Skaneateles Falls, NY 13153-0187, Tel. (315) 685-8351, TWX (710) 545-0203.

Welch Allyn

INDUSTRIAL PRODUCTS DIVISION

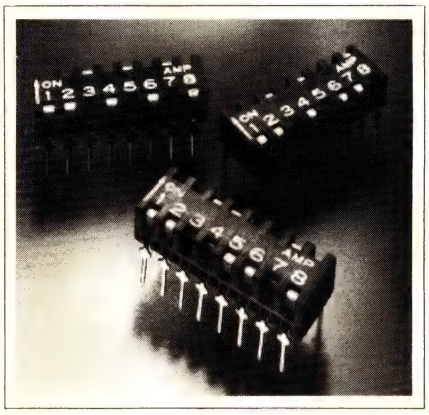
We Speak Bar Code

CIRCLE NO 115



EMI/RFI SHIELDS. These plated-steel enclosures for D-subminiature connectors provide EMI/RFI shielding and mechanical strength. Top- and side-entry versions fit 9- to 20-pin sizes. The 2-piece components can be opened for field service without disturbing the cable braid, which is terminated by crimping to provide mechanical strain relief and continuous shielding without solder or pigtails. Air-operated tooling is available for production, hand tooling for prototypes and field service. Custom ferrule diameters can be supplied to match precisely the user's cable diameter. Molded plastic shells are available in a variety of colors. A top-entry, 25-pin shield, $1.10 (1000). Delivery for custom products, 6 wks ARO. **Eldon Group America Inc,** 1 Westchester Plaza, Elmsford, NY 10523. Phone (800) 238-2388; in NY, (914) 592-4812.

Circle No 338



DIP SWITCH. Total compatibility with automatic IC-insertion equipment permits high-speed application of this permanently sealed, autoinsertable DIP switch. Integral sealing remains intact through the switch's 2000-cycle operational life and protects the gold-plated spring contacts from flux and environmental contaminants. For logic-level applications, the 4- and 8-position switches with standard 0.3×0.1-in. footprints provide spst and multipole/multithrow slide actuation with visual on/off indication. Thermoplastic housings, including the standoffs, stand only 0.21 in. above the pc board and are unaffected by wave-soldering techniques. Phosphor bronze tails 0.14-in. long, with tin/lead over nickel plating, accept a variety of board thicknesses. Switching capability equals 100 mA max at 6V dc. Contact resistance is 50 mΩ max initially, and 100 mΩ max after 2000 cycles with a resistive load of 24V dc and 25 mA. Maximum capacitance is 5 pF. **AMP Inc,** Harrisburg, PA 17105. Phone (715) 564-0100.

Circle No 339

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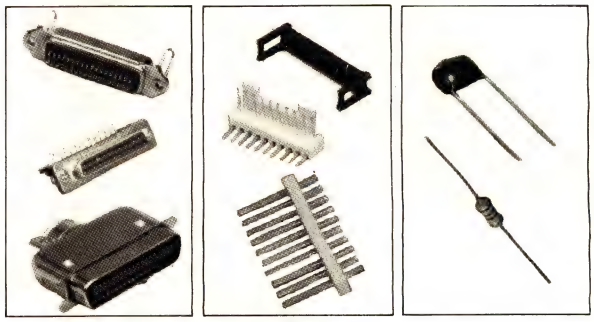
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CIRCLE NO 117



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Speed? Mine reads up to over 400 measurements/s. Its 2ns real-time clock gives higher resolution and speed than others.

Can you match all that? Only if you are already using the PM 6654.

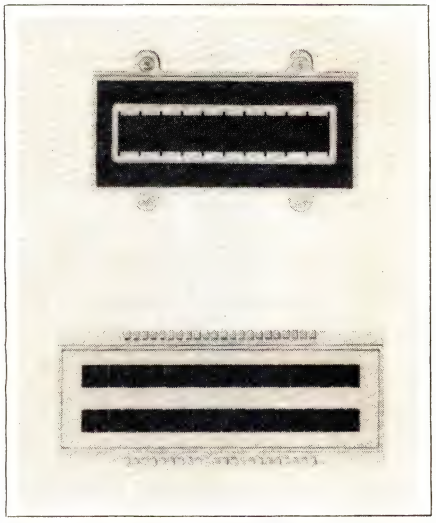
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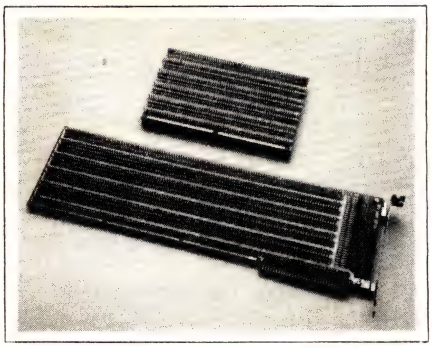
CIRCLE NO 118



BAR-GRAPH DISPLAYS. These LCD bar-graph displays replace mechanical meters and other display technologies in such applications as tape-deck VU meters and power-level indicators. The SP-539 comes with permanently attached pins or with conducting pads for use with elastomeric connectors and bezel assemblies. It measures 94×38 mm. Each bar measures 3.8×6.4 mm with 0.2-mm separation. Columns are 6.4 mm apart. The SP-533 is a true 1% bar graph with one column of 101 bars. Its viewing area measures 65×18 mm. The 0 bar and every 10th bar measure 12.7×0.5 mm, and the other bars are 13×5 mm. The diplay's overall 70×30.4-mm size makes it compatible with elastomeric connector and bezel assemblies. Both units operate over −10 to +60°C and require 3V for operation. SP-539, $8.30; SP-533, $5.70 (100). **Seiko Instruments USA Inc,** 2990 W Lomita Blvd, Torrance, CA 90505. Phone (213) 530-8777.

Circle No 340

PROTOTYPE BOARD. Model PC100 is an IBM PC/XT-compatible prototype board with 2-level wire-wrap pins on the component side. Its configuration uses no more space than a pc board and permits



mounting on a 0.5-in. slot spacing. The board accepts ICs with 0.3-, 0.6- and 0.9-in. pin centers. Extensive V_{CC} and groundplanes with uncommitted wire-wrap pins provide adjacent access to ICs and other components. Sixty I/O holes for right-angle, D-subminiature connectors are provided. For more circuit capacity, plug-in piggyback boards are available in four lengths. A full-size layout sheet is included to simplify component placement. $59. **Intercon Inc,** 11 Charlam Dr, Braintree, MA 02184. Phone (617) 848-9656.

Circle No 341

TUNABLE FILTERS. TCD Series bandpass filters generate continuous tuning without the reset problems of servo feedback. The devices are iris - coupled, 0.05 - dB Chebyshev-design cavities that come in 3- and 5-section configurations. Each section is capacity loaded to tune over a 2:1 frequency range. The filters are tunable over any one octave in the 32-MHz to 3-GHz band. A self-contained, μP-based control provides easy interface with the customer's digital system. The unit is automatically tunable to any center frequency within the range of the filter array. RS-232C, IEEE-488 and 8-4-2-1 parallel BCD interfaces are available. Standard bandwidth is 5% of center frequency, and tuning resolution is 0.5% of center frequency. $2400. Delivery, 6 to 8 wks ARO. **Telonic Berkeley Inc,** Box 277, Laguna Beach, CA 92652. Phone (800) 854-2436; in CA, (714) 494-9401.

Circle No 342





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CIRCLE NO 121

COMPONENTS & PACKAGING

PRESSURE TRANSDUCER. Serving low-pressure applications, the AR's accuracy is within ±0.25% from the best fit line, including the effects of nonlinearity, hysteresis and repeatability. Each unit is computer trimmed for temperature compensation, and calibrated to ensure unit-to-unit interchangeability of ±1%. A stainless-steel case and diaphragm provide immunity against corrosive media. Overpressure capacity specs at three times without damage and 10 times without bursting. The unit can be flush mounted or mounted to a variety of pressure port adapters. High-input impedance (400±100Ω) reduces power consumption. With an excitation level of 5 to 10V dc, the unit generates a FS output signal of 100 to 200 mV. $110 (100). **Data Instruments Inc,** 4 Hartwell Pl, Lexington, MA 02173. Phone (617) 861-7450. TLX 200081.

Circle No 385

HYBRID AMPLIFIERS. Incorporating silicon monolithic gain stages, Models GPM-552 and -1052 thin-film, cascadable modular amps cover 5 to 500 MHz and 5 to 1000 MHz, respectively. They feature 33-dB gains, 5-dBm output power and noise figures as low as 6 dB (4.5 dB typ). They're housed in hermetically sealed TO-12 transistor cans. Premium-performance Models UTM-1053, -1055, -1056 and -1057 cover the 5- to 1000-MHz range with gains as high as 27 dB, noise figures as low as 6.5 dB, 15 dBm of output power and gain flatness as low as ±0.2 dB typ at 25°C. They come in hermetically sealed TO-8 transistor cans. Models AGC-553 and -1053 have voltage-controlled gains ranging to 45 dB and 5 dBm output power. The 0 to 5V control signal is TTL compatible. GPM models, from $33; UTM models, from $136; and AGC models, from $175. **Avantek Inc,** 3175 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-6710.

Circle No 386

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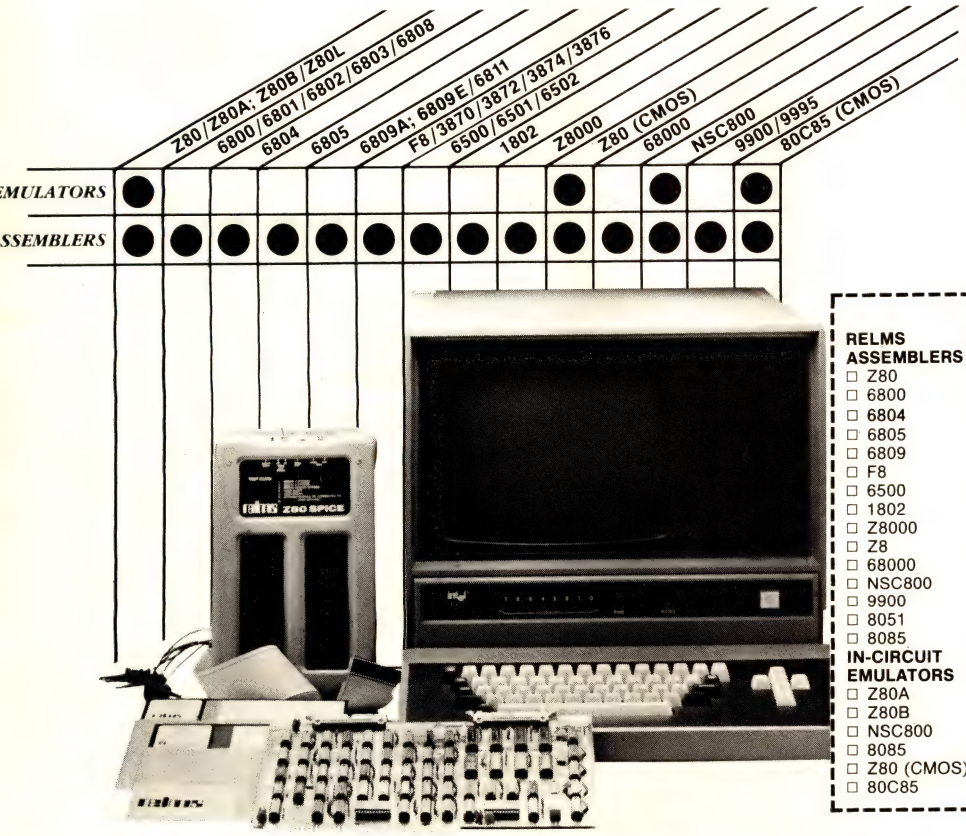
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DISK PRODUCTION. The Xeno-Disk Production System for the IBM PC/XT and compatibles reads, writes, formats and duplicates nearly 60 different types of 5¼-in. double-density disk formats without additional hardware. Eighty track formats are supported with appropriate disk drives. Running under PC-DOS/MS-DOS, each module is menu driven. Disk formats supported include most CP/M computers plus CP/M-86, TRSDOS 1.3, p-SYSTEM, NECDOS and European formats. Direct disk format parameter input allows use of 40- and 80-track CP/M formats not on the menu. An additional utility, Xeno-Sift, provides ASCII file filtering and processing to aid data file conversions. Optional utilities include 80Mate CP/M-80 emulator, which simulates a CP/M 2.2 environment under PC-DOS or MS-DOS, and the 80Term terminal emulator. These additional programs simulate a CP/M environment under MS-DOS and allow the user to run CP/M software before using Xeno-Disk to prepare distribution diskettes. Xeno-Disk, $379.50; 80Mate, $99.50; and 80Term, $44.95. **Vertex Systems,** 7950 W 4th St, Los Angeles, CA 90048. Phone (213) 938-0857.

Circle No 350

CIRCUIT ANALYSIS. S-Node, a linear circuit analysis program, uses a combination of Hewlett-Packard's 200 Series BASIC language and a compiled subprogram to solve circuits. Data is entered by component- and node-specifying statements. The program uses a sparse matrix-enhanced technique, written in a compiled subprogram, to increase solution speeds. After the circuit description is written, the user can use soft keys to produce graphs and tables. As many as five parameters can be tuned, or an automatic optimizer can be engaged to optimize a network. S-Node requires at least 750k of RAM and runs on HP calculators 9816, 9836A, 9826, 9836C. It requires BASIC 2.0 with BASIC enhancements 2.0 or 2.1. Circuit limitations are maximums of 30 nodes, 50 components and 100 frequency points. $475. **Suncrest Software,** Box 40, Veradale, WA 99037. Phone (509) 926-6691.

Circle No 351

REAL-TIME OS. MTOS-86, a real-time multitasking operating system for the 8086/8088, is available for the IBM PC or equivalent. It controls the PC and its peripherals including keyboard, disk drives, timer, interrupt controller and process I/O systems. The system allows attachment of custom drivers for special hardware and for configuring the user's application. MTOS-86/PC is distributed on diskette in PC format and includes an executive, console driver, debugger, run-time interface for the Intel C compiler, user manuals and test/demonstration program. MTOS-86/PC $495. Technical support $125/year. **Industrial Programming Inc,** 100 Jericho Quadrangle, Jericho, NY 11753. Phone (516) 938-6600. TLX 429808.

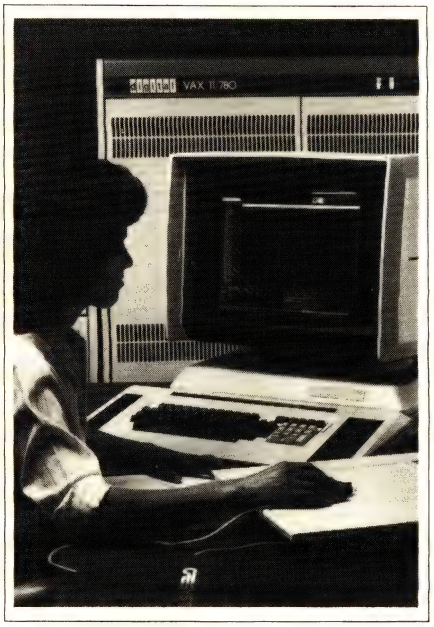
Circle No 352

PASCAL. The Pascal-286 compiler for the 80286 μP meets ISO standards for the Pascal language. The language is upwardly compatible with programs written in Pascal-86 for the 8086 μP, allowing programs written in Pascal-86 to be moved to systems employing the more powerful 80286 μP. The consistent format of object (or machine) code produced by the language and the manufacturer's other 286 translators (PL/M-286 and ASM-286) lets users develop programs using a mixture of languages. The language's extensions increase program efficiency. In addition, the compiler automatically marks where nonstandard features occur with flags. PASCAL-286 supports the IEEE standard and operation of the 80287 numerics coprocessor. $3900. **Intel Corp,** Literature Dept I-11, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle No 353

C CROSS COMPILER. BSO/C, an optimizing Motorola 68000 compiler for the DEC VAX, conforms to the Kernighan and Ritchie standards for C. Its extensions make it a systems implementation language permitting easier C language programming for embedded μP systems and applications. Features include built-in optimization functions, interrupt and I/O functions, a run-time math function library, an operating-system interface that permits interface to any operating environment, recursive and reentrant code programming capability and symbolic debugging support. $5000 with assembler and debugger. **Boston Systems Office,** 469 Moody St, Waltham, MA 02254. Phone (617) 894-7800. TWX 710-324-0760.

Circle No 354



WORKSTATION SOFTWARE. CAE/2000 VX computer-aided-engineering software for VAX computer systems runs under either the VAX/



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VMS or Berkeley UNIX 4.2 operating systems. Features include a multiuser distributed database, hierarchical command menus, pop-up menus, multiple overlapping viewpoints (windows), templates and menus, user-defined macros, self-explained English commands, and command summary explanations. A schematic capture package permits capturing, manipulating, and managing electronic designs. The package can be interfaced with the VAX-11/750 and 780 32-bit computer systems. Interfaces include HILO, SPICE, TEGAS and the manufacturer's IDEAL. The package supports Megatek 1645, 1650 and 7250 graphics terminals. Each supports local graphics display list processing via an RS-232C communications line to a VAX at a maximum of 19.2k bauds. $45,000. **CAE Systems Inc,** 1333 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 745-1440.

Circle No 355

SCREEN MANAGEMENT. TIFORM/PC, a form-based screen management utility, reduces development time for Professional Computer software by simplifying screen design. Compatible with TIFORM 990 for the manufacturer's Business System Series, the package allows screen formats in applications programs to be migrated from Business System minicomputers to the Professional or Portable Professional Computers and provides essentially the same screen-development capabilities as TIFORM 990. Form design determines the fields layout on the screen, the type of data accepted within each field and any post-processing that occurs. The utility's generation of common screens for Professional Computers and Business System computers makes it useful in environments that use both. It allows a choice of eight colors or monochrome intensities for each field or mask on the screen. The system includes interfaces for RM/COBOL 1.5, MS-Pascal 3.01 and MS-FORTRAN 3.04 and requires MS-DOS, 192k bytes of RAM and two disk drives. $400. **Texas Instruments,** Data Systems Group, Box 402430, Dallas, Texas 75240. Phone (800) 527-3500.

Circle No 356

MAIL MESSAGING. Electronic-mail messaging packages ComNet-8 and ComNet-16, and complementary inter-network communications packages ComNet-8N and ComNet-16N, are for 8- and 16-bit μCs. Both operate with either a multiuser μC or within a LAN environment. ComNet-8 supports CP/M; ComNet-16 supports CP/M-86 and MS-DOS. All packages are written in C, permitting transfers to most networks and computer environments. Both provide a keyword la-

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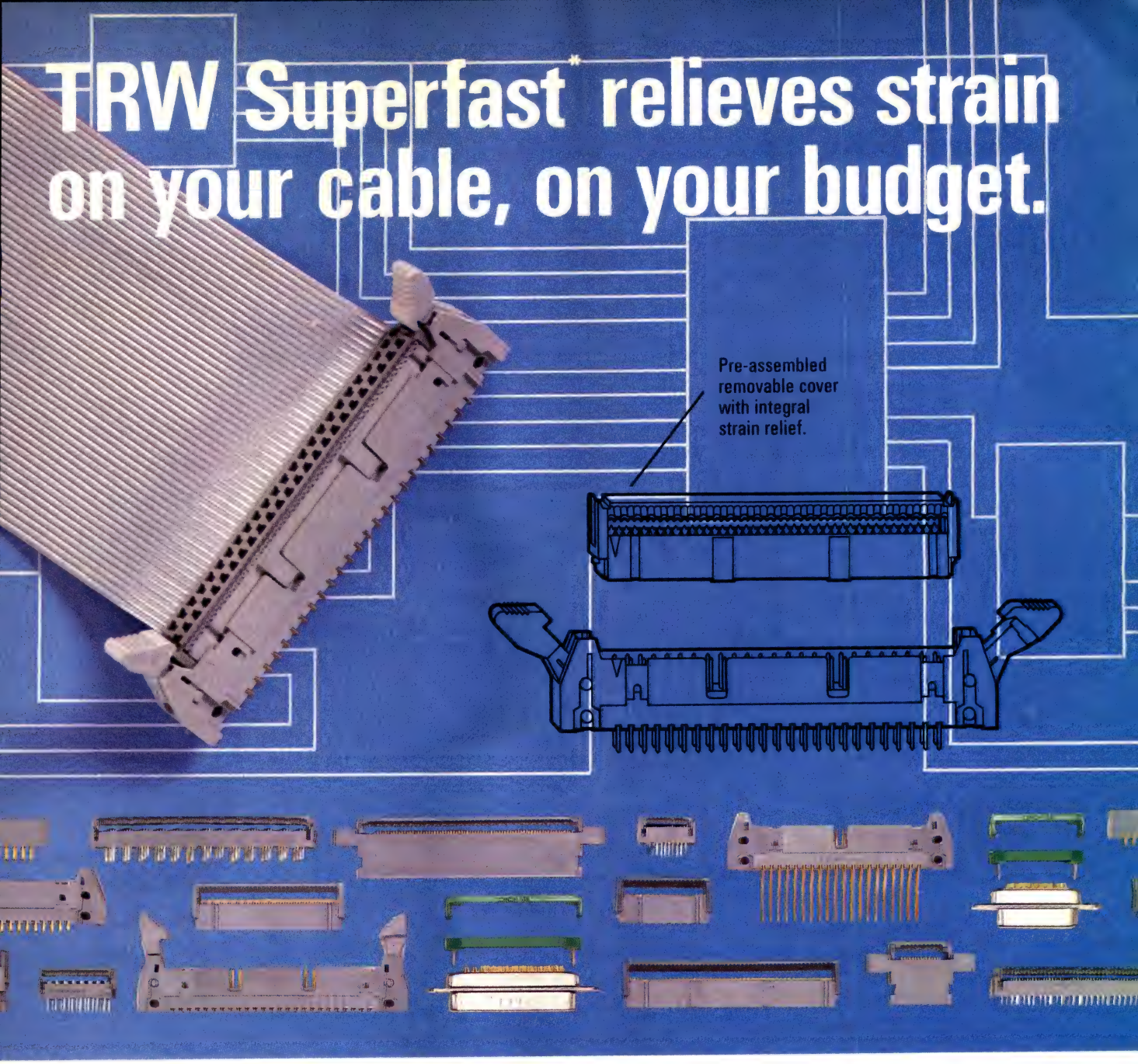
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CIRCLE NO 125

Connector Division
TRW Electronic Components Group

beling system for easy identification of messages, distribution lists, name aliases and codes to identify a message's status: unread, answered, unanswered, deleted, copied or filed. Together the packages handle mail and allow access to other networks via hardwire, telephone/modem links or standard gateways. ComNet-8 and ComNet-16, $395 each. ComNet-8N and ComNet-16N, $495 each. **Action Technologies Inc,** 1804 Broadway, San Francisco, CA 94109. Phone (415) 775-9396.

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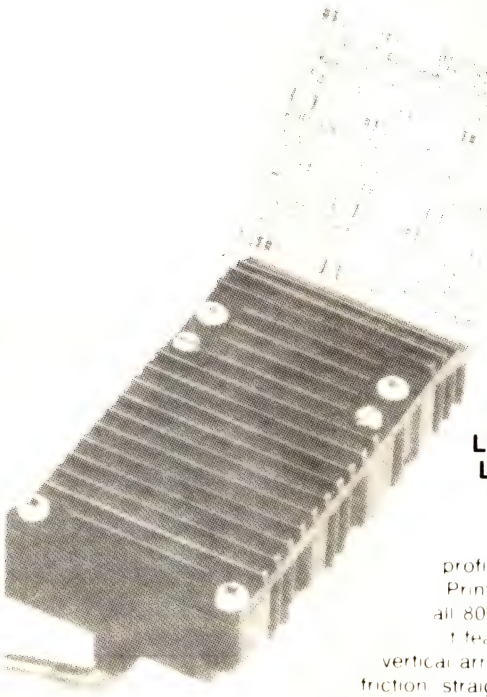
GRAPHICS PACKAGE. Four graphics systems for the Advanced Personal Computer (APC) meet a variety of graphics needs. Each contains a graphics software package, an APC graphics subsystem (graphics board), and 128k bytes of user RAM. The Analyst includes CP/M-86, GraphPlan and a printer. The Executive includes Context MBA and a printer. The Presenter comes with the Screen Shooter with Polaroid camera; its screen-oriented version uses Videograph and is used for producing slide presentations, and its plotter-oriented version uses Graphwriter and generates paper copies and overhead transparencies. The Designer uses Autocad software with input via keyboard, mouse, or digitizer and output via pen plotter. With APC purchase, each package in monochrome costs $848; in color, $998. **NEC Information Systems Inc,** 1414 Massachusetts Ave, Boxborough, MA 01719. Phone (617) 264-8000.

Circle No 358

KEY DEFINITION. SmartKey II Plus, an enhanced version of the SmartKey II keyboard-redefinition program, provides users of the IBM PC or compatibles a keyboard-definition display visible at the bottom of the computer's display while a key is being redefined. The display scrolls either vertically or horizontally and accommodates any number of characters. Users can assign a series of characters or commands to any key on the keyboard, thus eliminating the need for repetitive typing. Each key can take on seven different definitions. With a word processing program, SmartKey II Plus lets a personal computer function as a dedicated word processor using specially defined keys to perform routine functions. The package requires 4k of memory. $89.95. Owners of Smartkey II can upgrade to SmartKey II Plus by sending the original disk and $20 for shipping and handling to the company. **Software Research Technologies,** 3757 Wilshire Blvd, Suite 211, Los Angeles, CA 90010. Phone (213) 384-5430.

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MICROWAVE COUNTER. The Model 2440 counter provides 3-channel frequency measurements from 10 Hz to 20 GHz. It displays measurements on a 9-digit LCD. You achieve resolution to the full nine digits automatically in normal use, or you can set it manually to 0.1 Hz over the full range. The display rate adjusts from 11 msec to 20 sec. Microwave-acquisition time is typically 20 msec. The instrument can make measurements in the presence of as much as 30-MHz peak-deviation FM and 40% AM depth. £3750 to £3950. Delivery, 8 wks ARO. **Marconi Instruments Ltd,** Longacres, St Albans, Herts AL4 0JN, UK. Phone (0727) 59292. TLX 23350.

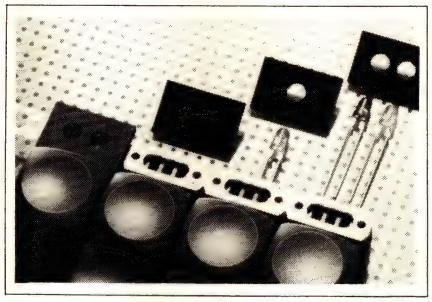
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HV DIGITAL VOLTMETERS. The 50/5 high-voltage systems DVM is available in two versions, measuring to ±65,536 and ±131,072V with 5 and 5½ digits plus polarity, respectively. Measurement rate for both instruments is 1.66 readings/sec. Resolution is either 0.1 or 0.2V, and input impedance is 6.5 or 13 GΩ. The IEEE-488 bus-interface address can be set from 0 to 15. 7480 or 9870 DM, depending on version. **Heinzinger,** Happingerstrasse 71, 8200 Rosenheim, West Germany. Phone (08031) 64141. TLX 0525-777.

Circle No 362

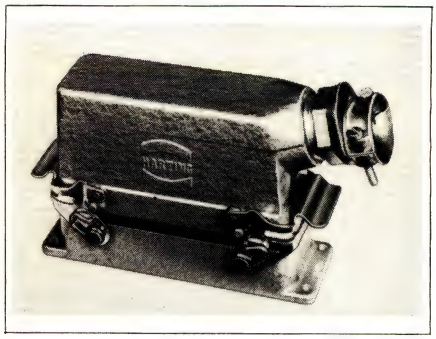
2.5-kW HV SUPPLY. The OL Series of high-voltage power supplies incorporates remote-control facilities and the output protection needed for ion-implantation and other rugged applications. Output power is 2.5 kW max. The supply comes in a 10.5-in.-high, 19-in. rack-mounting enclosure, with a 7-in.-high section for the high-voltage part, which is air-insulated. Available outputs range from 1 kV at 2.5A to 30 kV at 80 mA. The front panel includes twin meters for voltage and current monitoring and 10-turn potentiometer output controls. The supply can operate in current-limit or variable-trip modes. Line and load regulation figures are both 0.1%. Ripple is 0.5% at full load, and the standard temperature coefficient is 300 ppm/°C, with better values available. Approximately £3500. Delivery, 8 wks ARO. **Wallis Electronics Ltd,** Dominion Way, Worthing, West Sussex BN14 8NW, UK. Phone (0903) 211241. TLX 877112.

Circle No 363



KEYPAD MODULES. Intended for pc-board mounting, Albis 82 key-assembly modules allow you to build keypads of any required size. The keys have a normally open contact and come with or without LEDs. They fit on a 0.1-in. grid and have a service life of more than 10^6 operations. You can fit one or two 3-mm LEDs. You insert the indicators into a mounting strip that directly attaches to the key assembly. The contact system comprises a moving contact member made of conductive elastic material, which is gold plated in the dust and splash-proof area. The modules can be protected against ESD by placing a conductive strip over the diode mounting. **Siemens AG,** Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2341. TLX 0523121.

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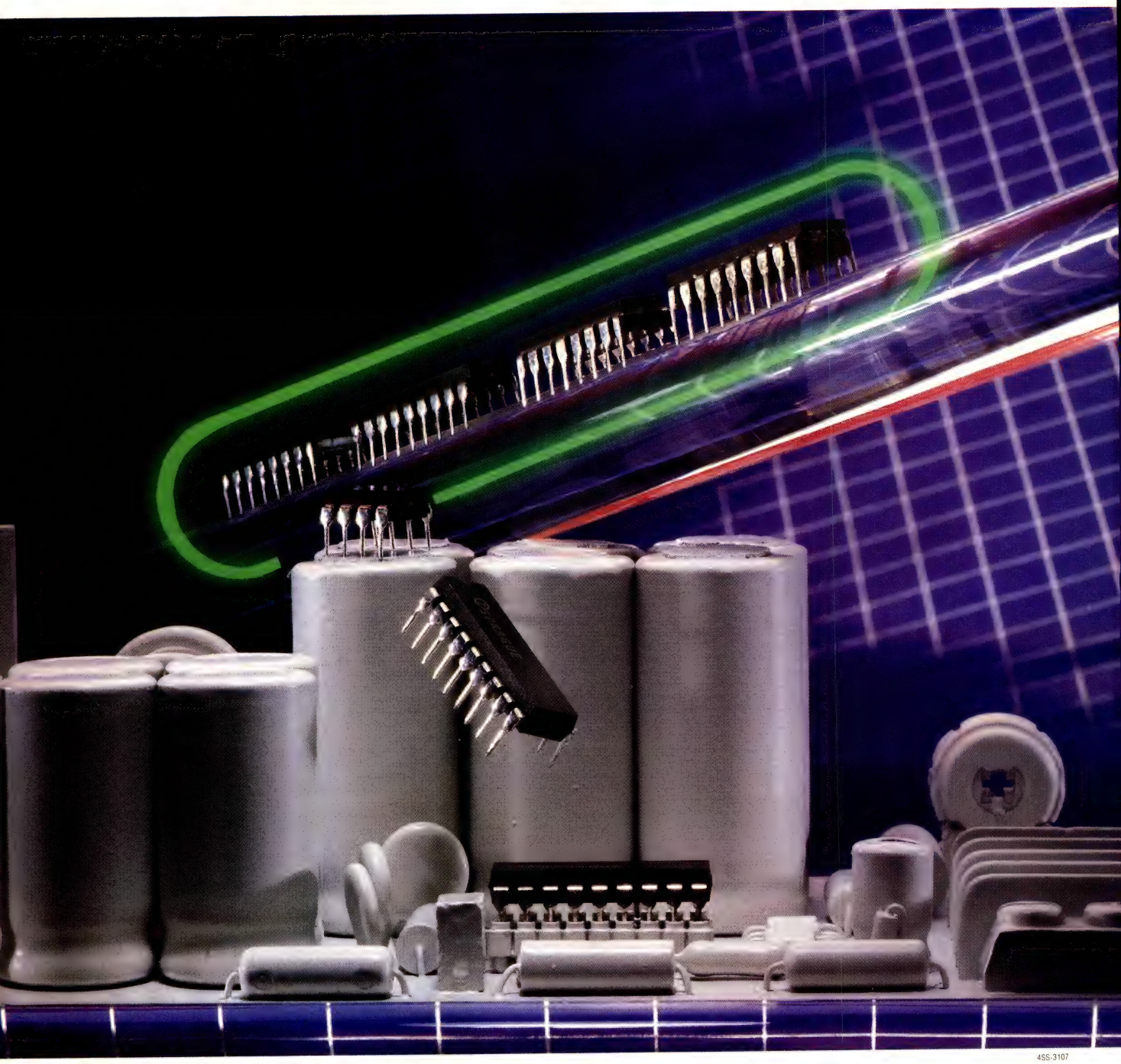
CONNECTOR HOUSING. Providing protection against splashes, Han 24E and 64D alloy housings fit over DIN-41612 connectors, allowing the DIN connectors to be used throughout a system. Guide pins and sockets ensure that the housing clips together without instability or inadmissable inclination. Two connectors can be mounted in a single housing. 3.72 to 6.30 DM (without contact elements), depending on configuration. **Harting Elektronik GmbH,** Postfach 1140, 4992 Espelkamp, West Germany. Phone (05772) 471. TLX 97231011.

Circle No 365

SILICON COMPILER. Dedicated to CMOS designs, the Chipsmith automatic silicon compiler runs on the Apollo Domain workstation and a variety of other computers, including VAX systems, IBM's 4300, or Perkin-Elmer's 3200. Input is accomplished via the company's MODEL design language. Once a logic design has been compiled into an intermediate design language, it can be evaluated on the switch-level simulator, EXERT. The compiler is a new version of the previous GATT software, and it can be used in both gate-array and standard-cell designs. It has a back end that produces complete mask-making artwork, which is compatible with most popular machines, including Electromask, Ebeam and David Mann 3600. $30,000 to $150,000, depending on hardware configuration. **Lattice Logic,** 9 Wemyss Place, Edinburgh EH3 6DH, UK. Phone (031) 225 3434.

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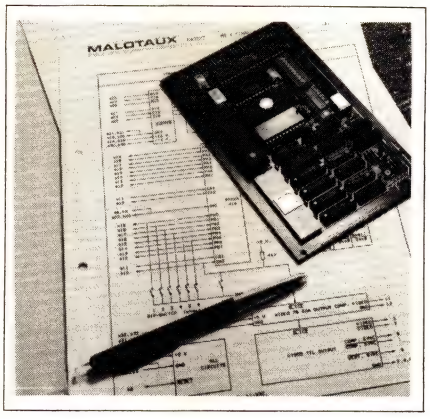
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Circle No 367

GRAPHICS BOARD. Using a NEC 7220 graphics processor and a 6809 μP, this single-Eurocard module provides 262,144 (eg, 576×432) monochrome graphic dots at a rate of 24 MHz, or 35 MHz optionally. Screen formats and scan and refresh rates are fully programmable. Output is TTL *or* 75Ω composite video.



The board contains two 8-bit bidirectional I/O ports, two 16-bit timer/counters and one 8-bit I/O shift register. Other features include a serial RS-232C/V.24 interface, 20 parallel (6522 VIA) I/O lines and the capacity for 32k bytes of EPROM and 8k bytes of RAM. 1950 Dfl. **Malotaux Electronic Systems Design,** Dorpsstraat 74, 3732 HK, De Bilt, Holland. Phone (030) 770105. TLX 47825.

Circle No 368

PLASMA DISPLAY. The TH7612 ac plasma panel has a 12-line×40-character display capability. The panel is supplied with control circuitry and terminal-interface logic in a package measuring 260×155 mm with a depth of only 33 mm. RS-232C, 20-mA or parallel interfaces are available as options. Brightness of the 5×7-dot matrix characters can be adjusted in four discrete levels. Cursor, underlining and selective character blinking can be provided. The display operates over −10 to +60°C and requires four supply voltages—5, 12 and ±95V. **Thomson CSF,** 38 Rue Vauthier, BP 305, 92102 Boulogne-Billancourt Cedex, France. Phone (1) 604 81 75.

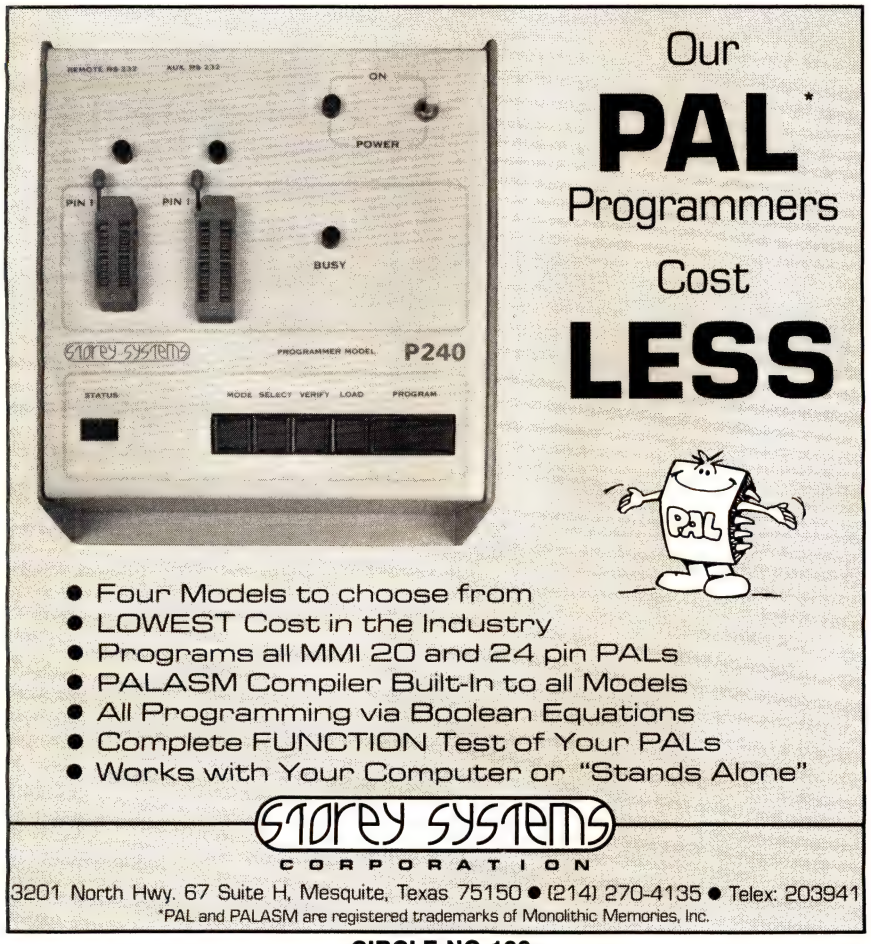
Circle No 369



VME μC. The SYS68K standard 1AC is a fully-integrated VME μC system with the Coherent operating system (UNIX-compatible with C compiler). It comprises an 8-MHz 68000 μP, 512k bytes of dynamic RAM, a SASI interface and controller, a 20M-byte Winchester and 1M-byte floppy-disk drive, and a 200W power supply. Space for an additional six VME cards is provided. The unit comes in a 19-in. enclosure with a 9-slot backplane, twin fans and cables. **Force Computers GmbH,** Daimlerstrasse 9, 8012 Ottobrunn, West Germany. Phone (089) 6092033. TLX 524190.

Circle No 370

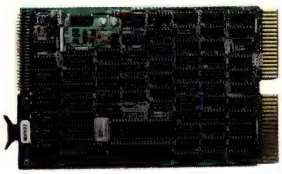
VME MODULE. The EFD-Combo board for the VME Bus provides a multipurpose slave function with as much as 1M byte of RAM, four ROM sockets, on-board EPROM pro-



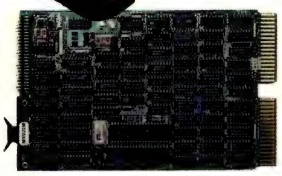
CIRCLE NO 129

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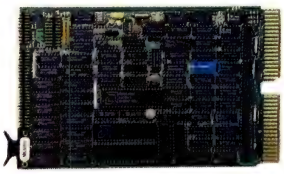
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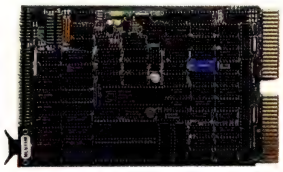
1. Q-BUS RX02 COMPATIBLE 8" FLOPPY DISK CONTROLLER-MXV22.



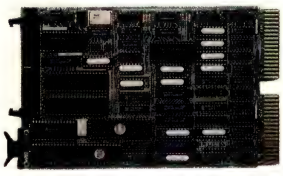
2. Q-BUS RX02 COMPATIBLE 5¼" FLOPPY DISK CONTROLLER-MXV22M.



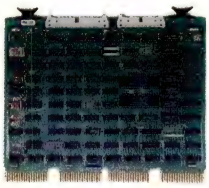
3. Q-BUS RL01/RL02 COMPATIBLE 8" WINCHESTER DISK CONTROLLER MLV11.



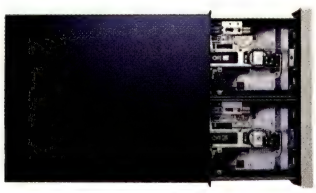
4. Q-BUS RL01/RL02 COMPATIBLE 5¼" WINCHESTER DISK CONTROLLER MLV11M.



5. NEW Q-BUS TSV05 COMPATIBLE ¼" STREAMING CARTRIDGE TAPE CONTROLLER-MSV05.



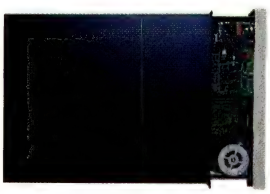
6. NEW UNIBUS RX02 COMPATIBLE 5¼" or 8" FLOPPY DISK CONTROLLER-MX22.



7. Q-BUS RX02 COMPATIBLE 8" FLOPPY DISK SUBSYTEM-MD3100.



8. Q-BUS RX02 and RL02 8" FLOPPY/ WINCHESTER SUBSYSTEM-MD3500.



9. NEW Q-BUS RL02 AND TSV05 8" WINCHESTER / ¼" STREAMING CARTRIDGE TAPE SUBSYSTEM MD3800.

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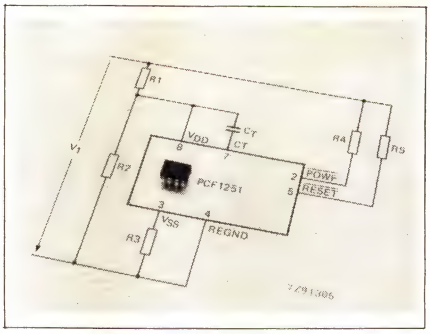
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CIRCLE NO 130

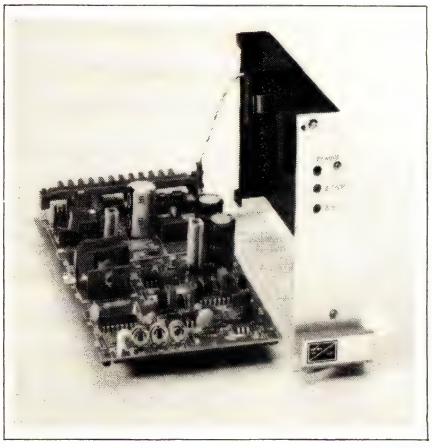
gramming for either 8k or 16k devices in two sockets, and a SASI interface using the 68230. Other functions include a timer, programmable interrupt and LED status display. 15,000 FF. **Thomson Semiconducteurs,** 45 Ave de l'Europe, 78140 Velizy, France. Phone (3) 946 97 19. TLX 204780.

Circle No 371



VOLTAGE DETECTOR. External resistors set the trip point and hysteresis for the PCF1251 voltage detector. There are four outputs, two of which can be delayed through the use of capacitors. Current consumption is typically 1 μA. Designed primarily for power on/off monitoring, the device consists of a 1 to 1.3V bandgap reference and a delay circuit. Two versions are available, in either SOT-96A or SOT-97A packages. **NV Philips' Gloeilampenfabrieken,** Elcoma Div, Box 523, 5600 AM, Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

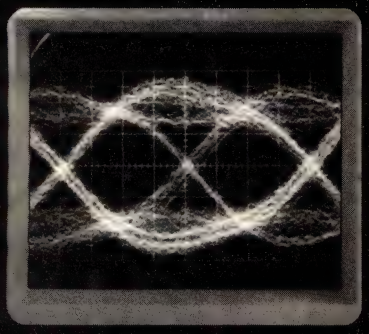
Circle No 372

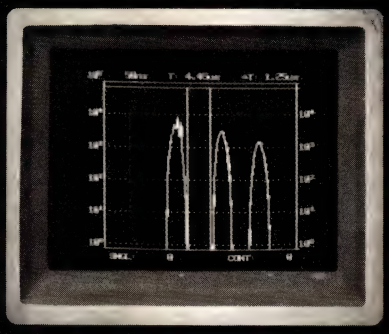


DC/DC CONVERTERS. Switchpac dc/dc converters use MOSFETs switching at 150 kHz to handle 50W on a single 100×160-mm Eurocard. Output choices are 5V at 5 or 10A, 12V at 4.2A, 15V at 3.3A, 18V at 2.8A and 24V at 2.1A. Input voltage is 24V to a tolerance of −2V, +4V. Supplied in a plug-in format for 19-in. racks, the front-panel width is 40.64 mm. Features include soft start and overvoltage protection. **Schroff GmbH,** 7541 Straubenhardt 1, West Germany. Phone (07082) 794 1. TLX 7245024.

Circle No 373

New precision without eye patterns
Time interval analysis advances from





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Increased precision and productivity...

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Qualitative vs. quantitative...

Traditional eye patterns measure performance qualitatively—indicating only good, bad, or marginal results. Kode's TIA's, rendering event-by-event histograms, are quantitative tools that usher in a new and unprecedented degree of accuracy for design and testing.

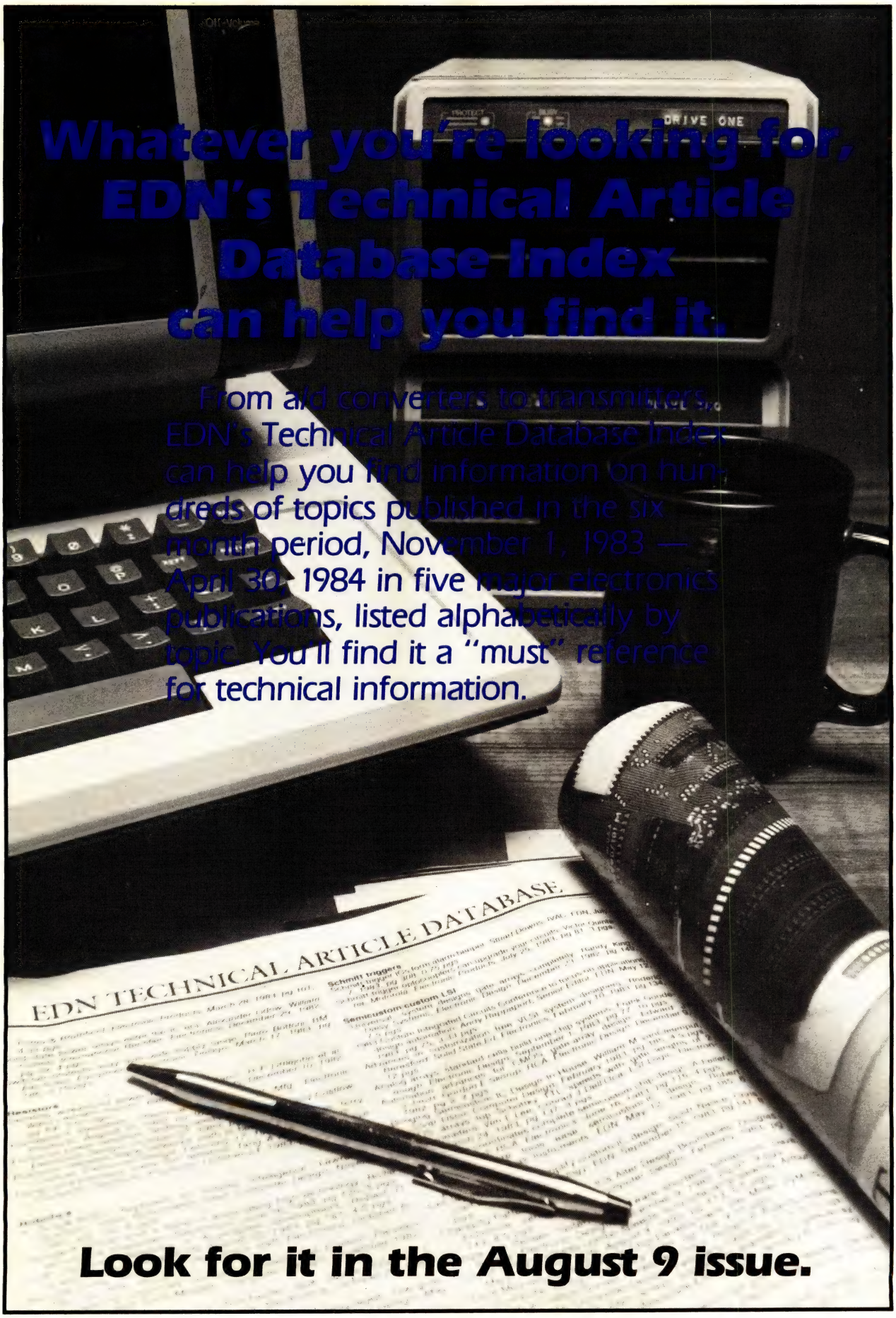
Kode's time interval analyzers offer you...

- Detailed statistics to quantify and analyze bit distributions.
- Capture of isolated, single events. Infrequent events are not only detected but shown to the operator and quantified.
- Aid in pinpointing design causes of bit distortions.
- Graphic screen displays to tell the operator everything at a glance.
- On-board analysis storage for future reference and screen comparison.

Kode Inc. A subsidiary of Odetics, Inc.
2752 Walnut Ave., Tustin, CA 92680
Phone: (714) 730-6901

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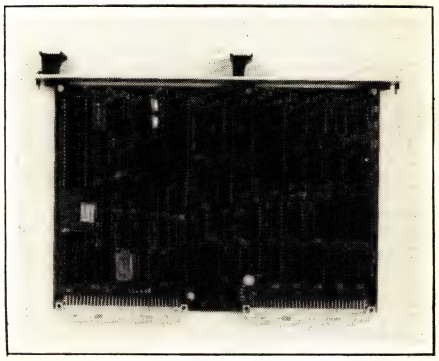
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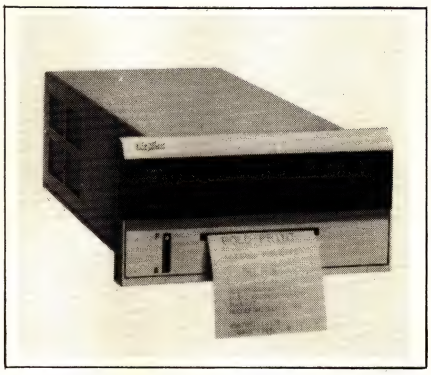


DISPLAY CONTROLLER. The IV-1653 is a VME Bus, character-oriented, color CRT-display controller that supports displays of 48 lines×80 characters noninterlaced or 66 lines×102 characters interlaced. It has a 256-character, downloadable RAM character set for user-defined fonts and mosaic graphics. You select among eight foreground and eight background colors, with blinking and underlining options. The controller supports soft scroll, split screen and horizontal scroll. It includes a parallel keyboard-input port and two full-duplex, asynchronous serial ports. The 16k-word character map memory and 4k-word character-generator RAM are dual ported with the VME Bus. These ports are accessible from the bus with minimal latency and no visual disturbances. Additional circuitry allows synchronization with the IV-1651 graphics-display controller to provide an alphanumeric overlay. $1295. **Ironics Inc,** Box 356, Ithaca, NY 14850. Phone (607) 277-4060.

Circle No 301

D/A BOARD. Compatible with all S-100 Bus μC systems, the Model SB-64 D/A converter board provides 64 output channels by multiplexing an 8-bit converter. The 64 channels perform as discrete D/A converters, each with digital input latches and an output amp. Each output drives a 1-kΩ load and has ±0.4% absolute accuracy from 0 to 10.625V. Address decoding allows memory-mapped I/O to any 256-byte sector in the RAM. Ten digital outputs, a 12-bit D/A converter with 3-msec settling, a ±15V tracking regulator with 600-mA output, and 24-bit address decoding are all optional. AC devices are computer controllable when driving dc/ac proportional controllers with the converter. $495. **Digital Multi-Media Control,** 355 California St, Suite 122B, Burlingame, CA 94011. Phone (415) 342-5904.

Circle No 302



PANEL PRINTER. Model 6610 is a μP-based, 24-column, panel-mount printer that uses plain roll paper, similar to the type used in calculators. According to its supplier, it's the first panel-mount unit to feature a true RS-232C 20-mA port. Baud rate is switch selectable from 75 to 9600 baud. Data bits, parity and stop bits are also user selectable. Standard type prints in a 5×7-dot matrix, and users can choose fonts of double height or double width or both. The printer's μP can be factory programmed for graphics capability. A switch or control character provides first-line-up or first-line-down printing. Impact heads print 0.9 lps. A word-wrap switch lets users eliminate split words or numbers on lines exceeding 24 characters. $495. **Digitec Corp,** Box 458, Dayton, OH 45401. Phone (513) 254-6251.

Circle No 303

PROGRAMMABLE CONTROLLER. The Quantum 2000 provides scan speeds of 4 to 5 msec, 24 I/Os (expandable to 472 I/Os), and 2048 16-bit words in RAM or EPROM. It has 56 counters or timers, 512 control relays and internal fusing. In addition, the printer features 75k-cps counting, positioning, 2-speed motor control, analog comparison and adjustable counting and timing. A handheld personal computer or the supplier's One-Step CRT programmer performs programming. The One-Step, based on the KayPro II computer, has a ladder-diagram documentation package. Contacts, coils and relays have 3-line, plain-English descriptions. Each rung can be as many as 60 characters in width and one page in length. $700. **McGill Manufacturing Co Inc,** 1002 N Campbell St, Valparaiso, IN 46383. Phone (219) 465-2200.

Circle No 304

TAPE COUPLERS. Models TC05 and TC15 provide software-transparent storage and back-up capabilities, using Control Data's start/stop/streaming ¼-in. cartridge tape drive, with DEC LSI-11, PDP-11, Micro/PDP-11 or VAX-11 CPUs. The couplers incorporate bipolar, bit-slice μP technology. Microprogrammed firmware on the board supports high-speed tape-streaming operations automatically, dictated by application efficiency and requiring no operator intervention. Both couplers provide functional emulation of the DEC TS11 tape subsystem and operate transparently to the DEC RSX11M and M-Plus, RSTS-E, RT-11 and VMS operating systems and diagnostic software. Both units are packaged on a quad-wide pc board. The TC05 embeds directly into a Q Bus backplane slot in LSI-11 and Micro/PDP computers; it supports 22-bit addressing and provides 4M bytes of memory. The TC15 embeds in a Unibus SPC slot of PDP-11 or VAX-11 CPUs. Both couplers handle 16-bit NPR data transfers. TC05, $1300; TC15, $1400. **Emulex Corp,** Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; in CA, (714) 662-5600.

Circle No 305

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ht-inch, high-ca
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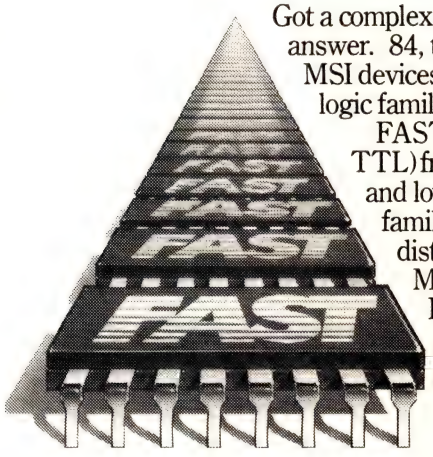
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CIRCLE NO 145

COMPUTER-SYSTEM SUBASSEMBLIES

IEEE-488 BOARD. The MXI-241 IEEE-488 (GPIB) multifunction board provides an interface between the IBM Personal Computer and GPIB-compatible devices. You can connect as many as 15 devices to the unit. The board allows the IBM PC to act as a GPIB system controller. The unit has one programmable interval timer and one programmable Intel 8255 peripheral-interface chip with 24 I/O lines. A software package supplies all routines for the GPIB function. All macro commands are in object code, which is loaded into memory upon powering the IBM PC. The package furnishes an address link into the object code when macro commands are called from BASIC. $395. $100 for software support package. **Qua Tech Inc,** 478 E Exchange St, Akron, OH 44304. Phone (216) 434-3154.

Circle No 306

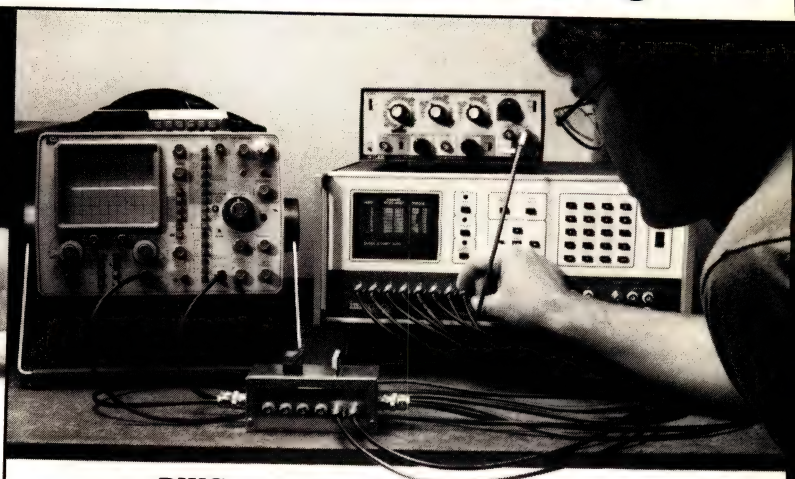
INSTRUMENT CONTROL. The GPIB-1014 lets you implement VME Bus-compatible computers as general instrumentation system controllers. It provides IEEE-488 access to high-end VME Bus systems based on 32-bit μPs like the 68000, and compatibility with 8- or 16-bit μPs. The board furnishes direct VME Bus memory access to and from the GPIB. The interface can serve as an IEEE-488 talker, listener or controller. It supports normal and extended talker and listener, serial and parallel poll, service-request and remote-programming functions. Other capabilities include VME Bus addressing, GPIB synchronization detection, a carry-cycle function and DMA test mode. Software support includes a set of driver routines, an interactive control program and diagnostics. The driver package is available as a shared, multiboard handler running under UNIX System III. $1295. **National Instruments,** 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-5066; in TX, (512) 250-9119.

Circle No 307

WHO'S GOT DIBS ON THE DWG?

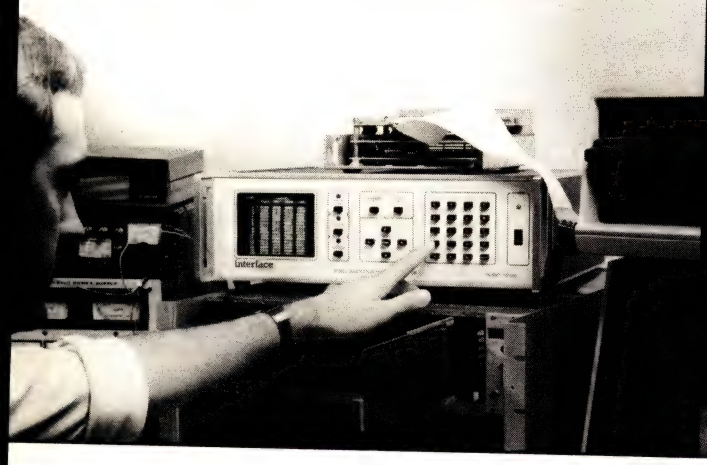


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DWGs speed up IC characterization.

DWGs simulate prototype environments.



DWGs eliminate building dedicated circuitry.



You never know where a Digital Word Generator from Interface Technology will show up next.

From testing discrete designs before system integration to simulating prototype environments, these DWGs can handle it all. Speeds to 100 MHz and up to 4096 bits of memory on each of 16 channels make the RS-660 and RS-680 the most powerful and versatile instruments of their type.

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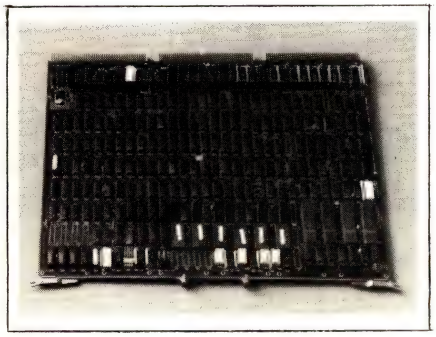
Circle 188 for literature

Circle 189 for demonstration

PRINTER EMULATOR. The dual-purpose Passport printer emulator prevents potential time and data loss in personal computers. It features two operational modes: print passthrough and print bypass. When the latter mode is selected, the emulator appears as a standard printer device. Inadvertent depression of the print-screen key or other means of invoking printer operations prevent the keyboard from locking up, or from forcing you to reload the computer. The mode requires no physical printer mechanism or printer cable. When pass-through mode is selected, the unit permits normal printing operation. Reselecting the bypass mode allows you to abort a print operation. Designed to work with the IBM Personal Computer and compatible systems, the unit emulates virtually all parallel printers normally connected with a PC-compatible printer cable. The device is compatible with PC-DOS and MS-DOS. $29.95. Delivery, 4 to 6 wks ARO. **Micro Computer Components,** Box 195, San Diego, CA 92126. Phone (619) 453-3367.

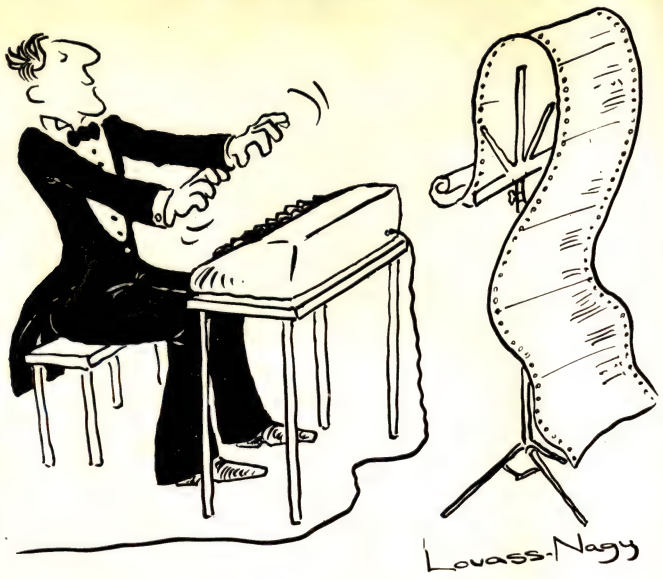
Circle No 308





VAX DISK CONTROLLERS. The SC7000 disk controller connects multiple, multivendor disk drives to DEC VAX-11/750 or -11/780 CPUs. It allows you to mix disk drives of different types and configurations, handling as many as four physical (eight logical) industry-standard SMD or Winchester-type drives with capacities of 825M bytes and beyond. Serial data-transfer rates reach 1.8M bytes/sec. The extended-hex-size pc board plugs into the CMI bus of the -11/750 via one of three RH750 backplane slots, or into one of two slots in the vendor's V-Master chassis, which fits in the -11/780. DMA data transfer handles 32-bit words via the CMI or SBI bus. On-board switching allows you to select 64 combinations of predefined disk-drive configurations on four ports. On-board firmware emulates DEC's RM03, RM05 and RM80 disk subsystems. A 4k RAM buffer furnishes 12-sector buffering. The controller operates transparently to VMS and UNIX operating systems and diagnostic software. $8950. **Emulex Corp,** Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; in CA, (714) 662-5600.

Circle No 309



Before Johann Sebastian Bach developed a new method of tuning, you had to change instruments practically every time you wanted to change keys. Very difficult.

Before Avocet introduced its family of cross-assemblers, developing micro-processor software was much the same. You needed a separate development system for practically every type of processor. Very difficult and very expensive.

But with Avocet's cross-assemblers, a single computer can develop software for virtually any microprocessor! Does that put us in a league with Bach? You decide.

The Well-Tempered Cross-Assembler

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Avocet cross-assemblers are fast, reliable and user-proven in over 3 years of actual use. Ask NASA, IBM, XEROX or the hundreds of other organizations that use them. Every time you see a new microprocessor-based product, there's a good chance it was developed with Avocet cross-assemblers.

Avocet cross-assemblers are easy to use. They run on any computer with CP/M* and process assembly language for the most popular microprocessor families.

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Turn Your Computer Into A Complete Development System

Of course, there's more. Avocet has the tools you need from start to finish to enter, assemble and test your software and finally cast it in EPROM:

Text Editor VEDIT -- full-screen text editor by CompuView. Makes source code entry a snap. Full-screen text editing, plus TECO-like macro facility for repetitive tasks. Pre-configured for over 40 terminals and personal computers as well as in user-configurable form.

CP/M-80 version $150
CP/M-86 or MDOS version $195
(when ordered with any Avocet product)

EPROM Programmer -- Model 7128 EPROM Programmer by GTek programs most EPROMS without the need for personality modules. Self-contained power supply ... accepts ASCII commands and data from any computer through RS 232 serial interface. Cross-assembler hex object files can be down-loaded directly. Commands include verify and read, as well as partial programming.

PROM types supported: 2508, 2758, 2516, 2716, 2532, 2732, 2732A, 27C32, MCM8766, 2564, 2764, 27C64, 27128, 8748, 8741, 8749, 8742, 8751, 8755, plus Seeq and Xicor EEPROMS.

Avocet Cross-assembler	Target Microprocessor	CP/M-80 Version	CP/M-86 IBM PC, MSDOS** Versions
XASMZ80	Z-80	$200.00 each	$250.00 each
XASM85	8085		
XASM05	6805		
XASM09	6809		
XASM18	1802		
XASM48	8048/8041		
XASM51	8051		
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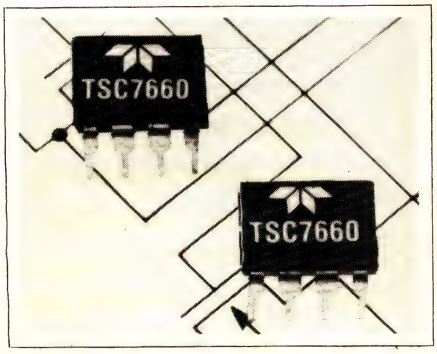
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CIRCLE NO 135

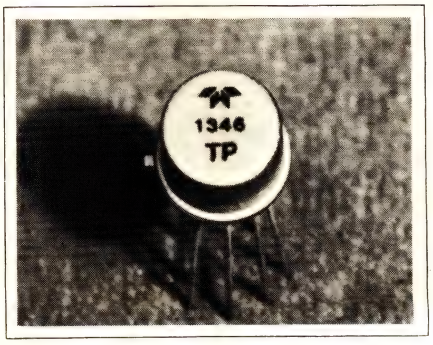


DC/DC CONVERTER. The Model TSC7660 CMOS dc/dc converter generates a negative voltage from a positive source. With two external capacitors, the unit converts a 1.5 to 10V input signal to a level of −1.5 to −10V. It generates −5V in +5V digital systems. The converter charges a capacitor to the applied supply voltage, and internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor, completing the voltage conversion. The negative open-circuit output voltage is within 0.1% of the positive input voltage. Power-conversion efficiency is 98% for 1-mA loads and 92% for 15-mA loads. Contained on chip are a series dc power-supply regulator, RC oscillator, voltage level translator, four output power-MOS switches and a logic element. The logic element senses the most negative voltage in the device and ensures that the output n-channel switches are not forward biased to provide operation that's free of latch-up. The unit can convert the positive input voltage to a higher positive level. It comes in a plastic or hermetic 8-pin DIP and is available for commercial, industrial and military temperature ranges. $1.90 to $8 (100). **Teledyne Semiconductor,** 1300 Terra Bella Ave, Mt View, CA 94043. Phone (415) 968-9241. TWX 910-379-6494.

Circle No 310

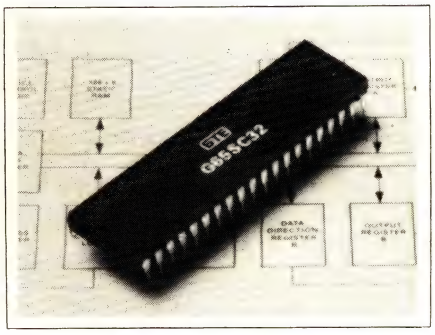
INSTRUMENTATION AMP. The addition of a CMOS multiplexer and resistor network aids the AD625 single-chip instrumentation amp in designing 12-bit software-programmable-gain amps (SPGAs). The amp's four grades spec 5-ppm/°C max gain TC, 4-nV/$\sqrt{\text{Hz}}$ input noise and a ±10V input range. Users can configure the unit either as a resistor-programmable-gain amp (RPGA) or as an SPGA. An AD625-based RPGA can be configured for gains between 1 and 10,000 with three external resistors. The amp's gain-sense pin has 130 dB of common-mode rejection regardless of feedback-resistor matching. Maximum specs for the A and S models are ±0.005% nonlinearity, ±0.05% gain error, 200-μV input offset voltage, 5-mV output offset voltage and 110-dB CMR. The B version's maximum specs are ±0.003% nonlinearity, ±0.03% gain error, 75-μV input offset voltage, 3-mV output offset voltage and 120-dB min CMR. Maximum specs for the C version are ±0.001% nonlinearity, ±0.02% gain error, 25-μV input offset voltage, 2-mV output offset voltage and 130-dB min CMR. $9.50 to $27 (100). **Analog Devices Semiconductor,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 935-5565.

Circle No 311



OP AMPS. Combining JFET/bipolar technology and dielectric isolation, Models 1346 and 1347 provide ±250-fA bias current, ±100-μV offset voltage, 2-MHz unity-gain bandwidth and 30-mW power consumption. The amps are suitable for such applications as precision long-term integrators, high-impedance buffers and low-drift track/hold amplifiers. Housed in 8-lead TO-99 packages, the amps operate over 0 to 75°C. They're also available spec'd for the military temperature range. $5 to $19 (100). **Teledyne Philbrick,** Allied Dr at Rte 128, Dedham, MA 02026. Phone (617) 329-1600. TWX 710-348-6726.

Circle No 312



TIMER IC. The Model G65SC32 programmable-CMOS-RAM, I/O-timer device is bus compatible with 6500/6800 Series μPs and has functions for programmed control of two peripherals. In a 40-pin DIP the device combines a 128×8-bit static RAM, two 8-bit bidirectional data ports, an interval timer and interrupt control. The RAM, which can be used as a scratch pad or special data buffer, interfaces directly with the μP through the data bus and address lines. The bidirectional data ports permit direct interfacing of the μP and selected peripherals. Two programmable registers provide data direction control at each port; this control can be implemented line by line with intermixed I/O lines within the same port. The interval timer contains a preliminary divide-down register, programmable 8-bite register and interrupt logic. It can be programmed to count 256 time intervals with interrupt timing capability in intervals from one to 262,144 clock periods. The IC is implemented using the silicon-gate CMOS process; it consumes 2 mA at 1 MHz. It comes housed in plastic or ceramic packages or ceramic DIPs. $7.65 (100) in plastic packaging. **GTE Microcircuits,** 2000 W 14th St, Tempe, AZ 85281. Phone (602) 968-4431.

Circle No 313

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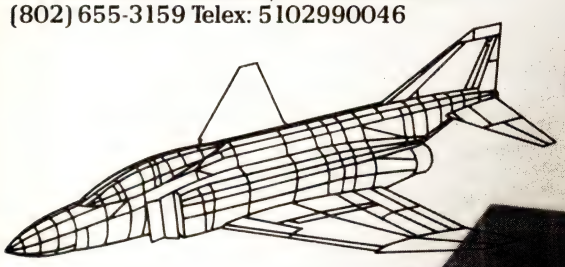
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For more information call or write Jack Scully, Polhemus Navigation Sciences Division, McDonnell Douglas Electronics Company, P.O. Box 560 Colchester, Vermont 05446 (802) 655-3159 Telex: 5102990046



Imagine digitizing a 3-dimensional model simply by placing a stylus on points of interest.

MCDONNELL DOUGLAS

CIRCLE NO 136

DRIVER ICs. Power interface ICs UDN-2935Z and -2950Z each incorporate a source-sink driver, associated predrive and input buffer stages and clamp diodes. The high-current, bipolar half-bridge 2A motor drivers also include logic lockout to prevent the source and sink drivers from turning on simultaneously, and they provide thermal shutdown and an increased logic-supply voltage range. Although designed for use with servo motors, they're also applicable to ac, single-winding dc and brushless dc motors as well as capacitive loads. The units eliminate the requirements for four external logic elements in the full-bridge configuration. The -2935Z directly replaces the SG3635P, and the -2950Z replaces the UDN-2949Z and SN75605 in most applications. **Sprague Electric Co,** North Adams, MA 01247. Phone (413) 664-4411.

Circle No 314

POWER MOSFETs. These 64 TMOS power MOSFETs are direct second-source replacements for the IRF 100, 200, 500 and 600 Series MOSFETs and cost 10 to 25% less than those units. The devices are for use in switching power supplies, motor controls, inverters, audio amplifiers and coil drivers. They feature a V_{DSS} rating of 60 to 200V and an I_D of 3.5 to 40A, depending on the device. $1.16 to $20.66 (100). Delivery, stock to 6 wks ARO. **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. Phone (602) 244-4911.

Circle No 315

FET OP AMP. The dielectric-isolation FET (DiFET) OPA111 op amp features a 0.4-fA/$\sqrt{\text{Hz}}$ current noise, which allows it to achieve total circuit noise lower than a bipolar device in applications where source resistances exceed 15 kΩ. Its 6-nV/$\sqrt{\text{Hz}}$ voltage noise is three to five times better than the top BiFETs, according to the manufacturer. Other specs include 1-pA max bias current, 1-μV/°C max voltage drift and 1-μV rms max noise. Testing guarantees noise performance. Laser trimming achieves ±250-μV max offset voltage and 1-μV/°C max FET drift. The amp produces 125-dB open-loop gain and consumes 2.5 mA. Common-mode and power-supply rejection are 110 dB typ, and slew rate and unity-gain bandwidth are 2V/μsec typ and 2 MHz typ, respectively. Housed in a hermetic TO-99 package, the op amp has a standard 741 pinout. Two versions operate over −25 to +85°C, and a third operates over −55 to +125°C. From $6.35 (100). **Burr-Brown,** Analog Div, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

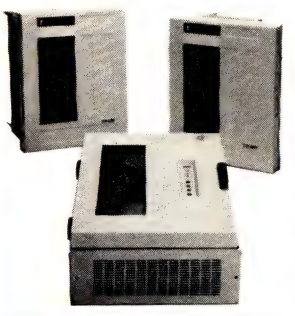
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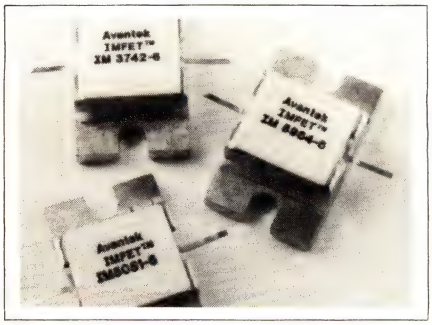
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CIRCLE NO 138

POWER MOSFETs. Characterized by low $r_{DS(ON)}$ figures, these high-current TMOS power MOSFETs range from 50 to 200V and feature a 120 to 200A continuous drain current rating. The units feature high-frequency capabilities as well as peak current capability to 800A. The low $r_{DS(ON)}$ results in minimal On losses and improved efficiency. These units can replace TO-3 devices operating in parallel. Applications include mainframe power supplies, motor controls, inverters, solar regulators and uninterruptable power supplies. Model MTE200N05/06 200A devices with 50 and 60V V_{DSS}, respectively, $114 and $120. **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. Phone (602) 244-4911.

Circle No 317



GaAs FETs. IMFET internally matched FETs furnish 6W (+38 dBm) min output power at 1-dB gain compression. Each unit delivers 7W typ output power with 20W max power dissipation. The IM-3742-6 is optimized for the 3.7- to 4.2-GHz frequency band, the IM-4450-6 for 4.4 to 5 GHz, the IM-5051-6 for 5 to 5.1 GHz, and the IM-5964-6 for 5.9 to 6.4 GHz. Power-added efficiencies are 31% or 32%, and minimum gain is 8.5 to 10.5 dB. Each model is tuned for operation in a 50Ω system. External tuning is not required. $525 (50). **Avantek Inc,** 3175 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-6710.

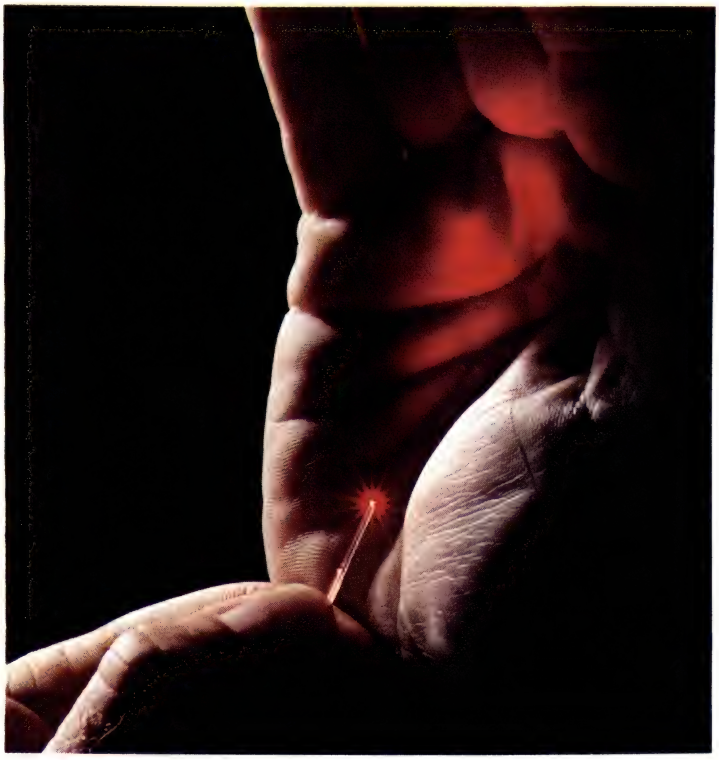
Circle No 318

OCTAL LATCH. The CD74HC373 octal transparent latch has 3-state outputs and is an addition to the QMOS high-speed-CMOS logic family. Its 6-mA current-drive capability lets it serve as a data-bus driver in 8-bit μP systems. For transparent operation, the eight output lines track the eight input lines when the Latch Enable ($\overline{LE}$) line is High. When $\overline{LE}$ goes Low, data is latched in the chip's input buffers, and the output lines are unaffected by input line changes. A separate Output Enable line controls the 3-state outputs. Latch operation is independent of the Output Enable line. The latch specs a 14-nsec typ propagation delay time. Power-supply range is 2 to 6V dc, and operating temperature spans −40 to +85°C. The latch comes housed in a 20-lead plastic DIP. $1.98 (100). **RCA Solid State Div,** Rte 202, Somerville, NJ 08876. Phone (800) 526-2177.

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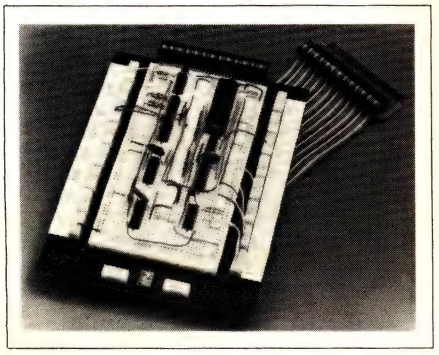
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CIRCLE NO 140



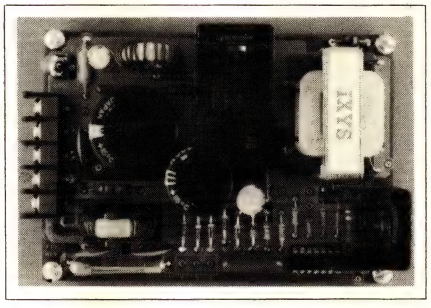
PROTOTYPING BOARD. The eZ board is a solderless system that provides a method for building experimental add-ons that interface with personal computers. A flat-ribbon cable connects a solderless breadboard to a computer's bus expansion slot. Versions are available for the IBM Personal Computer and Apple and Commodore computers. The breadboarding area consists of 2090 tie points with a capacity of 24 14-pin DIPs. Components with lead diameters as great as 0.032 in. plug in and are connected with solid hook-up wire. Four distribution buses with 50 tie points each can be used for power, ground, clock lines, reset commands, etc. A 4-position DIP switch is mounted on the board; each switch position connects to a set of tie-point block sockets on either side, to aid in the development and analysis of experimental circuits. $174.95. **Sabadia Export Corp,** Box 1132, Yorba Linda, CA 92686. Phone (714) 630-9335. TLX 756582.

Circle No 374

FLOPPY SWITCHERS. The ML Series floppy-disk-drive switching power supplies provides open- or closed-frame construction, 50-kHz operation and an input-voltage range of 98 to 132V ac at 47 to 440 Hz. The series' three supplies conform to UL 114, 478 and CSA C22.2, Nos 143 and 144, and meet FCC noise regulations, Class B. They provide power for two standard 5¼-in. floppy-disk drives. Other specs include as many as three outputs, typically 5V dc at 1 to 3A, 12V dc at 0.2 to 1.5A (3A peak) and −12V (or −5V) dc at 0 to 0.1A; 0.2% max input line regulation; 2% max load regulation; 1% p-p max ripple and noise; overvoltage and short-circuit protection; and a 50°C operating temperature without derating. The units measure 5.7×3.15×1 in. and weigh 1.1 lbs. $30 (OEM qty). Delivery, stock to 16 wks ARO. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094. Phone (201) 392-4264.

Circle No 375

50W SWITCHER. The XS5D is a 50W, single-output switching power supply featuring CMOS PWM, power-MOS switching, fixed switching frequency from 50 to 200 kHz (cus-



tomer selected) and an optocoupled voltage sensor. Other features include fault-tolerant connectors for uninterruptible operation, short-circuit protection, soft start and 85% typ efficiency. Units can be stacked together in series or in parallel. $99. **IXYS Corp,** 3685 Enochs, Santa Clara, CA 95051. Phone (408) 733-4045.

Circle No 376

WAVEFORM DIGITIZER. The 3500SA/200 consists of an intelligent mainframe and a plug-in 200M-sample/sec transient recorder. It provides 5-nsec time resolution and 8-bit amplitude resolution. You can add other digitizer or signal-conditioning modules as needed. The digitizer features 8192-point waveform memories. Bit-slice-processor technology controls acquisition and performs high-speed signal processing on the data as it's ac-



quired. The system generates 512-point FFTs on raw or averaged time-domain data, and it can average the instantaneous frequency spectrum. A separate processor permits simultaneous viewing of frequency and time displays without slowing acquisition time. On-screen manipulations include normalization, subtraction, overlay, peak search, smoothing and display of selected regions. The system furnishes fully programmable control and analysis. You control acquisition and display via keyboard or light pen. A stored command procedure sequentially executes as many as 600 actions, including archiving to a floppy disk or a remote computer. $24,995. **LeCroy Research Systems Corp,** 700 S Main St, Spring Valley, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

Circle No 377

SIGNAL SWITCHER. Allowing multiple switches to be closed at the same time, Model 604 200-MHz programmable signal switcher performs make-before-break or break-before-make operations. It switches 200-MHz signals with only 0.6-dB typ attenuation at the highest frequency. The unit is IEEE-488 compatible. Automatic bed-of-nails testing takes approximately 15 sec. In the field, an input can be attached and channels switched through to measure output. The unit measures 8.5×3.5×11 in. $695. **Wavetek,** 9045 Balboa Ave, San Diego, CA 92123. Phone (619) 279-2200. TWX 910-335-2007.

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CIRCLE NO 141



QUAD-OUTPUT SWITCHERS. The MRX-400 Series of 400W, quad-output, open-frame switching power supplies has a regulated 12 or 24V, 1.5A output for driving CRT displays. The units also provide a 5V, 50A output and a choice of ±12 or ±15V, 10A outputs. The supplies have a power density of more than 2.1W/in.^{3} An adjustable main control loop regulates the line and load of the 5V output to ±1%. A second adjustable control loop on the primary side of the output transformer regulates the line and load of the ±12 or ±15V outputs to ±2%. An adjustable linear postregulator holds the 12 and 24V outputs to ±1%. Selectable ac inputs vary from 90 to 132V ac or 180 to 264V ac, at 47 to 63 Hz. Soft-start circuitry minimizes input-current surge at turn-on. Ripple and noise are 0.2% rms (1% p-p) or 100 mV, whichever is greater. All outputs have overload protection; overvoltage protection is provided for the first three outputs. Remote sensing is standard on the 5V output. Efficiency is 75% typ. The units weigh 5 lbs. $535. **Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717. Phone (516) 231-3366. TWX 510-227-4905.

Circle No 379

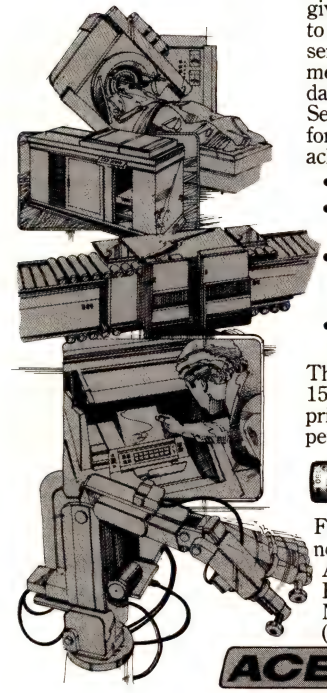
FLOPPY EXERCISER. The portable Model 911 floppy-disk exerciser runs 8-, 5¼- and 3-in. drives with standard interfaces. It features a crystal-controlled write frequency, a 7-segment display for seek address, and auto, continuous and single-step modes. It provides all status signals via LEDs. Test points align and troubleshoot drives down to the component level. A keypad sets the desired track address. The unit operates from a 5V supply. Adapters for running the Osborne and Apple floppy-disk drives are available. $550. **J&E Computer Service,** 4000 Rosebay St, Chino, CA 91710. Phone (714) 597-5135.

Circle No 380

8096 DEVELOPMENT TOOL. The iSBE-96 single-board emulator is the debugging portion of an 8096 development package (see Software Products section). It's the logical equivalent of the 8096 microcontroller, allowing the debugging of 8096 hardware and software in real time. You can use the board to integrate hardware and software development for some MCS-96 applications. $3500; $2450 for ASM-96 software; $16.50 (10,000) for the MSC-96 microcontroller (the MSC-96 is currently available in sample quantities). **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-9484.

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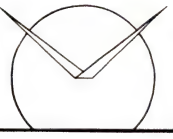
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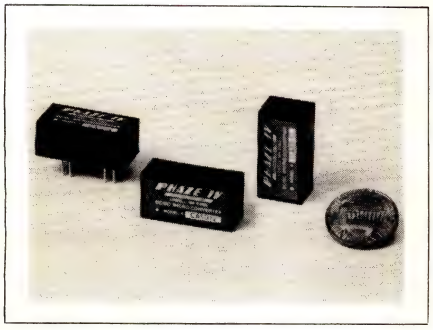
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DIP-SIZED CONVERTERS. The CA Series of dc/dc converters provides unregulated, isolated single and dual outputs. Maximum output power is 1.5W and the units withstand 1000V dc at 100-MΩ input-to-output isolation. The converters come in 16-pin DIP-compatible packages. Power foldback furnishes indefinite short-circuit protection. The units have only eight leads in a staggered pattern that ensures proper orientation. The missing leads also allow extra room under the device for additional pc-board traces. $27.60 (100). **Phaze IV Technology Inc,** Box 8187, Lowell, MA 01853. Phone (617) 454-3044.

Circle No 382

CABLE TESTER. This tester troubleshoots insulation-displacement connectors (IDCs) and cables that conform to MIL-C-83503 dimensions. The FCT-100 automatically tests for shorts, miswiring, connector reversals and opens in IDC terminations of as many as 64 conductors. The unit's total testing time is 58 msec, and it weighs 10 lbs. Thirty adapter boards are available, along with uncommitted boards for individualized fabrication. $1603. **Alpha Wire Corp,** Box 711, Elizabeth, NJ 07207. Phone (201) 925-8000. TWX 710-996-5895.

Circle No 383

500W VARIABLE SUPPLY. The SYR 50-9.5 has an output-voltage range of 0 to 50V and a 9.5 max current output. It operates in a constant-voltage or constant-current mode with automatic crossover. The efficiency rating exceeds 75%. The unit provides for remote voltage and current programming, remote shutdown and connection for remote sensing. You make voltage and current adjustments with dual concentric coarse and fine front-panel controls. Standard units operate on an ac input of 103 to 127V ac at 48 to 63 Hz. Optional ranges are 188 to 230V ac, 198 to 242V ac and 205 to 255V ac. Current regulation, line or load, is 0.25%. The unit specs a 0.02%/°C TC and a 0 to 71°C ambient operating-temperature range with derating. The 3.5×19×16-in. unit weighs 42 lbs. $695. Delivery, stock to 10 wks ARO. **Sytron Inc,** RFD 1, Perimeter Rd, Londonderry, NH 03053. Phone (603) 627-3655.

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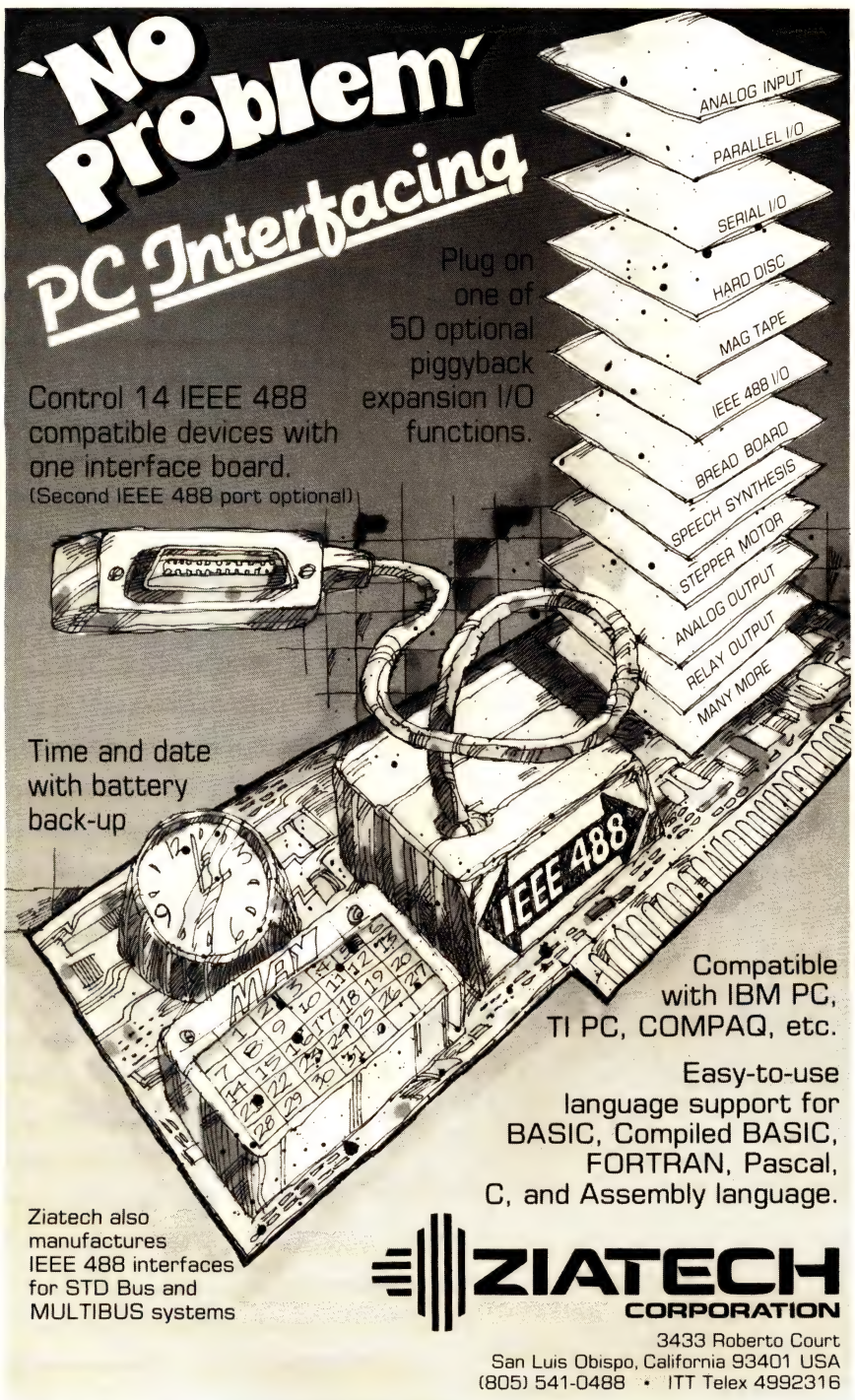
MAKING CMOS WORK FOR YOU.

CIRCLE NO 146



DATA ACQUISITION. The PCI-3000 operates as a front-end processor interfacing a personal computer's bus to both industrial and laboratory transducers as well as signal sources for transmission of analog and digital data. Compatible host computers include the IBM PC and XT, Apple, Compaq, DEC and Hewlett-Packard systems, and many minicomputers and mainframes. The front end has a modular design and a wide selection of analog, digital and special-function I/O boards. Internal, user-modifiable firmware accepts high-level commands. The basic system includes a master unit with power supply, Z80A μC and firmware board with 64k of RAM and EPROM, and as many as three I/O boards. As many as 192 analog or digital I/O points are available from a single master unit. With additional expansion enclosures, the master unit provides as many as 1024 I/O points using 15 I/O boards. Analog input is ±10 mV to ±10V direct, with programmable gain of 1 to 1000 and 12-bit resolution. Analog output is ±10V, 4 to 20 mA. TTL digital I/O is 24-mA current sink, 15-mA current source. From $3000. **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

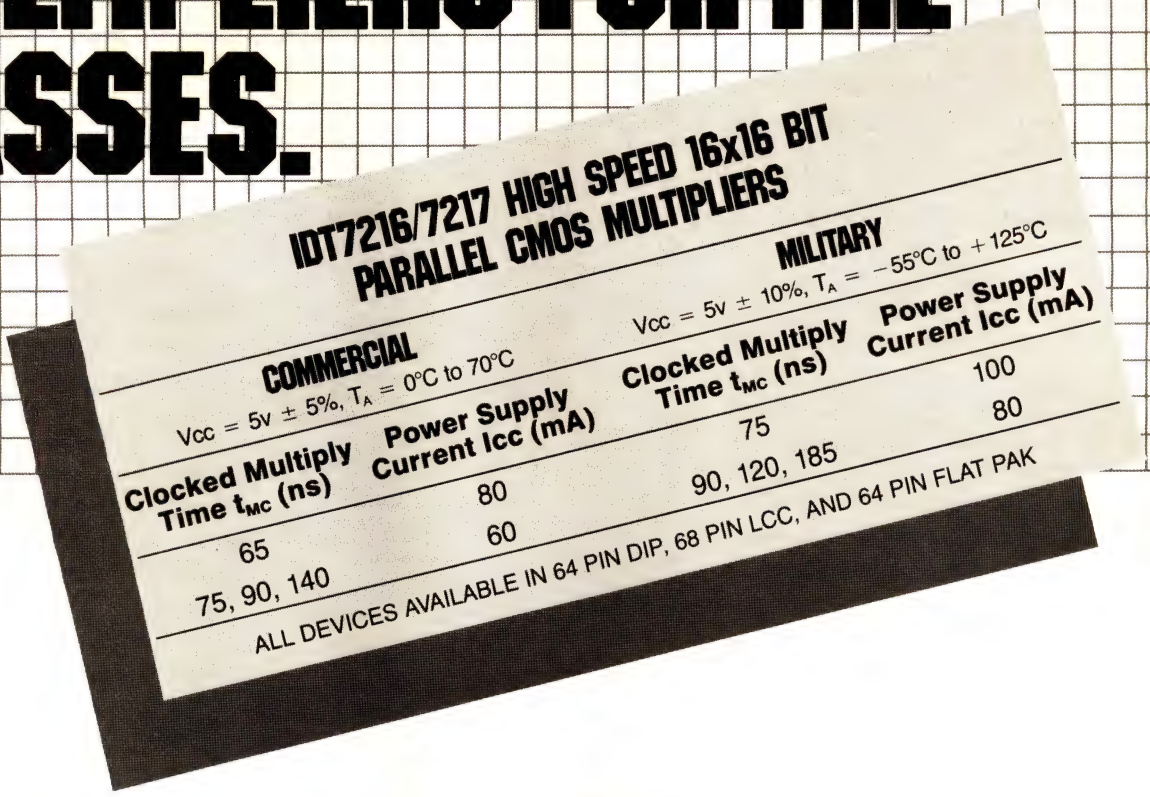
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3½-DIGIT DMM. In peak-hold operation, Model 3100A handheld DMM holds the peak value of transient signals in a short-term analog memory, remembering and displaying the highest positive dc or ac rms level reached by the input signal. Should the signal on the input leads change to a larger value, the peak-hold memory will track the change to hold the new maximum level, even if the input should fall thereafter. The DMM provides eight functions in the following ranges: dc volts from 200 mV to 1000V FS; ac volts to 750V; dc and ac current from 200 mA FS to 10A; and resistance from 200Ω to 20 MΩ. Other features include a diode-testing mode and continuity beeper. Basic dc accuracy specs at ±0.1%. The unit can measure ac signals to 5 kHz. Electrostatic shielding protects against EMI. The unit operates from a 9V alkaline battery. $129. **Ballantine Laboratories Inc,** Box 97, Boonton, NJ 07005. Phone (201) 335-0900.

Circle No 388

MULTIPLIERS FOR THE MASSES.



In the past you probably didn't even consider using multipliers in your system design for obvious reasons: high power consumption, heat build-up, low reliability, large power supplies, elaborate cooling schemes, and more…

Now all that's over.

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Speed/torque drive systems and SCR controls

Catalog CDM-PM-C contains 20 pgs of information on the selection and application of permanent-magnet adjustable speed/torque drive systems and companion SCR controls. Featured products are SCR controls, motors and gearmotors as well as a newer line of motors and gearmotors with more power per frame size. Text, operation graphs and control- and drive-selection tables guide the reader to the best selection for his application. Use of the vendor's drives with power supplies from other companies is provided with application information for user-designed systems. Dimensional drawings, mounting recommendations and electrical operating requirements are included. **Bodine Electric Co,** 2500 W Bradley Pl, Chicago, IL 60618.

Circle No 343

A primer on robotics

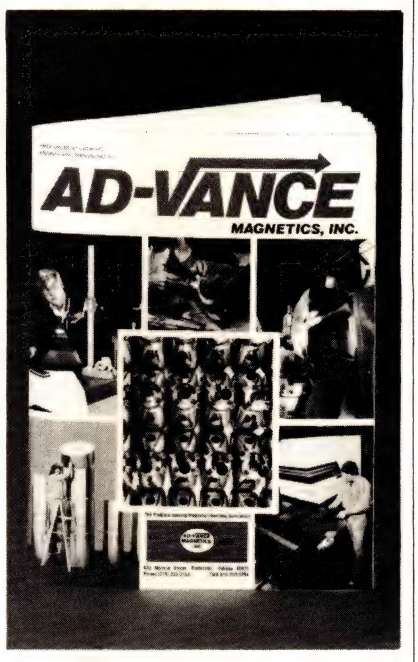
This primer describes the fundamentals of simple, nonservo robots. The 26-pg publication covers the elementary aspects of robotics and includes application information. A layout chart and associated manual serve as practical guides in structuring a robot in the cartesian coordinate system from standard components. **Mack Corp,** 3695 E Industrial Dr, Flagstaff, AZ 86001.

Circle No 344

Buyer's guide focuses on hand tools and testers

This 144-pg buyer's guide illustrates and describes hundreds of hand tools, tool kits, test equipment and related products. In addition, one section is devoted to tool kits for those who repair, maintain and service electronic and electromechanical equipment. Name-brand hand tools are illustrated and described in detail with specifications included. **Electronic Tool Co Inc,** 101 Castleton St, Pleasantville, NY 10570.

Circle No 345



Guidelines for designing or selecting magnetic shields

For magnetic-shield users, the 84 - pg Procurement Catalog / Engineering Manual No 90 contains useful technical data needed to design or choose the optimum magnetic-shielding solution for a given application. Three engineering sections include reprints of articles written by the publisher's engineering staff. Technical articles also cover the enhanced skin effect and the basic relations between $\overline{E}$ and $\overline{H}$ vectors for a plane wave. Twenty-five case histories contain solutions to such problems. **Ad-Vance Magnetics Inc,** 625 Monroe St, Rochester, IN 46975.

Circle No 346

Quartz frequency management devices

The *Guide to Quartz Frequency Management Devices* provides photographs and outline drawings of standard and custom crystal products. Included are precision, military and μP crystals; TCXO-TCVCXO, ovenized, SC cut, voltage-controlled crystal and hybrid clock oscillators; and standard filters/discriminators and custom filters. Crystal performance curves and a MIL-vs-commercial cross reference for MIL-equivalent crystals are provided. **CTS Corp,** Knights Div, 400 E Reimann Ave, Sandwich, IL 60548.

Circle No 347

Specs on LVDTs

Featuring graphically plotted performance specifications, this 40-pg catalog furnishes complete design parameters on linear variable differential transformers (LVDTs). The graphs are provided for each of seven variables, showing what happens to an LVDT's performance when such parameters as temperature, frequency and output load impedance are introduced. The catalog details the use of the products in various displacement-sensing instrumentation systems. It also describes LVDT operating principles, construction, custom designs and accessories and includes a glossary introducing readers to LVDT terminology. **Robinson-Halpern,** Box 248, Plymouth Meeting, PA 19462.

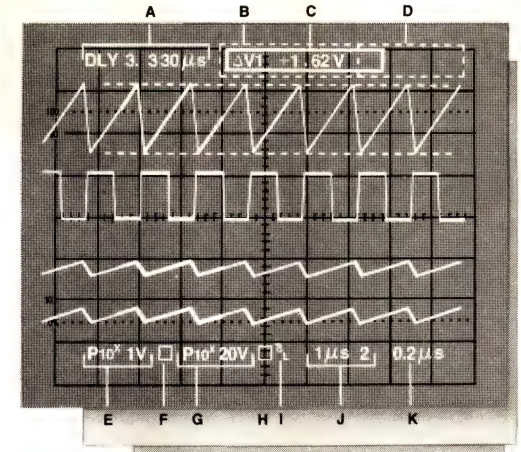
Circle No 348

Reference guide to data systems

This 6-pg color brochure provides data-systems engineers with a quick reference guide to the magnetic-tape systems and controllers that are compatible with specific HPIB and IEEE-488 computer systems. It describes how the products enhance data-processing systems for users of Hewlett-Packard, DEC, Tektronix, Fluke and other computer systems. The brochure includes performance ranges and applications of the supplier's product line. A convenient reference chart shows which products interface with specific computer brands on a model-by-model basis. **Dylon Data Corp,** 9561 Ridgehaven Ct, San Diego, CA 92123.

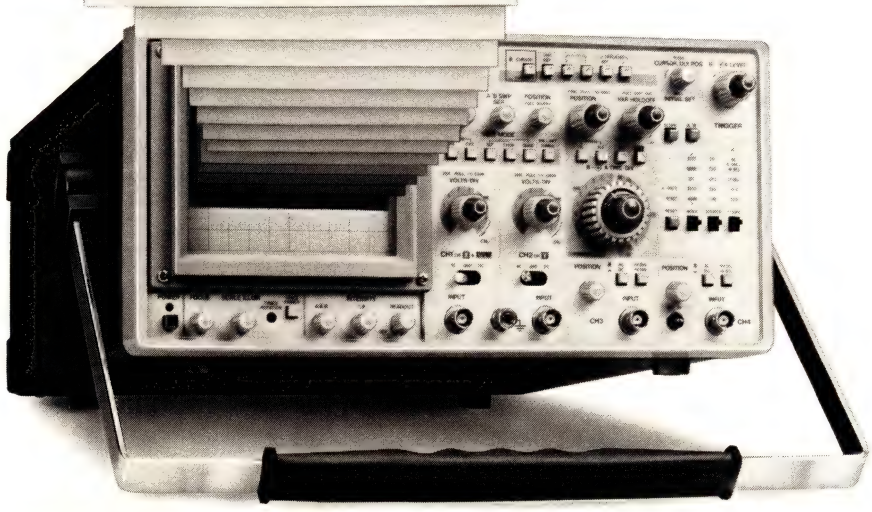
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A. Delay Time
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F. Add Indicator
G. Scaling Factor (CH2)
H. Invert Indicator
I. BWL Indicator
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HITACHI V-1100



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		Frequency counter	Frequency: 120Hz to 99.9MHz		
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	Panel setting Value displays		Vertical axis: V/div, INVERT, ADD, BWL, UNCAL, MAG Sweep speed: s/div, UNCAL, MAG Other: delay time and A trigger source		
GND Reference function	Ground line display (GND LINE)		CH1 and CH2 displays are available.		

Additional features include quad channel (CH. 1, 2, 3, 4) with independent position controls, 8 trace with alternate sweep, 18kV-6" rectangular CRT, minimum deflection factor 1mv/div, maximum sweep time 2ns/div, TV-sync, X-Y operation up to 1 MHz (3° or less), variable hold-off, gate output for A and B sweep, CH 1 signal output to 100 MHz (-3dB)...plus much more.

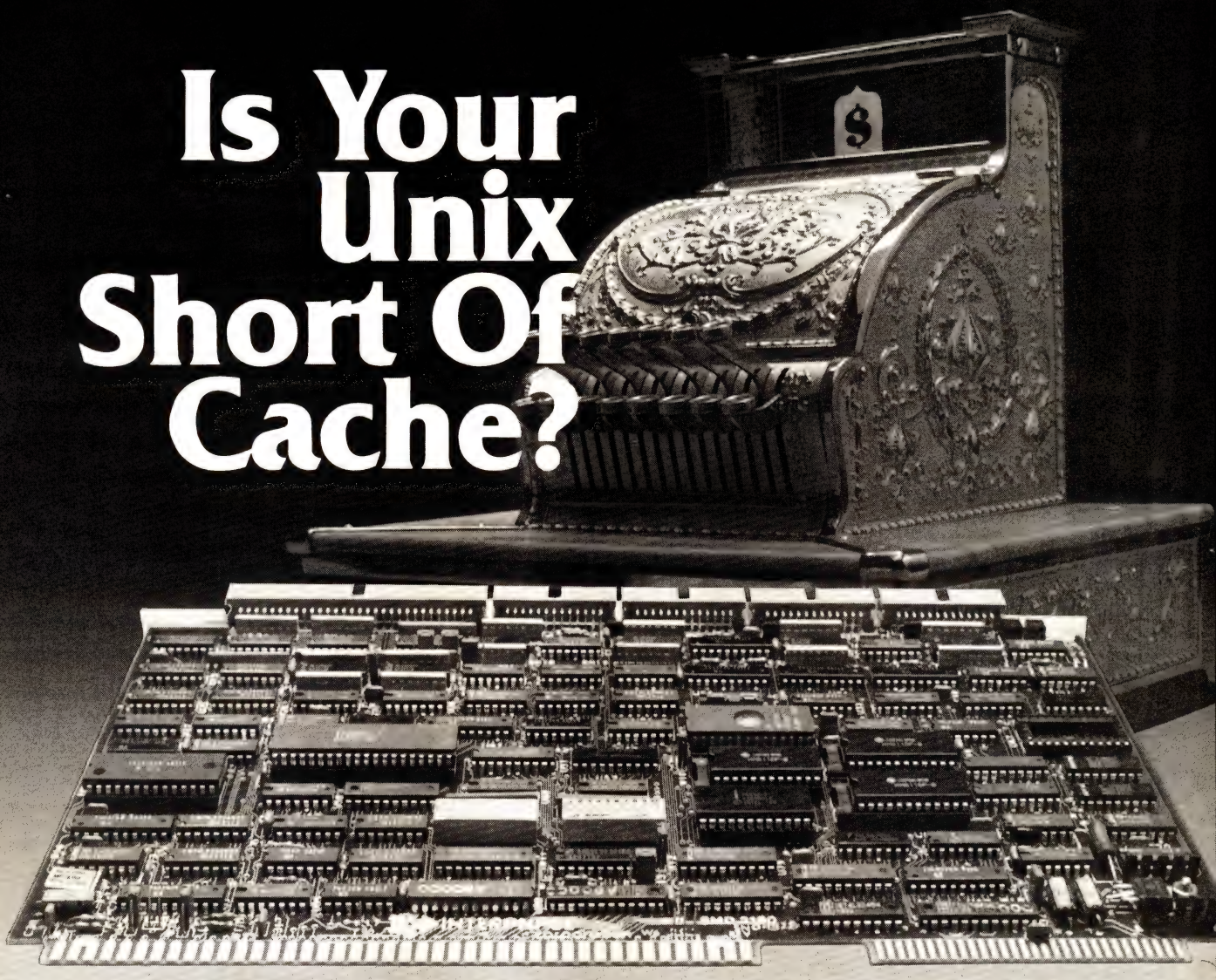
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CIRCLE NO 157

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Software compatibility across the Interphase Family of SMD disk controllers means the maximum return on your software investment.

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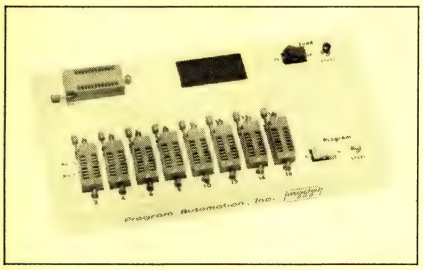
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CIRCLE NO 149

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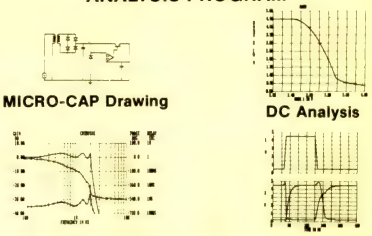
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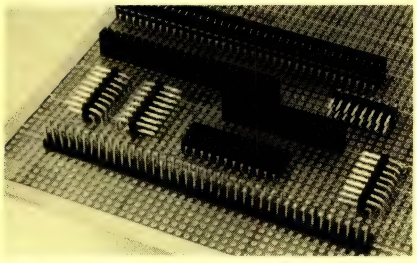
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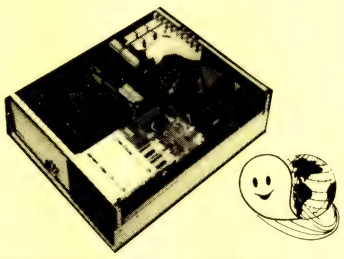
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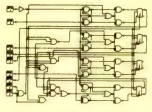


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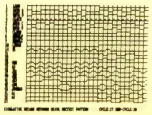
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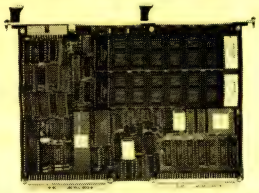
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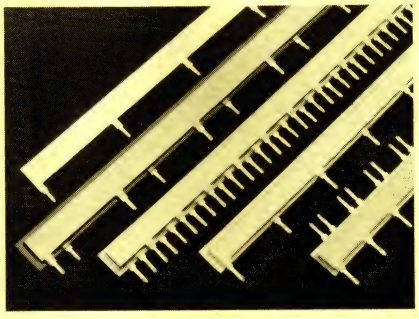
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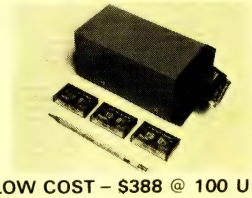


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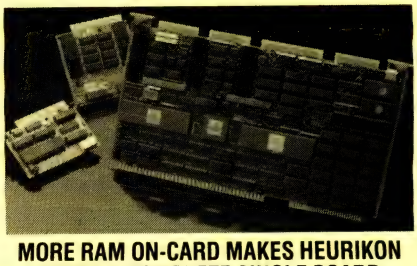
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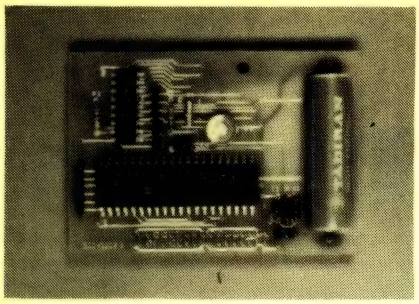
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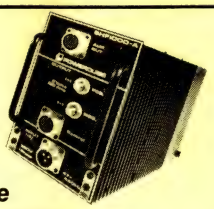
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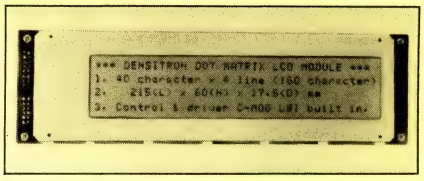
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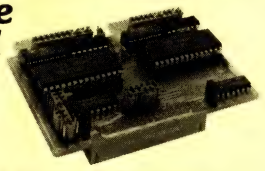
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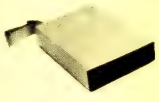
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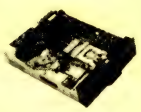
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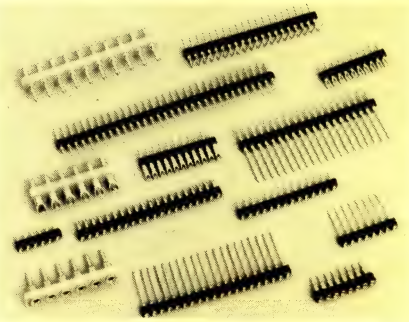
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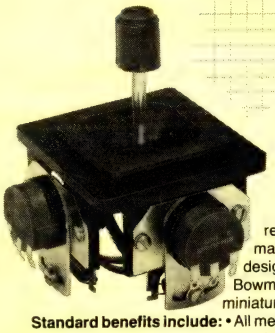
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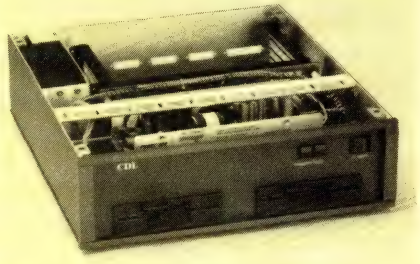
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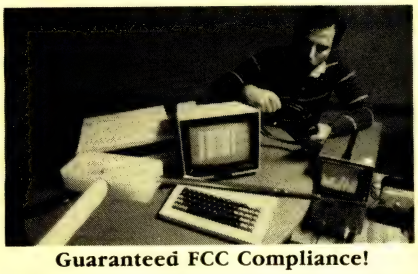
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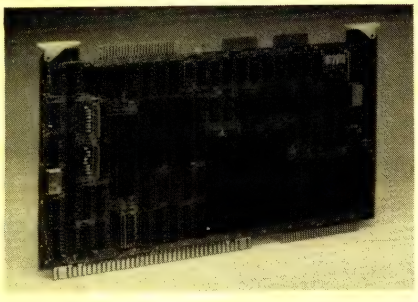
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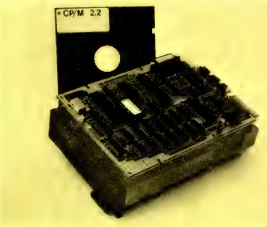
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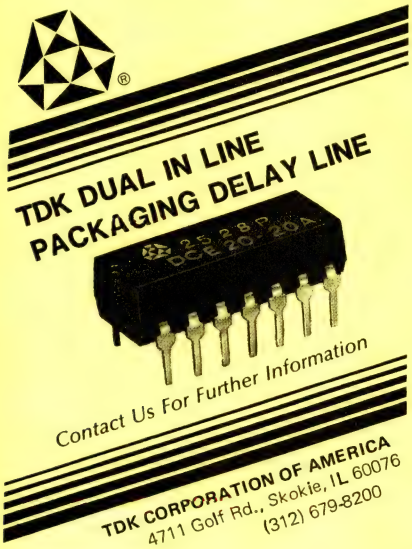
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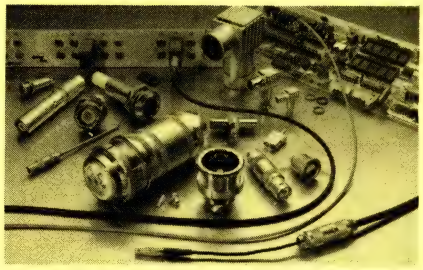
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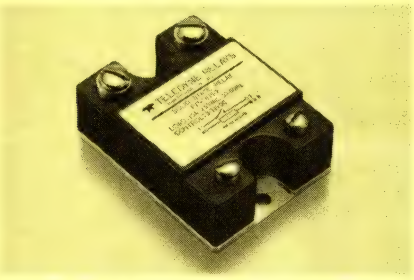


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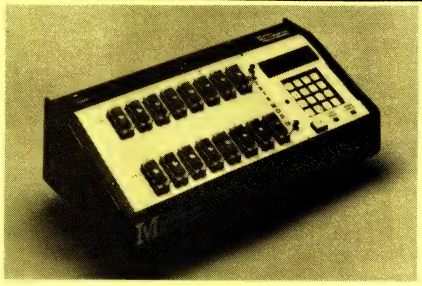
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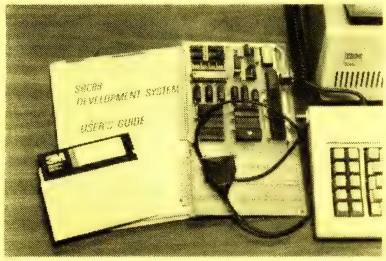
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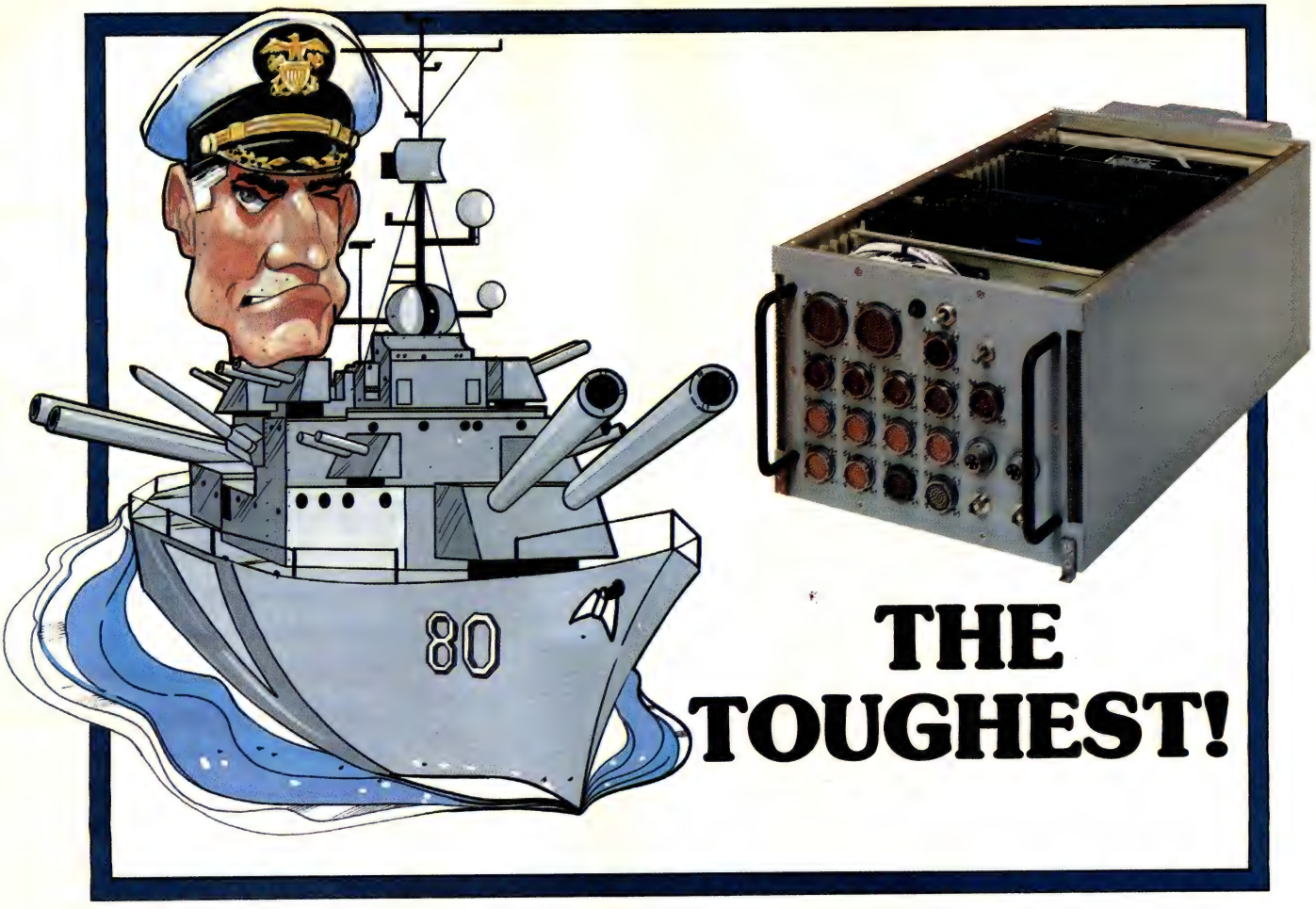
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CIRCLE NO 150

Written and edited by Shelley Mumford

More jobs with higher salaries greet 1984 engineering graduates

With the current high demand for electrical engineers, this year's graduates are experiencing no difficulty in finding employment. Many high-technology companies prefer new EE graduates who can be trained to the organizations' particular styles, so the firms are urging recruiters to spend more time on college campuses.

The current popularity of graduating EEs is also causing enrollment figures to soar. At Rensselaer Polytechnic Institute (RPI, in Troy, NY), where undergraduates have until their sophomore year to choose a major, almost 70% of the 1984 freshman class is interested in electrical engineering. Programs in computer science (CS) and computers and systems are equally popular.

But RPI and many schools like it are having difficulty accommodating this high interest. To remedy the problem, RPI is attempting to discourage some students from entering the EE or CS programs. The school has tightened its grade-point-average requirement for transfer students to a minimum of 3.7. Furthermore, RPI is encouraging students to consider future fluctuations in the demand before rushing into an EE or a CS curriculum. Pointing to the rise and fall in the demand for chemical engineers, Vicki Lynn, director of RPI's career development center, cautions incoming students that the same kind of decrease could occur in the demand for electrical engineers.

Despite efforts to control matriculation, the number of graduates continues to grow. According to the Engineering Manpower Commission, the number of BSEE graduates in 1983 increased by 16% over 1982's total, rising from approximately 16,000 to almost 19,000. On the MSEE level, the number of degree recipients also escalated by 14%, moving from approximately 4086 to 4645. PhDs increased by 14% from 549 to 628 recipients. Throughout the nation, those schools graduating the highest number of EEs in 1983 include the Georgia Institute of Technology (Atlanta, GA), with the most BSEE graduates (349), and Stanford University (Palo Alto, CA), with the highest number of masters-degree recipients (209) and the largest class of PhDs (41).

		Rensselaer Polytechnic Institute	Stanford University	Massachusetts Institute of Technology	Georgia Institute of Technology	UCLA
BSEE	1984	$27,271	**$29,268**	$28,260	$26,745	$27,759
	1983	$26,136	$25,776	$26,880	$26,436	$25,827
MSEE	1984	$31,123	$32,628	$31,800	$31,100	**$33,134**
	1983	$29,201	$29,268	$31,080	$29,520	$31,340
PhD	1984	—	**$54,504**	$43,000	$48,100	NO FIGURE YET COMPILED
	1983	—	$40,416	$39,720	$30,000	$38,680

A random sampling of US engineering schools *reveals that this year's salary offers are higher than last year's. Stanford University (Palo Alto, CA) graduates are being offered the highest salaries at both the bachelors and doctorate levels.*

Demand creates inflated wages

College-placement officials report that high-technology firms nationwide are paying premium salaries for EEs on all three levels—bachelors, masters and PhDs. The Engineering Manpower Commission reports that as of last March, the average salary offerings for EEs were $26,100 for BSEEs, $30,444 for MSEEs and $38,964 for PhDs. (These figures are based on a compilation of offers from 167 US schools.)

In comparison, graduates of Stanford and MIT are receiving the country's highest salary offers. A June 1984 PhD recipient from Stanford, for example, is receiving an average of $55,000, an increase of 35% over last year's average offer of $40,000. (See the **figure** for average salary offers at sample schools.) Masters-degree recipients will command an average of $33,000, up 11.4% from 1983, while BSEEs will earn approximately $29,000, a 13.5% increase over the average 1983 offer of $26,000.

Similar salaries are going to MIT graduates at the bachelors- and masters-degree levels. This year's MSEEs will earn an average of $32,000 (no significant increase over the previous year), and BSEEs will earn approximately $28,000. PhDs, on the other hand, are being offered

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considerably less than their Stanford peers. The average offer is approximately $43,000—$12,000 less than the Stanford figure.

Graduating from these top schools, however, appears to lose its significance below the PhD level. In fact, the highest offers for MSEEs goes to graduates of the University of California at Los Angeles (UCLA), who may expect to receive an average salary of $33,000. Similar salary offers greet graduates of RPI ($31,000) and the Georgia Institute of Technology ($31,000). Salaries remain comparable at the BSEE level with RPI graduates being offered $27,000; Georgia Institute of Technology, $27,000; and UCLA, $28,000.

Wall Street seeks EEs

EEs are being sought in a variety of areas; the most prevalent include aerospace, robotics and computer-aided design. College-placement officials report that the demand for hardware vs software engineers is evenly divided, as is the demand for analog vs digital engineers.

The most unusual hiring trend noted by the major engineering schools is the growing interest of Wall Street brokerage firms. According to Robert Weatherall, director of career services at MIT, companies like Morgan Stanley Inc and Goldman Sachs Inc are combing the doctorate level for EEs specializing in management information systems (MIS). Weatherall states that Morgan Stanley, in particular, is seeking someone to develop an MIS and computer model to support the financial side of the house. He adds that with the enormous trading in AT&T right now, the brokerage firm feels computer analysts could provide much needed assistance.

Carnegie Mellon's assistant director of career services and placement, Robert H Nelson, has also observed the Wall Street interest in PhDs. He attributes brokerage interest to a need for bright, innovative people who have a broad technical base to build on. However, despite the high salaries offered by Wall Street (beginning at $60,000), Nelson doubts that this year's PhDs will actually trade in their technical expertise (and the time and money spent obtaining it) to join Wall Street.

Graduates remain in the area

Regardless of their degree level, most EE graduates tend to stay in the same geographic area as their alma mater. At RPI, for example, 70% of 1983's graduating class remained in the Northeast. The graduates were least attracted to opportunities in the Southeast.

At two California schools, Stanford University and UCLA, the tendency of engineers is to stay in the state. Approximately 80% of the 1983 Stanford graduates remained in Silicon Valley, and 85% of those from UCLA stayed in California.

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CIRCLE NO 152

A Question of Law

Lack of federal software-protection law produces inefficient, incomplete coverage

Ralph D Clifford, *Attorney at Law*
Stamford, CT

Although copyright, patent and trade-secret laws protect software to varying degrees (see **Refs 1** and **2**), software remains without its own clear and simple protection mechanism. This final article in a series of three will explore the reasons why the legal system hasn't adequately provided that mechanism, and it will suggest changes to the existing system that would cure some of the problems associated with protection.

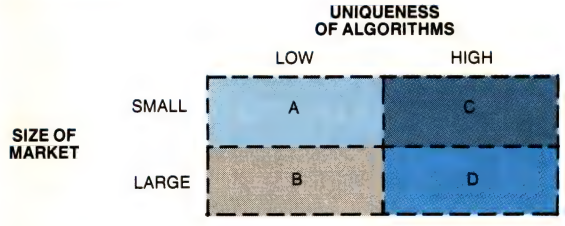
Computer software represents an invention that has several characteristics never seen before. Prior inventions were either machines that could be touched or processes that produced physical results. The work required to reproduce the invention or result was generally significant and normally required the manufacturer's factory.

Software has none of these characteristics. It isn't physical, and once entered into a machine, it can be reproduced rapidly at almost no cost. After distribution, it can be replicated without any assistance from the manufacturer or his equipment. For the first time, therefore, an invention of high complexity and cost can be duplicated rapidly and cheaply by someone who isn't the invention's manufacturer.

As a consequence, the problem of protecting software isn't easy to solve. Unfortunately, given the nature of software, any legal scheme that's established for its protection will not be able to prevent its misappropriation. If your software is illegally reproduced, the only legal recourse you have as the software's inventor is the recovery of the losses suffered as a result of the copying.

Keep in mind that recovering your losses might not be easy either. The current legal system is inadequate. Specifically, there are four debilitating problems in the existing laws that might prevent you from being fully compensated. These problems can be classified as incomplete coverage, inconsistent coverage, preemptive coverage and expensive coverage.

The current laws for software protection can't protect all the computer programs that deserve legal coverage. To determine to what extent your program can be protected, examine the matrix pictured in the **figure.** The horizontal axis measures the uniqueness of your program's algorithms. The vertical axis computes the size of the potential market for your program.



Analyzing your software program's potential market appeal *and the uniqueness of its algorithms can help determine the laws best suited to your software's protection.*

If your computer program can be placed in cell A or B, your program's algorithms have a low uniqueness level, and so the value of that program is derived from the work necessary to express its algorithms rather than from the algorithms themselves. The copyright law is specifically designed to protect objects that gain their value because of the work necessary in expressing them. Consequently, any program falling into those areas is covered under copyright-law protections.

If your program falls into box C, however, your market share is small, and you will thus be able to maintain your program's secrecy fairly easily. In this case, you are best protected by trade-secret laws, which protect your program's unique algorithms from loss due to any cause except independent discovery.

Protecting programs in cell D, however, poses serious problems and remains virtually impossible. If your program falls into this category, you can't use the copyright law, because it requires the disclosure of precisely that which gives the program its value—its unique algorithms. You can't rely on trade-secret protection either, because it's virtually impossible to enforce laws protecting widely marketed trade secrets. This difficulty in enforcement is caused by the variance in state laws and the restrictions existing in consumer-protection and antitrust laws.

In addition to incomplete legal coverage, software protection is further complicated by the multiplicity of

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laws available to the software inventor. For instance, the law of copyrights and trade secrets can always be used for any given computer program. However, those programs that are highly unique and suited for integration into a larger invention require the protection of patent law.

So choosing the right set of laws to protect your program is important. A protection mechanism should be chosen when you're ready to market your program. Beware, however, that if the wrong system is chosen (relying on trade secrets, for example, for a program that ultimately is widely marketed), you might loose your ownership rights to the program. Unfortunately, it's not always possible to predict the market behavior of your program before it's introduced.

A third obstacle to sufficient protection is preemptive coverage. Copyright law contains a provision that might preempt any state's trade-secret protection that's effectively equivalent to copyright protection. Should this apply in a given case, the protections provided by trade-secret laws become invalid. Therefore, if you distribute your programs using trade secrets to protect them, this preemption might amount to total loss of protection, because your trade secret no longer exists.

Unfortunately, if the program is protected under the copyright law as an alternative to trade-secret coverage, anyone can study the program (copyrighted programs can be examined at the Library of Congress in Washington, DC for a nominal fee), extract the algorithm and then rewrite the program. As long as the program is rewritten and not simply copied, no violation of the copyright law has occurred. You'll thus have lost whatever rights you had to the algorithm.

Varied coverage is costly

Whenever multiple options are available, there are costs associated with the process of choosing among them, particularly in protecting computer software.

Prior to marketing your software, you must investigate the factors that control your choice of protection schemes. Such an investigation is expensive and time-consuming. For example, you must evaluate the size of your potential market. In addition, you must determine the uniqueness of your program, the type of purchaser you're most likely to attract, and the potential misappropriation threats you might encounter.

Obviously, the solution to all four types of problems in the current system is a single nationwide law to protect computer software. The best law should provide protection for the computer program, *including its algorithms*. This could be accomplished by adding secrecy provisions to the copyright law. With such an amendment, when copyrighting your program you would have the choice of requesting protection of the algorithms in addition to the program. When such protection is requested, the program wouldn't be available for inspection at the Library of Congress.

However, because it's important to disclose an algorithm so that additional algorithms can be developed from it, the secrecy provided for the program should only last for a limited period of time—10 to 15 years, perhaps. To encourage the disclosure of an algorithm, an additional fee should be charged for the secrecy service, so that only programs that actually obtain their economic worth directly from their algorithms would be kept secret.

Also, the law should explicitly preempt all other possible protections for computer software. If the law were to take effect, only a copyright could be used to protect computer software.

Finally, so that the currently existing software could take advantage of the new law, the ideal statute should contain a saving clause that would allow existing programs to obtain the new form of protection.

The advantages of a single Federal software law are obvious and essential to anyone active in the computer industry. To promote such a statute, however, it's necessary to alert Washington with regard to the significance of such a law. Currently, the groups most active in expressing their opinions to Congress are the major industry giants and their representatives. But while the efforts and needs of large firms are important, their proposals make it more difficult for small companies and single inventors to obtain protection. Thus, if you're not with a large company and want a legal system that will serve your needs also, you too must express your needs to your Congressional representative. **EDN**

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1. Clifford, Ralph D, "Understand copyright laws to ensure software protection," *EDN*, February 9, pg 277.

2. Clifford, Ralph D, "Patents and trade secrets provide two alternatives to software protection," *EDN*, March 8, pg 331.

Author's biography

Ralph D Clifford, JD, received a Juris Doctor degree from New York Law School and a BS in computer science from Duke University. He has been a computer-software consultant for seven years and maintains a private practice of law as a member of the Connecticut and New York Bars.

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Still, specifying the right impact printer isn't easy. So we suggest you begin with a few questions targeted to the end-user.

For example, what form of hard copy would be needed? On cards or roll paper? And if paper, how many plies are needed?

And what about characters per line? And pre-printed forms? Is throughput speed or transaction time critical? How important is graphics capability?

TAKE A TEST DRIVE.

Dot matrix impact printers come in all shapes and sizes. But the biggest variable is speed.

In most impact printers, speed is affected by the shape and density of the characters—both of which can be changed. Another key factor is the method of moving paper through the printer.

By compressing the matrix, you can get more characters per line. By using stepper motors rather than solenoids, you can greatly improve paper speed.

As you can see, the possibilities are endless. So take a test drive first.

To assist you, Eaton Printer Products offers a development kit complete with expanded driver board and printer mechanism to help test & evaluate your complete prototype.

FACE-TO-FACE INTERFACE.

A prime factor in specifying a printer is the supplier's willingness to work one-on-one with you.

Rather than costly trial-and-error on your part, Eaton provides the necessary technical advice, either in person or in written form.

And Eaton offers you customized service for your customized design. Because there's nothing standard about your work.

FAST CHANGE CHANNELS.

There are two other important considerations in your design process: product changes and short lead times.

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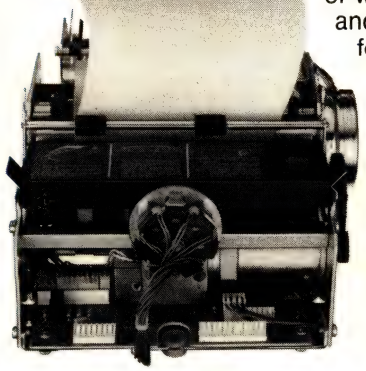
Investigate the track record of both printer and manufacturer. For example, Eaton pioneered dot matrix impact printers . . . earning a reputation as a specialist in today's highly competitive market. And Eaton's 40 column dot matrix printer has a field-proven performance record that has set industry standards. It can be a solid complement to your design, too. It's a high performance printer. It's reliable. And it offers one practical feature that no other printer has . . . it's built in the U.S. and backed by Eaton worldwide. 262-3

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NEWNEWNEW

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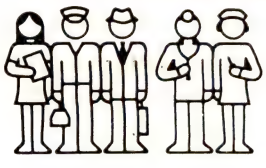
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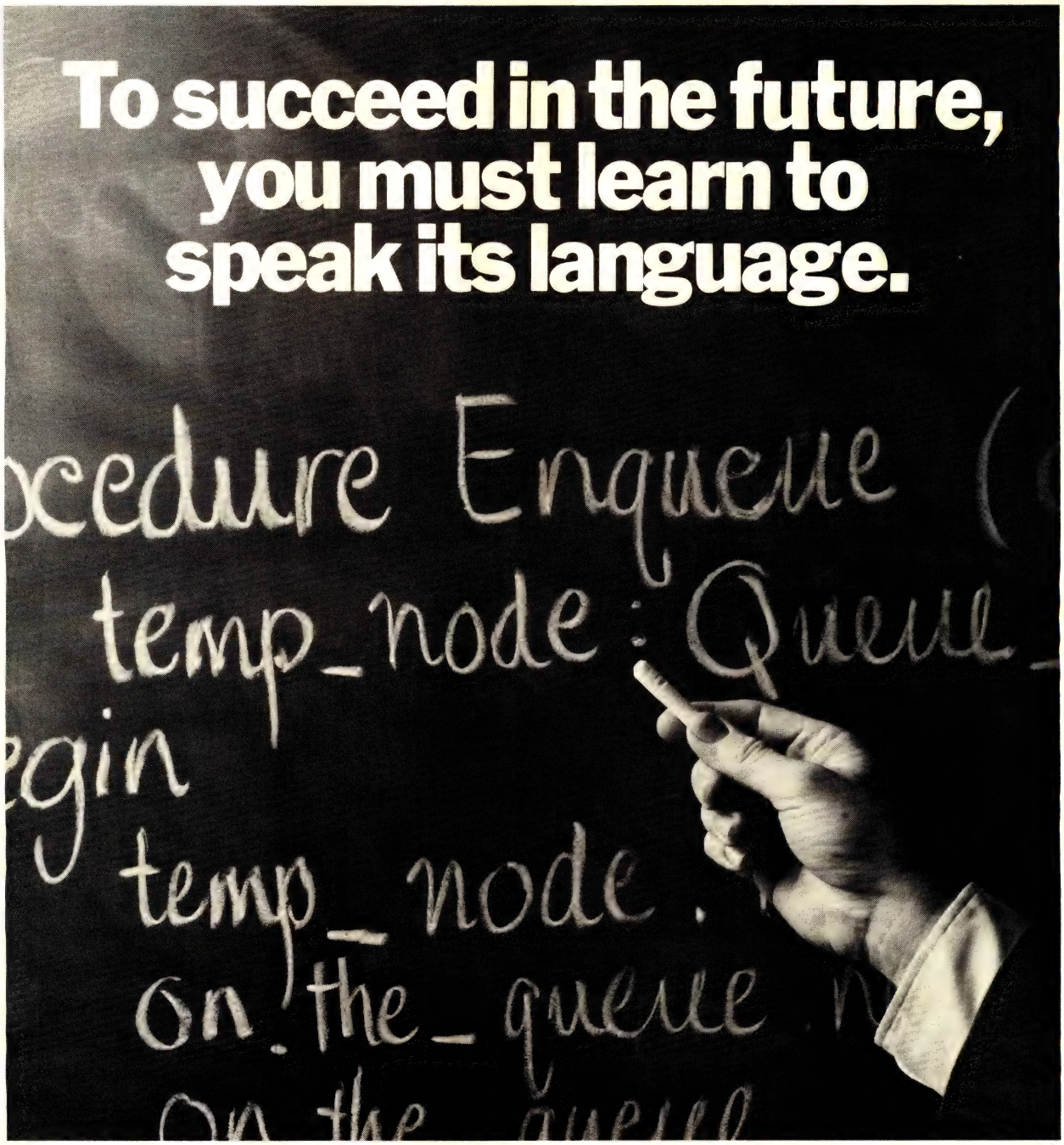
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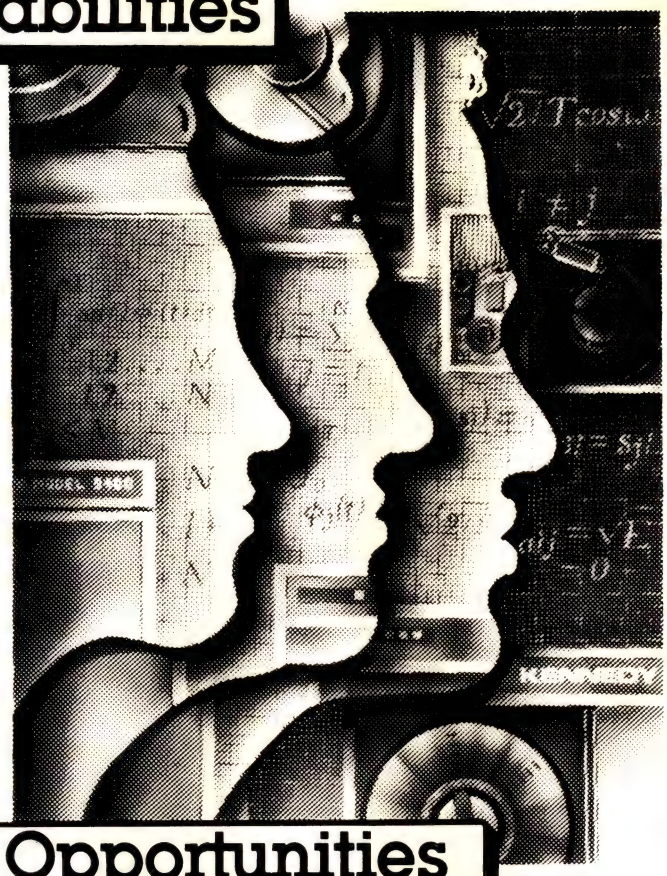
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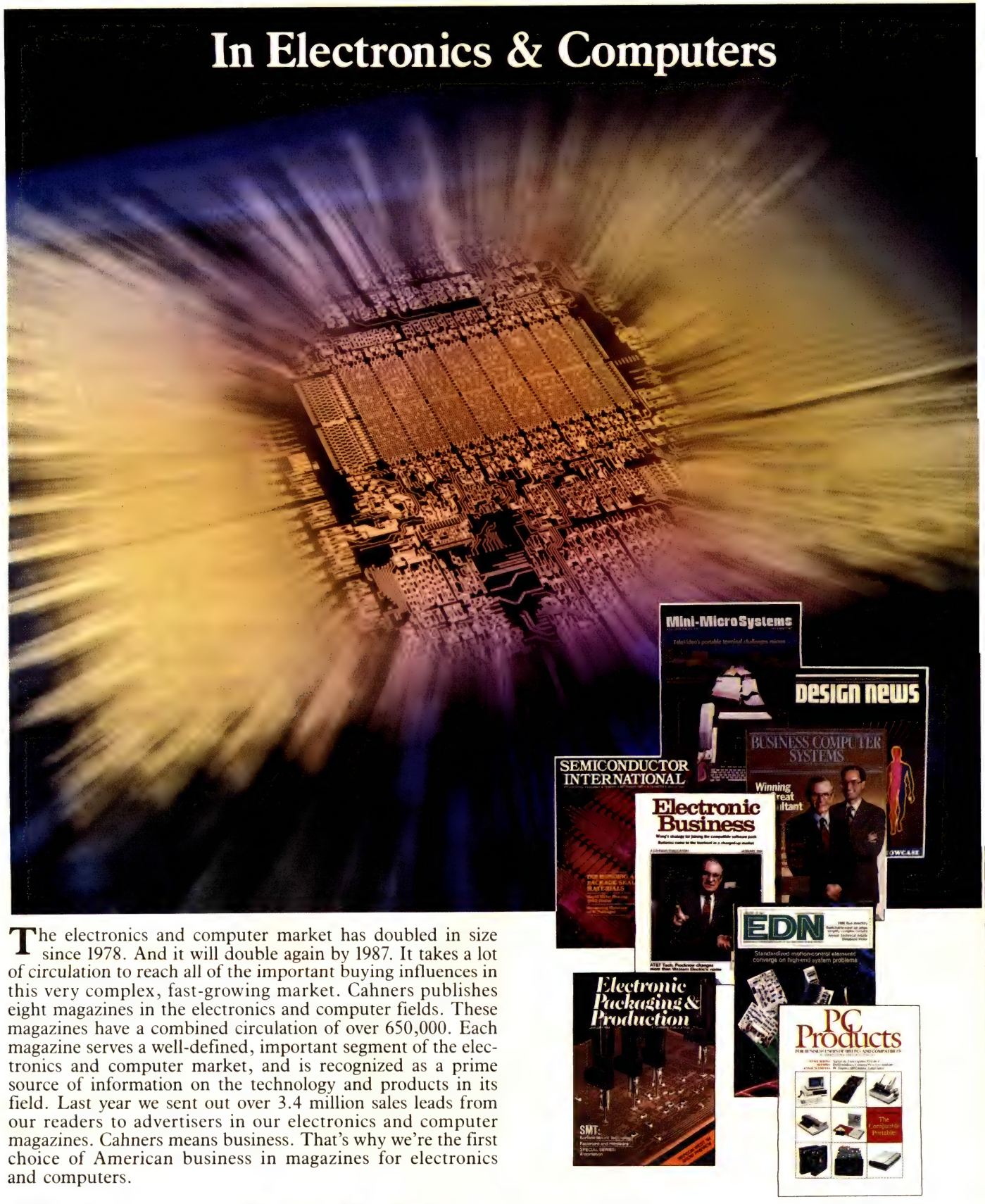
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LOOKING AHEAD

Edited by George Stubbs

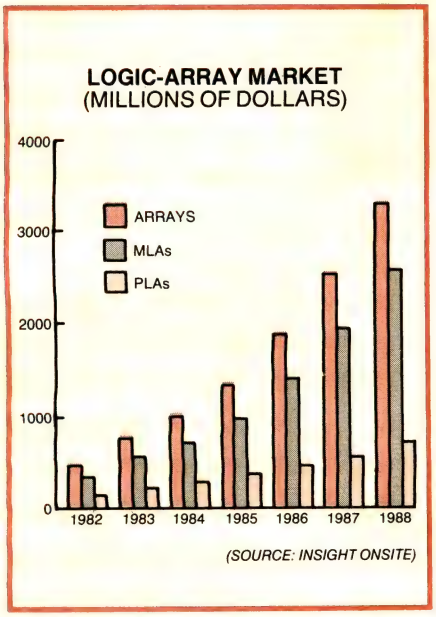
Standard-function ICs yield to custom circuits

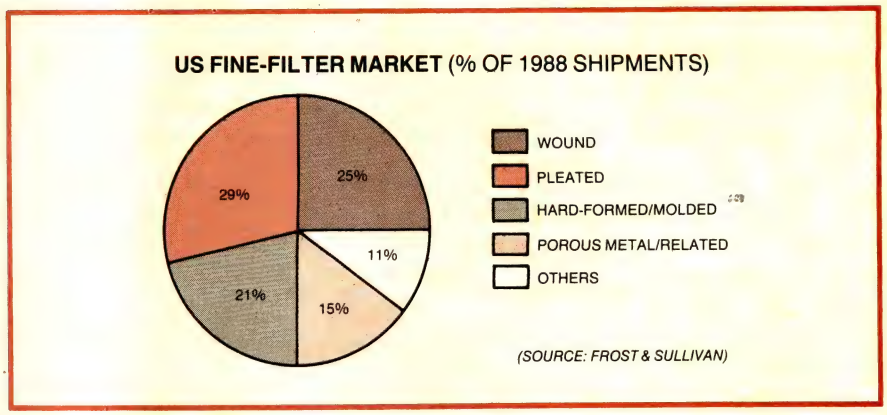
The demand for standard-function SSI, MSI and LSI circuits is shifting to a demand for custom arrays, according to Insight Onsite, a consulting group based in San Jose, CA. The company foresees a 33% growth rate in the worldwide merchant logic-array market between 1983 and 1988 to $3.3 billion, or 35% of the total logic market.

Masked logic arrays (MLAs) are expected to grow at a 36% rate to $2.6 billion. The programmable-logic-array (PLA) share of the array market, however, will drop from 29 to 22%, reaching a sales level of $710 million in 1988.

Two-thirds of the MLAs shipped in 1982 were in the speed range traditionally served by TTL. By 1988, 1- to 5-nsec devices should dominate. Insight Onsite also predicts that silicon-gate CMOS processing will be used for approximately 70% of all MLAs by 1988.

According to the firm, 72% of 1982's MLA shipments were gate arrays, 11% were cell arrays and 20% were standard cells. It expects the major growth to be in standard cells, with cell arrays gaining in market share.





Fine, ultrafine filters to reach $525M by 1988

The aim of semiconductor-device makers to protect microchips from impurities will spark the growth of the market for fine and ultrafine filtration equipment through the next several years, reports Frost & Sullivan, a market-research firm based in New York City. By 1988, shipments of filters and housings will reach $525 million, a 38% increase from 1983's $381 million.

Growth in the electronics industry's demand for fine and ultrafine filters is approximately the same: 14.2 and 14.3%, respectively. Such growth outpaces the demand of other industries. There is a significant need for the ultrafine filters in electronics, a direct result of the miniaturization of integrated circuitry. The filters must provide effective contamination control.

At $39 million, wound-cartridge models were the most popular of the fine-filter types, accounting for 29% of all shipments. Their popularity could shrink, however, as the trend continues toward finer filtration requirements. On the other hand, pleated models and porous-metal and related filters will gain in market share. The porous-metal types are costly but economically competitive in the long term because of their heat resistance, noncorrosive nature and ability to be reused.

Virtually all ultrafine filters are membranes in pleated or disk form. Cellulose types represented approximately one-third of all ultrafine-filter shipments in 1983, but they will grow at only a 2.6% annual rate. Nylon units have emerged as the clear leader among the cartridge types and will grow at nearly a 12% annual rate. Other types include Teflon, polyvinylidene-diflouride and polysulfone devices. Disposable units are also gaining market share, at the expense of disk units.

Packaged-software market to see tenfold increase

Through the next 10 years, $23 billion worth of *mini-* and microcomputer software packages will be sold, reports Frost & Sullivan. This marks a tenfold increase in that market, which is already booming.

Application packages, which are expected to account for $453 million in sales in 1984, should see that sales figure jump to $3.4 billion by 1993. Even more dramatic will be the growth in systems software through the same period, from $70 million to $2.5 billion.

The firm observes that system software (operating systems, database managers, compilers, etc), once the province of computer-hardware vendors, is now being successfully sold by software companies. Microcomputer system software is expected to account for 77% of the demand for system packages sold in 1984, rising to 91% of that market sector by 1993.

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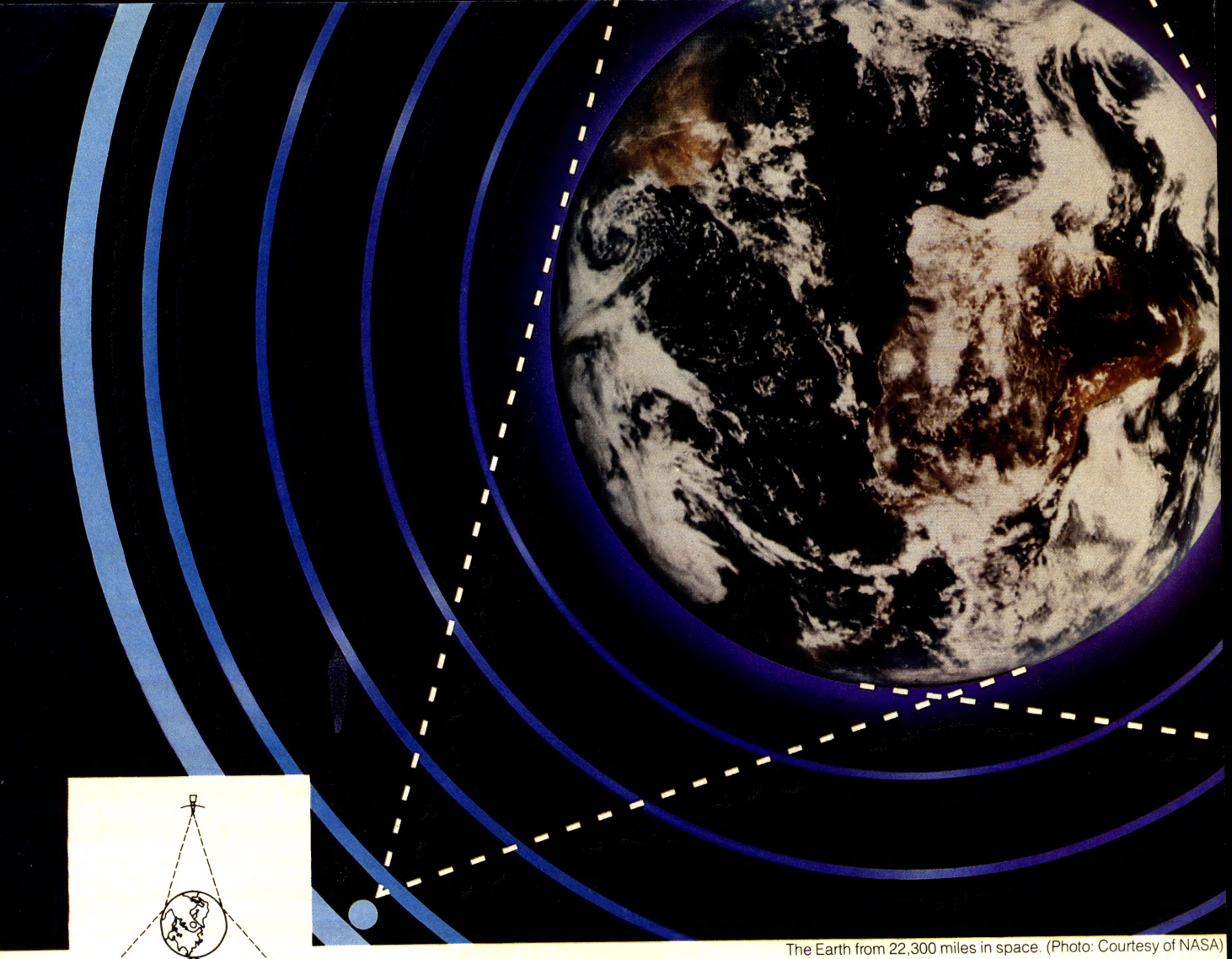
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The Earth from 22,300 miles in space. (Photo: Courtesy of NASA)

Clarke's proposed
3-satellite system.

FINDING NEW WAYS...

In 1945, Arthur C. Clarke—a British mathematician, wireless operator and creative science fiction writer found a better way to beam communications signals around the world. He theorized that an artificial satellite, carried by a rocket to an orbit 22,300 miles above the earth's equator and traveling at 6879 mph (the speed at which the earth rotates on its axis), would appear motionless to an observer on earth. From that height, Clarke reasoned, a radio relay station could cover one-third of the earth's surface; three such satellites, placed in geosynchronous orbit around the equator could provide worldwide communications. In 20 years, advances in electronics, miniaturization and rocketry made Clarke's dream a reality and gave the world improved communications capability.

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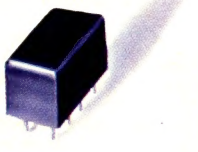
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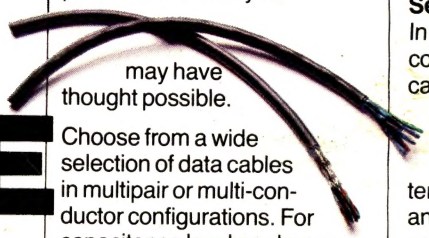


HOW TO RACE FASTER & LONGER DOWN THE DATA HIGHWAY

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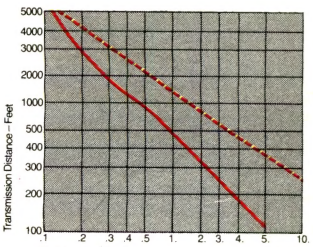
When data speed and distance set the limits to superior performance of your computer system, your design requires a new cable solution. Belden's new Extended Distance Data Cables provide faster data rates over longer distances while maintaining the integrity of the signal. This new series of data cables combines Belden's unique Datalene® foam dielectric or semi-rigid PVC insulation with superior shielding technology to achieve higher levels of performance than you may have thought possible.



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Bit rate vs. distance for individually shielded single pair cables.



Charts assume 5% peak to peak time jitter as determined by eye pattern measurements of pseudorandom NRZ code.

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